LIBERA

Libera Digit 125

The Libera Digit 125 is a **general purpose digitizer** with 4 channels and a sampling frequency of 125 MHz. The data is stored in a configurable buffer with max 8 M data samples stored per channel.

Highlights

- 4 channels sampled at 125 MS/s with 14-bit ADCs
- AC coupled and DC coupled versions
- 31 dB variable gain for DC version
- EPICS, Tango, Python, Matlab and LabVIEW compatible
- Passive cooled, PoE compatible

Applications

- Particle accelerators
- High energy physics
- Nuclear and particle physics
- Dark matter and astroparticle physics

AC and DC coupled versions

The DC-coupled version has a front-end with 40 MHz bandwidth, suitable for time-domain processing of signals coming from different types of sensors.
The AC-coupled front end has a bandwidth ranging from 10 MHz to 700 MHz and is suitable for narrow-band signals and digital down-conversion applications.

Flexible data buffering

One LEMO trigger input is used to trigger the data acquisition in a large ADC buffer with total size of 8 MS per channel. The data buffer size can be reduced in order to support higher acquisition trigger frequencies.

Network connected with several software interfaces

The instrument is accessible via the network, and several standard interfaces are available to facilitate the integration of the instrument into the control system. Besides the EPICS and Tango interfaces, the instrument can also be connected via a TCP-IP socket, enabling connections with Python, LabView, Matlab and others. The operating system is Linux-based and loaded via a Micro-SD card or a TFTP server.

Octave LabVIEW EPICS TANGO python MATLAB

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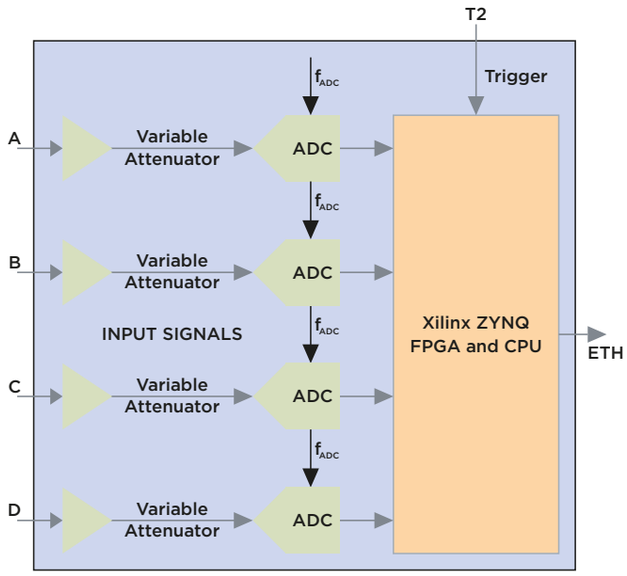
INSTRUMENTATION TECHNOLOGIES

Low power and no maintenance required

The Libera Digit 125 digitizers are based on the Xilinx ZYNQ SoC family, with low power consumption which enables the devices to be powered over Ethernet (PoE standard) and passive cooled.

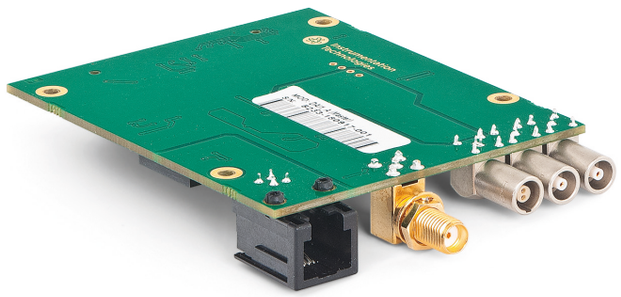


Technical Specifications

Libera Digit 125	
Dimensions	44 mm × 210 mm × 210 mm
Input signals and connector	4, SMA connector
Maximum input signal level	AC-coupled: ± 1 V @ 50Ω DC-coupled: ± 5 V @ 50Ω, 1.25 V @ 1MΩ
Input gain / attenuation	31 dB
Input signal bandwidth	AC-coupled: 10 MHz – 700 MHz DC-coupled: 40 MHz
Input impedance	AC-coupled: 50 Ω DC-coupled: selectable 50 Ω / 1 MΩ
Trigger signal level and connector	3.3 V TTL, LEMO connector
ADC conversion	125 MSps, 14 bit
FPGA / CPU	Zynq-7020 / ARM Cortex-A9
Booting	Micro-SD, TFTP server
Power	PoE
Cooling	Passive

HW extensions and further development

Extension module
An extension module can be added to the digitizer to extend the connection capabilities of the device.



Interface	Description
LEMO single (2x)	Single-ended LEMO, Input/Output configurable
LEMO differential (1x)	Differential LEMO, Interlock output (requires external circuit)
SMA (1x)	16-bit 100 kSps DAC output, 1 V at 50 Ohm
RJ-14 (1x)	6p6, up to 20 Mbps, half-duplex

FPGA / Software code availability

The Libera Digit 125 can be further extended by the user with modifications to the FPGA and software code (available under a non-disclosure agreement). Additional features or functionalities can be also added by our developers. For more information contact us at support@i-tech.si.

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