INSTRUMENTATION
TECHNOLOGIES

LIBERA

Introducing the new Libera Brilliance X

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Agenda

- Introduction
- Hardware modules
- Installation and interfaces
- Software and FPGA
- Measurement performance
- Availability

Introduction

L I B E R A B R I L L I A N C E X

Libera Brilliance X is a modular beam position processor based on the MTCA.4 technology. It has been developed in collaboration with DESY for PETRA-IV project.

Highlights:

- High channel density: 2 or 4 BPMs in 1U chassis
- Measurement performance: sub-micrometer RMS turn-by-turn
- Longterm stability: sub-micrometer variation over a week
- Functionalities: turn-by-turn (also multi-bunch), long buffers, parallel data access
- Fast Orbit Feedback: ready for integration (e.g. to star-topology)
- Software: Libera BASE with EPICS, TANGO, HTTP, TELNET interfaces

The X relates to the MTCA.4 technology.
It is also a rotated + which is part of Libera Brilliance+.

Libera Brilliance X

Front panel

DAMC-UNIZUP

(digital part, FPGA)

CPU module

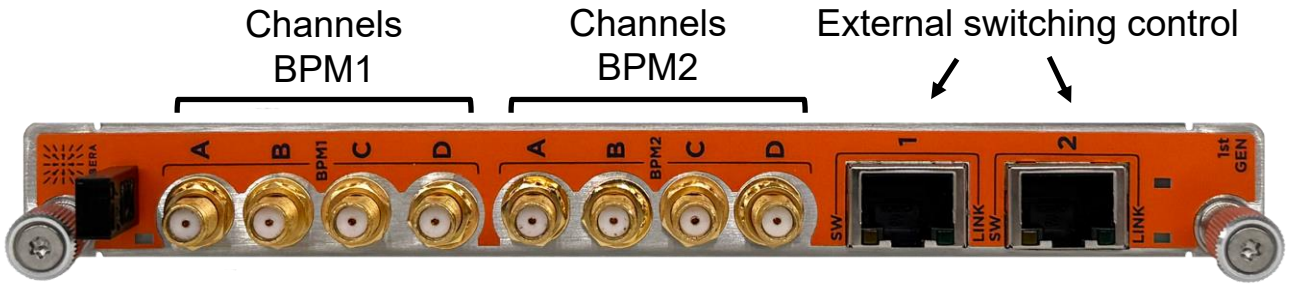
Back panel

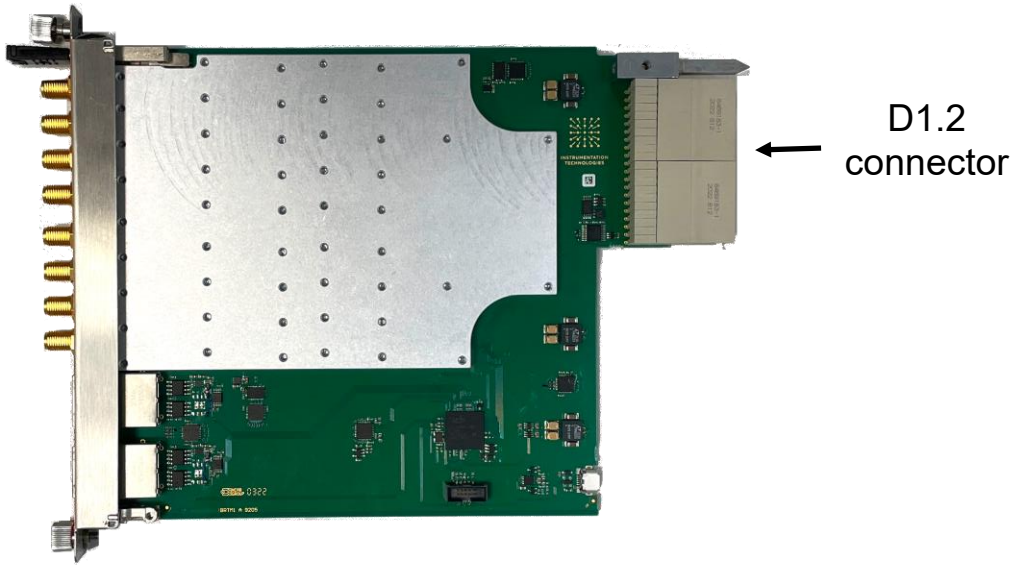
Power supply module

Libera 2BPMRTM

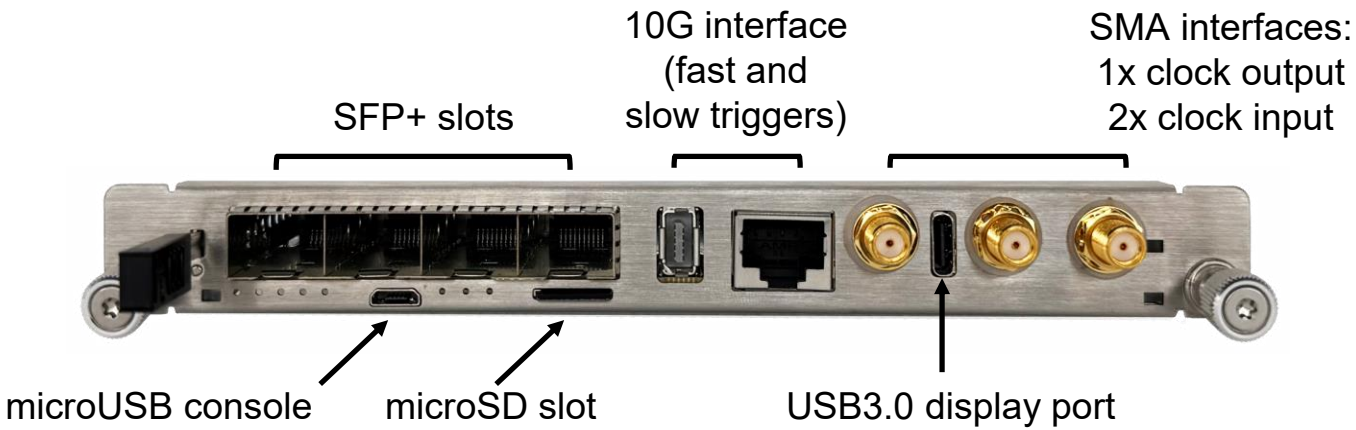
(analog front-end)

Modules: RTM
Libera 2BPMRTM

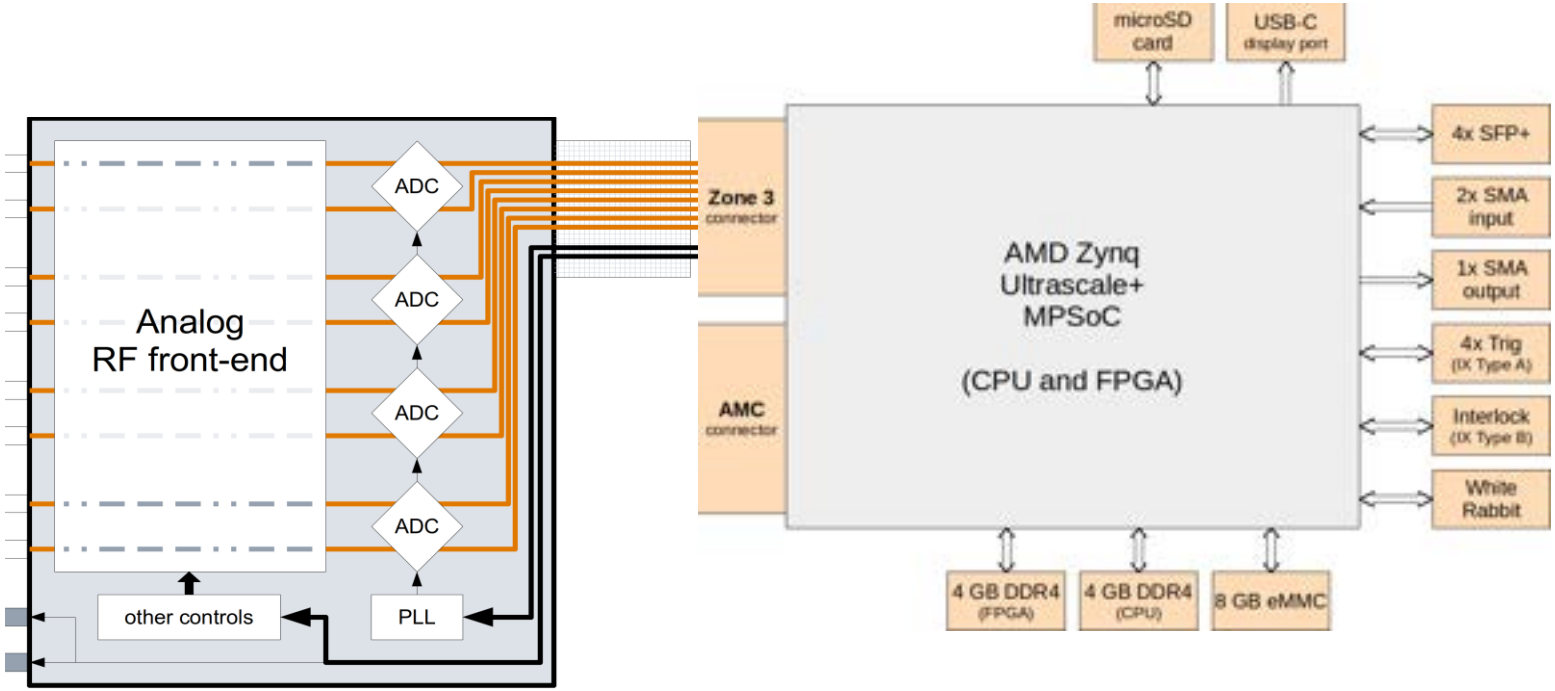




Modules: AMC DAMC-UNIZUP



Modules: RTM + AMC



Technical specifications

Libera 2BPMRTM

- 8 channels: **BPM1** (A,B,C,D) and **BPM2** (A,B,C,D), 50 Ohm
- 31 dB programmable attenuation
- **No cross-bar switch**
- 2 RJ-45 interfaces for external switching control

Specifications	
Input signal frequency range	500 MHz (available) 352 MHz (on request)
A/D converters	125 MHz, 16 bit
Maximum crosstalk	**-76 dB** between 4 channels **-95 dB** between BPM1 channel D and BPM2 channel A
Input noise density	**-144 dBm/Hz** (31 dB attenuation) **-169 dBm/Hz** (0 dB attenuation)

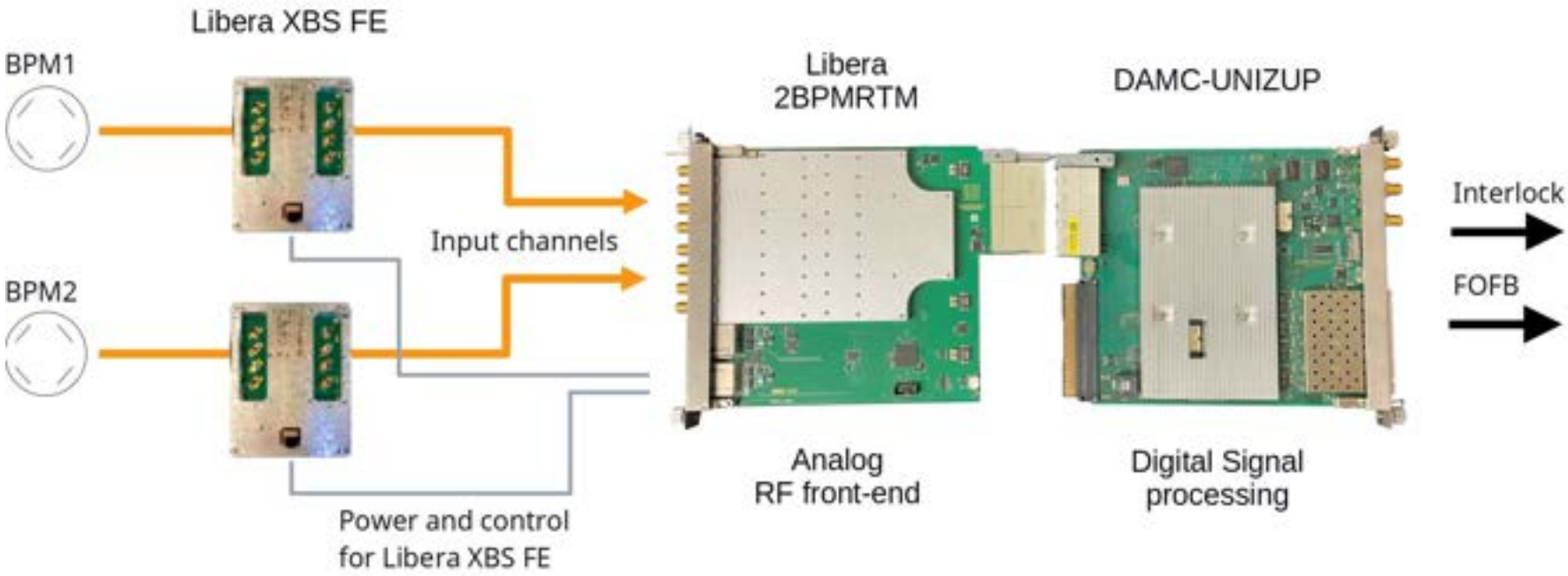
Technical specifications

DAMC-UNIZUP

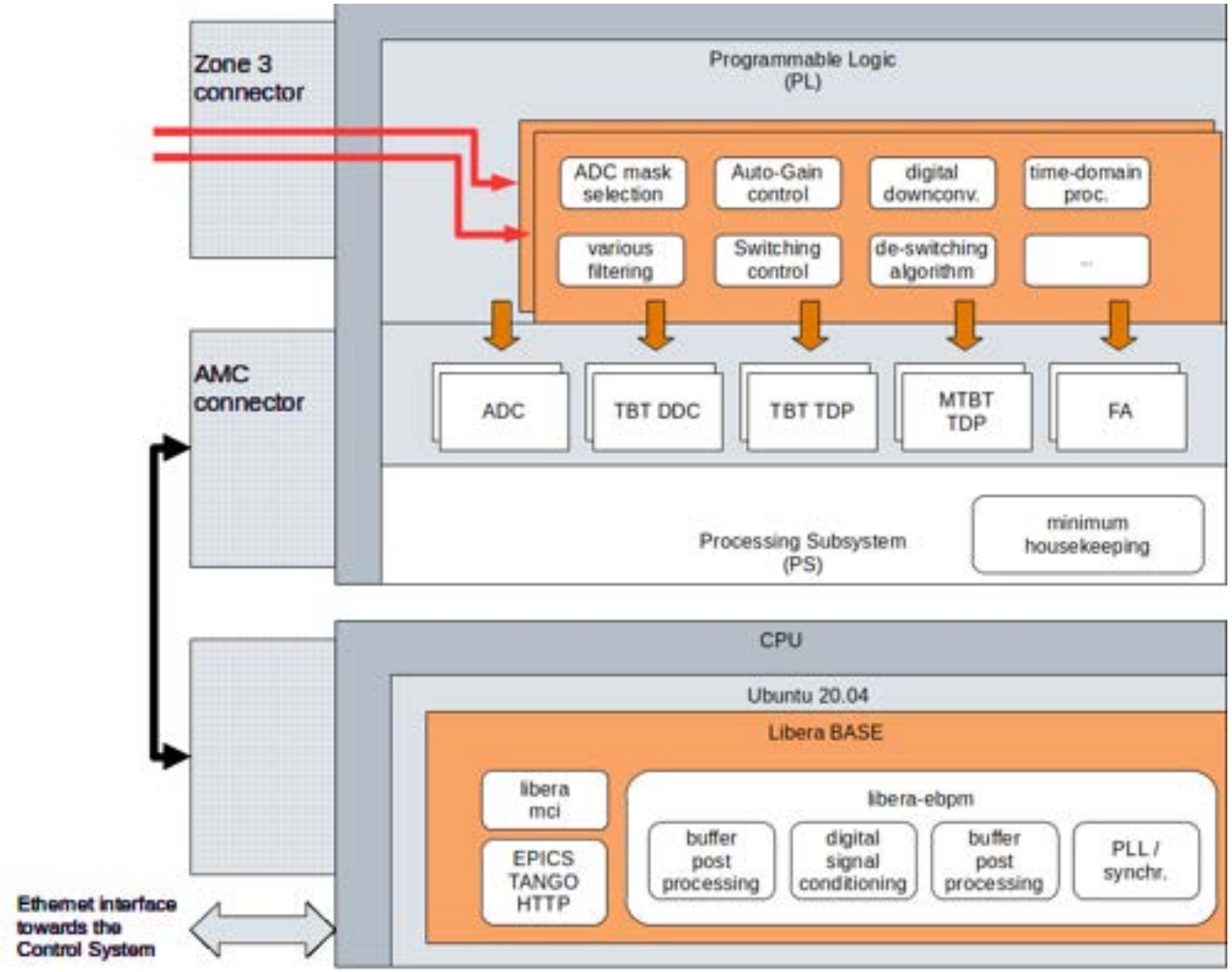
- developed by DESY, licensed and produced by Instrumentation Technologies
- several assembly options: Zone 3 connector, trigger configuration, MPSoC option
- can work standalone: USB-C display port, Ethernet to PS, Linux in Zynq
- module version 2 currently in production (RJ45 replaced by IX interface)

Category	Details
MPSoC Options	AMD Zynq UltraScale+ XCZU7EG or XCZU11EG
CPU	Dual/Quad-Core ARM Cortex-A53, 1.2 up to 1.5 GHz
Memory	4 GB DDR4 (PS) at 2400 MT/s + 4 GB DDR4 (PL) at 2660 MT/s
PCIe	Gen3 x4 or Gen3 x8 support, depending on RTM class config.
Compliance	MTCA.4.1 D1.2/D1.3, full M-LVDS and DESY interlock support
Connectivity	4x SFP+ (up to 16.375 Gbps), USB Type-C display port, USB3.0, IX trigger and interlock connectors

Installation and interfaces



FPGA and Software



DAMC-UNIZUP

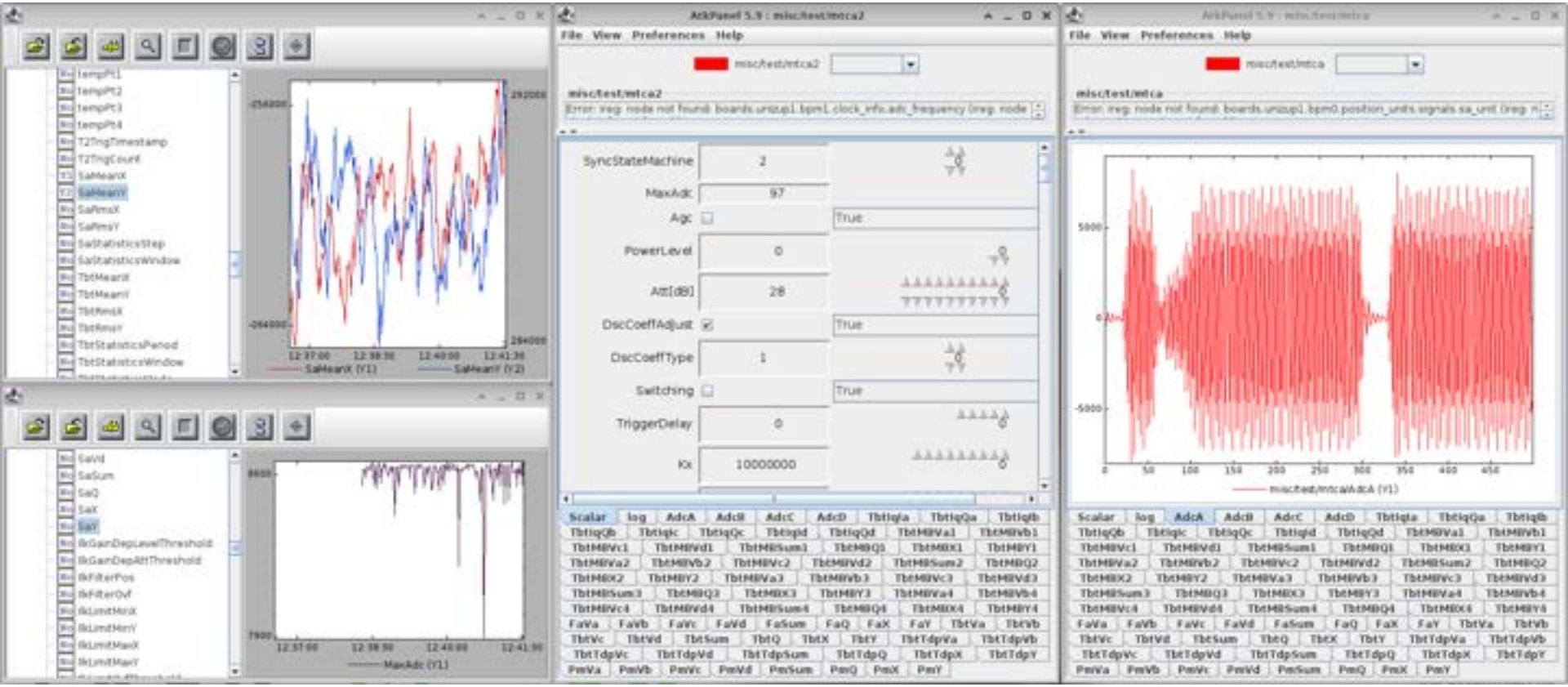
CPU module

Control System interfaces

EPICS 7.0.9, CSS Phoebus

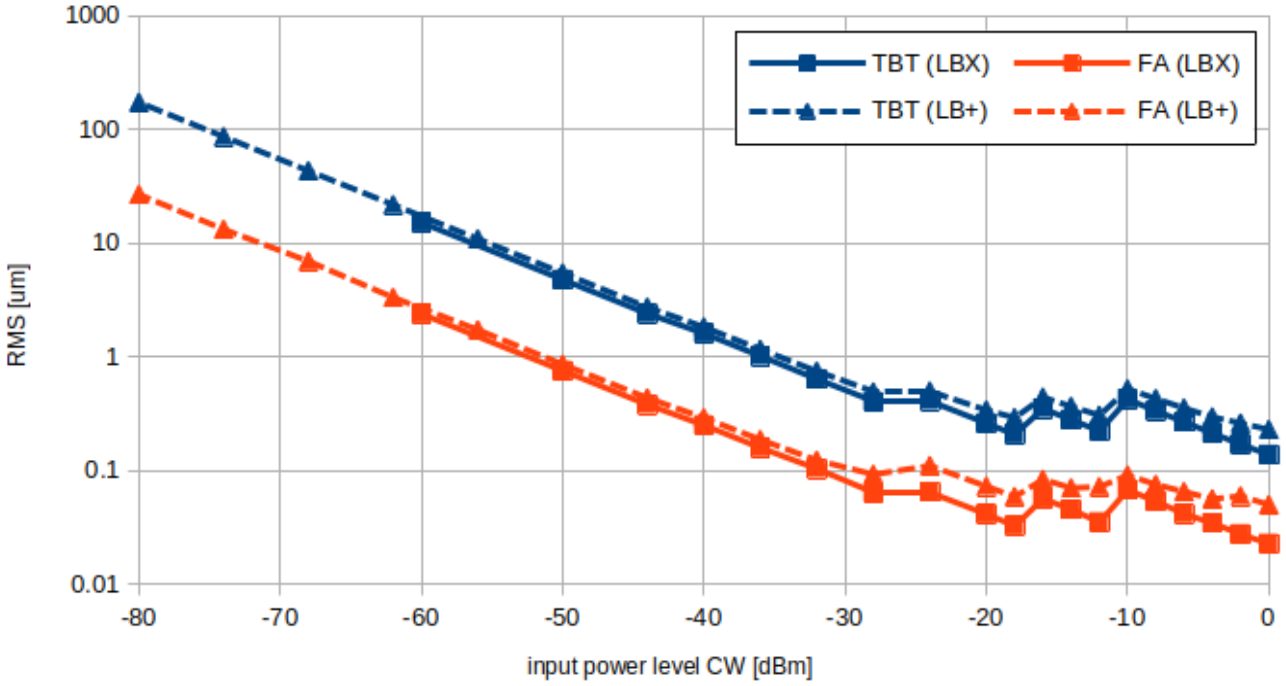
Control System interfaces

TANGO 9.5, AtkPanel



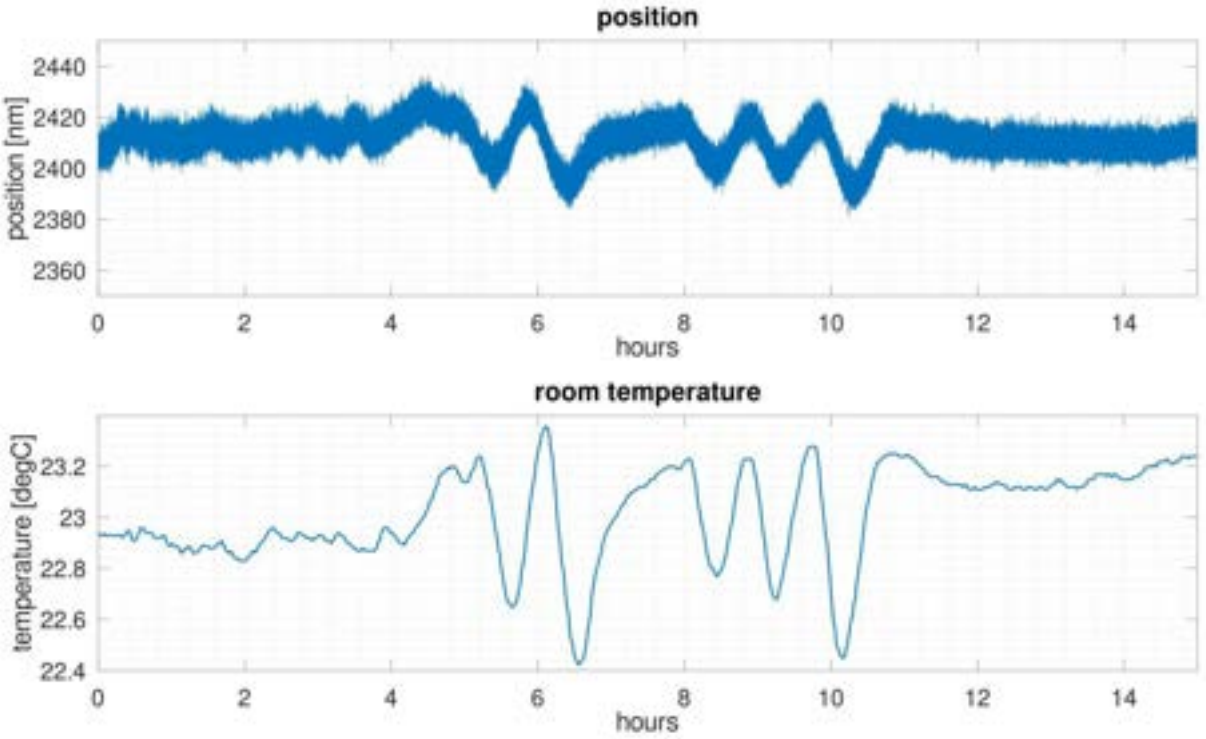
Measurement performance

- Same or better RMS performance than Libera Brilliance+
- Similar beam-current dependence (centered and off-centered)



Measurement performance

- 16-hour test in laboratory environment
- 1 degree Celsius peak-to-peak temperature variation
- ~40 nm peak-to-peak position variation



Availability

… in various form factors

12 BPM system

at DESY PETRA-III

(since 2022)

2 (4) BPM system

Prototype

(will be tested next week at BNL NSLS-II

Availability

System options:

- Crate size (+power supply, CPU and MCH)
- RTM module (Libera 2BPMRTM, frequency dependent)
- AMC module (DAMC-UNIZUP)
- Other than BPM application?
- Availbility from year 2026

sales@i-tech.si

Thank you!

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