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FIRST BEAM-BASED TEST OF FAST CLOSED ORBIT FEEDBACK SYSTEM AT GSI SIS18

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Abstract

The SIS18 synchrotron of GSI will serve as a booster ring for the SIS100 synchrotron in the FAIR project. In order to counter orbit distortion due to cycle-to-cycle hysteresis of the main magnets and stabilize the beam orbit during the full acceleration cycle, a global closed orbit feedback (COFB) system is being implemented in context of both synchrotrons. The primary design goal of the system is robustness against variations of the beam and machine settings. These variations are unavoidable due to large expected dynamic range in beam intensity and flexible machine settings at the FAIR facility. The detailed architecture of the system is discussed in this contribution. First beam-based tests for orbit correction were performed with a large spatial model mismatch, when the orbit response matrix corresponding to injection energy was used for the entire acceleration ramp only taking the beam rigidity into account. The result of these preliminary tests is also presented.

INTRODUCTION

The maximum beam intensities in FAIR (baseline) design goal are an order of magnitude higher in comparison to operational GSI facility [1,2]. This introduces stricter conditions for both machine protection and beam quality conservation in FAIR synchrotrons SIS18 and SIS100. These requirements translate directly into a better control of the closed orbit through SIS18 into SIS100. Further, the creation of fast dynamic orbit bumps and the possibility of orbit correction during the acceleration ramp impose a requirement of at least 100 Hz bandwidth taking model mismatch into account [3,4]. Although the COFB system is mainly conceptualized for SIS100, the prototyping is being performed at the operational SIS18 as further discussed in this paper.

SIS18 is a versatile synchrotron capable of accelerating particles ranging from protons to Uranium ions with a variety of charge states, with the maximum energy corresponding to the magnetic rigidity of 18 T-m. There is a (unique) optics transition from triplet to doublet quadrupole configuration during the acceleration ramp in order to incorporate a larger beam size due to multi-turn injection. This results in an on-ramp lattice model variation. A large dynamic range in beam intensity requested by experiments introduce more challenges, such as a) intensity dependent tune shifts, b) gain and offset calibration errors in the BPM system due to amplifier gain ranges and c) coupling of dipole magnet fields into matching transformers of the BPM system especially for lower beam intensities. These conditions lead to different design goals of our COFB system in comparison to those implemented in the light sources and colliders where the beam settings and machine model are typically fixed as well as the reference orbit is expected to be static during the beam storage.

Consequently, we aim for a COFB system which is robust against the changes in orbit response matrix (ORM), reference orbit changes, cycle to cycle changes in beam intensity as well as BPM and steerer magnet hardware and communication failures. There are 12 shoe-box type pick-ups and 12 steerer (corrector) magnets per plane, symmetrically distributed in the 12 sections of the SIS18 lattice [5]. The feedback system is tuned to operate with these existing BPMs and steerer magnets. In the scope of this paper, we report on the hardware layout, infrastructure dependencies, design overview, and the first beam based test of the SIS18 COFB hardware.

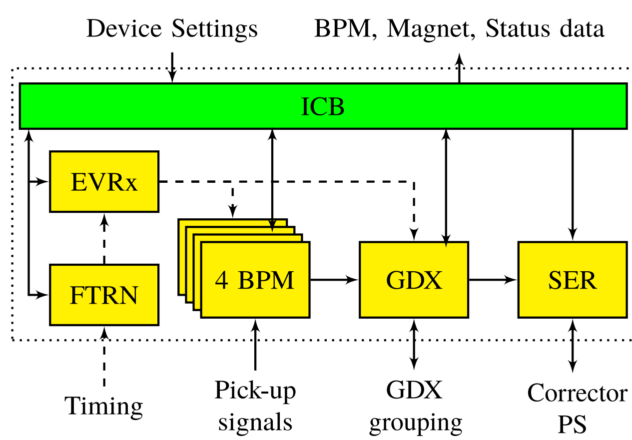

Figure 1: Libera Hadron hardware layout.

COFB HARDWARE LAYOUT

Libera Hadron platform B is the Slovenian in-kind contribution for beam position calculation and closed orbit feedback system targeted at SIS-100 and is utilized for these tests in SIS-18. It contains dedicated Beam Position Monitor (HBPM) modules for the data processing from upto four pick-ups, Gigabit data exchange (GDX) module for beam position data exchange with other GDX modules and feedback algorithm implementation and Serial communication

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module (SER) for supplying current values to the corrector power supplies. Two additional timing and trigger related modules are present, Fair Timing Receiver Node (FTRN) for obtaining the machine events from the General Timing System (GMT) of the FAIR facility, and EVent Receiver module (EVRx) for generating triggers based on FTRN inputs. A board computer with an Measurement and Control Interface (MCI) is in place for user communication with all the modules. Figure 1 shows the block diagram for these modules in the order of signal flow from BPMs to the corrector magnets.

Since each Libera Hadron platform B is equipped with four beam position processor modules, a total of 3 Libera Hadron platform Bs (shown in Fig. 1) are connected with the 12 pick-ups and 12 steerers forming the global closed orbit feedback system. Further details of each module is discussed below.

FTRN and EVRx Modules

Every component hardware (or front end) used for control or measurement of the beam in FAIR/GSI is attached to a Front End Controller (FEC) computer. The BPM hardware "Libera Platform B" is thus a FEC equipped with a FTRN within the GMT for FAIR and GSI [6]. The FTRNs are connected via optical SFP transceiver modules to a White Rabbit (WR) timing network. WR synchronizes the internal clocks of all FTRNs in sub-ns precision and distributes timing information. In the GMT, an accelerator cycle is divided into several beam processes where the point of time when a beam process will start is exactly known. This information is used to program the FTRNs with upcoming events in advance - like setting an alarm clock - so that trigger actions can be performed on all FECs synchronously. Non deterministic events such as the interlocks and in-cycle beam requests are also handled as elaborated in [6]. For the COFB system, FTRN uses two trigger outputs which are connected via Libera's backplane to the EVRx module. One trigger is used to start the specific DSP functions in HBPM modules (such as position measurement) and the other one is used to start the feedback system independently. In addition, FTRN generates a continuous 10 MHz clock signal which is connected via front panel output to the EVRx's front panel Machine Clock (MC) input. The EVRx has a Phase Locked Loop (PLL) which uses the MC input to generate the 250 MHz clock signal for the HBPM modules so that sampling of all BPM pick-up signals of an accelerator is performed synchronously.

HBPM Module

Each HBPM module digitizes the 4 pick-up channels at 250 MSa/s representing it into 4 16-bit values referred to as the raw ADC data. The raw data data is processed into the bunch-by-bunch data, Fast acquistion (FA) (at 10 kHz) and Slow acquistion (SA) (at 100 Hz) streams in the FPGA. The raw ADC and position data, along with accompanying timing and status data is stored into dedicated buffers, according to the received start/stop trigger events. Dedicated 2 GB buffer for raw ADC data enables data acquisition with maximum acquisition length of 268 M samples available as data on demand. Similarly, the bunch-by-bunch data is stored in another dedicated 2 GB DDR RAM buffer. Presently two position calculation algorithms options are available, "bbb" [7] or Narrow-Band Analysis "nba" algorithm. Presently a new fit based position calculation algorithm is being implemented [8, 9]. The "FA" data stream from all 4 HBPM modules is transferred synchronously to the GDX module via LVDS links.

GDX Module

Gigabit Data eXchange (GDX) module offers fast (6.5 Gbit/s) links (SFP connectors) with GDX modules on the other Libera modules through which the orbit data is transferred at 10 kHz rate in hard real time. The local FA data from the BPM modules is obtained through LVDS links. The heart of the GDX is an FPGA where the feedback algorithm is implemented. The algorithm relies on the inverted and decomposed orbit response matrix (ORM) matrices and Proportional-Integral (PI) controller parameters. This data along with the measured and reference orbits is used for the execution of COFB algorithm at a rate of 10 kHz. The calculated correction currents are delivered to the SER module. A COFB algorithm design and implementation is the subject of next section.

SER Module

The SER builds the interface between GDX and Adaptive Control Unit (ACU) which is the modular control system of a corrector magnet power converter developed in-house. SER provides eight RJ-45 ports where each one can be used for a point-to-point connection with an ACU. Data transmission is done over these ports by the Universal Serial Interface (USI) [10]. USI was developed along with the ACU to interconnect different components of a power converter and includes a RS-485 based protocol for communication. The GDX module sends 8 user-selectable 20 Bit wide magnet correction values out of the whole M correction vector to the SER module with 10 kHz data rate synchronous to the COFB execution rate. The SER module caches these corrections in a buffer. For communication via USI, the ACU always has to act as master and polls the data from the SER module asynchronously.

In our setup Cat 6 cables have been used on the physical layer and a maximum baud rate of 16 MBit/s has been reached for a cable length of 30 m. At our chosen baud rate and with total protocol overhead, the maximum polling rate is then 133 kHz. In the "synthetic generator" operation mode the SER can also generate fixed or swept sine functions as correction value output which can be used to measure the orbit response matrix.

COFB DESIGN OVERVIEW

The data interfaces of the GDX FPGA module along with the internal COFB design details are shown in Fig. 2. Each

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of the important conceptual design blocks are discussed below.

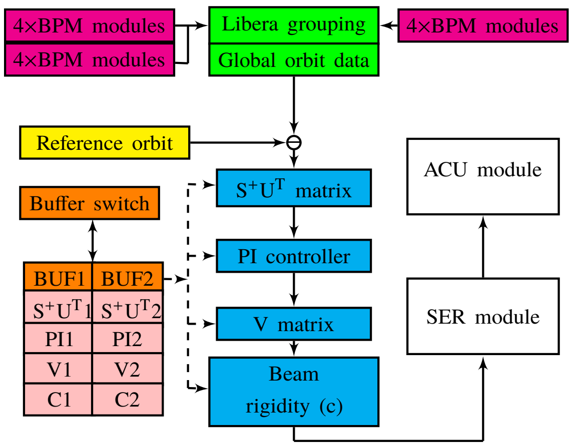

Figure 2: SIS18 COFB design overview.

Global Orbit Data

The FA data streams from all HBPM modules on a Libera are transferred to the GDX with low-latency over the back-plane. To gather position data of other BPMs in the accelerator, the "Libera Grouping protocol" is used. For the grouping, GDX uses two SFP slots with optical transceiver modules to build a dedicated network with all other Liberas in a daisy chain. In this grouping network global orbit data packets are passed from one GDX to the next where each GDX inserts the sum, position and status data of the connected HBPM modules. The latency of the Libera Grouping is in the range of 0.1 µs per BPM and thus is capable of distributing the current global orbit data within 10% of the 100 µs time slice for orbit correction. Synchronism between all the BPM modules is required and is achieved by starting the data chains at a specific time on all Liberas using the WR trigger scheduling mechanism.

Double Buffering

The orbit response matrix inverted and decomposed into $\mathbf{S^{+}U^{T}}$ and $\mathbf{V}$ matrices along with the reference orbit and beam rigidity vector C are supplied by the user. Since the optics and therefore these matrices vary during the acceleration cycle, it requires constant updating of the matrices during the orbit correction cycle. All matrices and vectors ($\mathbf{S^{+}U^{T}}$, $\mathbf{V}$, C and reference orbit G), along with the PI controller parameters, are double buffered in FPGA in order to guarantee data atomicity, and to allow their updates to be performed in a pipelined manner. During the orbit correction, one buffer is active and the other is available for parameter loading. The various data and the associated symbols are explained in Table 1.

PI Controller

The controller implemented in feedback system is a classic Proportional-Integral (PI) controller, featuring an anti-windup algorithm. Whenever the PI controller output saturates, the I accumulator (ACU) is held constant. The integrator is reset at each COFB_ON trigger event. The implementation provides the liberty of using different controller gains $\mathbf{k_P}$ and $\mathbf{k_I}$ for each of the SVD mode, a unique feature of this implementation. Figure 3 shows the PI controller schematic for the j^{th} SVD mode.

Table 1: The symbols of the signals and matrices used in the COFB algorithm.

Symbol	Description
$\mathbf{p}$	Measured orbit column
$\mathbf{r}$	Reference orbit column
$\mathbf{S}$	SVD singular matrix
$\mathbf{U}$	SVD left orthogonal matrix
$\mathbf{k_P}$	Proportional gains colomn
$\mathbf{k_I}$	Integral gains coloumn
$\mathbf{V}$	SVD right orthogonal matrix
θ	Corrector currents (A)
$\mathbf{c}$	Radian to current conversion
M	Number of BPMs
N	Number of corrector magnets
J	Number of corrected SVD modes

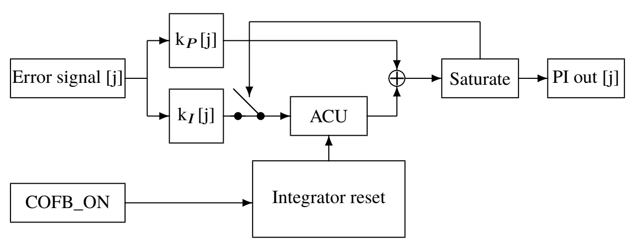

Figure 3: Detailed schematic of the PI controller block for j^{th} SVD mode.

Calculation of the Corrector Strengths

The global orbit vector is distributed among all GDX modules with the Libera Grouping protocol. Thus, each GDX module serves as data processing unit (DPU) where all corrector values are calculated. The correction algorithm is implemented in the FPGA of the GDX module and is described with the following equations.

$$\Delta\mathbf{p_{M\times1}} = \mathbf{r_{M\times1}} - \mathbf{p_{M\times1}} \quad (1)$$

$$\theta_{N\times1} = \mathbf{c}\mathbf{V}_{N\times J}(\mathbf{k_P} + \mathbf{k_I}\int \cdot)_{J\times J}[(\mathbf{S^{+}U^{T}})_{J\times M}\Delta\mathbf{p}_{M\times1}]$$

where $\mathbf{k_P}$ and $\mathbf{k_I}$ are the diagonal matrices having the controller gains at the diagonal locations in order to ensure the mode-by-mode multiplication to $\mathbf{S^{+}U^{T}}$. Specific BPMs and magnets can be removed from the calculation by setting the respective columns in $\mathbf{S^{+}U^{T}}$ and rows in $\mathbf{V}$ matrices to null. Reduced number of SVD modes can be used for calculation either by setting the lower rows in $\mathbf{S^{+}U^{T}}$ to null or PI controller gains of those modes to zero. The rigidity evolution vector $\mathbf{c}(t)$ translates the corrector strength into correction currents taking into account the evolution of beam magnetic rigidity of the beam during the acceleration. The correction

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currents for the selected magnets are sent to the SER module. Corrector value calculations can only be performed for a single, user selectable plane per Libera unit.

COFB Validity State Machine

The Validity State Machine (VSM) is responsible for controlling (stopping & resuming) the COFB feedback in the following way: The VSM is de-activated 1) whenever no bunch-by-bunch data is available within one period of orbit correction) 2) whenever an overload or underload occurs 3) whenever the result of Libera Grouping is not valid (missing data in vector P) and 4) whenever there is a fault on the ACU side. Each of these causes can be hidden using "masks". The effect of the VSM becoming de-activated is: a) The error signal fed to the PI controller is set to null b) The magnet output is either set to the integral part of the last calculated valid magnet correction value or to constant values, predefined by the user.

The VSM is activated: 1) Immediately after the conditions which led to its deactivation become valid (e.g. bunches get detected), if the "Auto Resume" signal is true. 2) After a manual user resume. The error signal is connected to the input of PI controller when the VSM is activated.

TEST WITH BEAM

The synthetic generator functionality is used for the orbit response measurement over the entire acceleration cycle. Excitation of the correctors one after another on all 12 correctors with position recording on all BPMs provide all the rows of the ORM. Figure 4 shows the closed orbit oscillations on 3 selected BPMs (marked according to the section names 1, 4 and 10 in SIS18) as a result of an excitation signal of frequency of 10 Hz and amplitude 2.8 V at the corrector marked as 1 in SIS18. The relative amplitude of the closed orbit oscillations change during the acceleration ramp due to the on-ramp ORM variation in SIS18. The synthetic generator is also used to obtain the temporal characteristics of the closed loop.

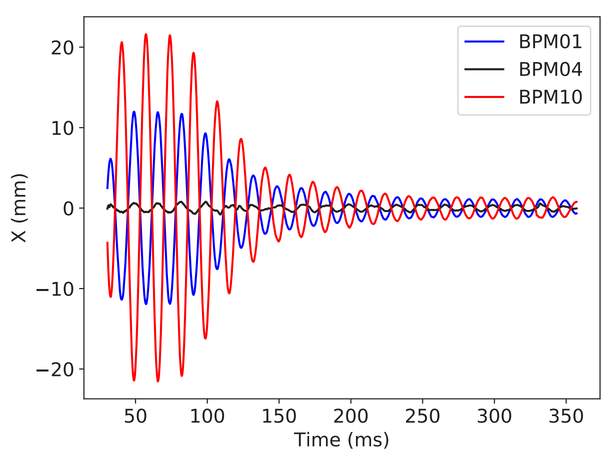

Figure 4: ORM measurement: measured beam position at three BPMs in x-plane over the entire ramp as a result of excitation at corrector 1 with the help of internal synthetic generator.

Orbit Correction Over the Ramp

The closed orbit system was tested with beam in early 2019 for the first time. Figure 5 shows the beam position at all 12 BPMs before and after the orbit correction. After the multiturn injection, the rf is adiabatically turned on, forming the bunches. Following the bunch formation, the closed orbit feedback system was turned on, marked as the beginning of Fig. 5. The acceleration ramp started at 40 ms and continues until 300 ms. Only 10 out of 12 SVD modes were used in order to ignore the dispersion induced orbit shift (visible as a residual in the corrected orbit). The orbit correction over the entire ramp was performed using a fixed ORM corresponding to the injection energy resulting in a large model mismatch. The COFB system was switched off after 260 ms and beam positions return to their original uncorrected values afterwards. After the tests, it came out that the communication to two of the steerer magnets was lost due to longer cables (40 m) between SER and ACU modules. Therefore effectively only 10 steerers were used for the correction and explains the small orbit residue left after correction.

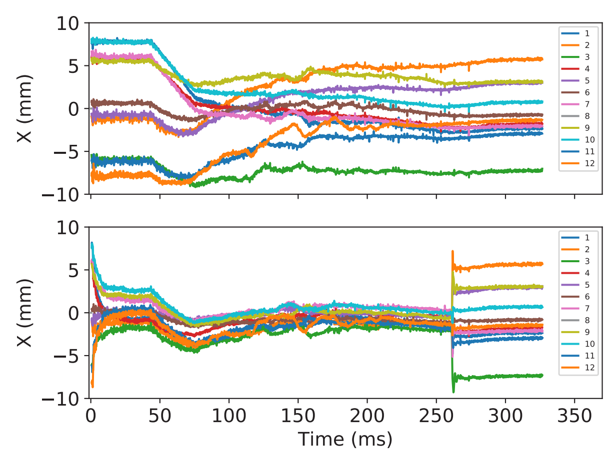

Figure 5: Orbit correction over the acceleration cycle in SIS18. The controller gains $k_P = 0.15$ and $k_I = 0.03$ for all modes.

These tests will be continued in upcoming Engineering run in the fall 2019.

CONCLUSION

A new closed orbit feedback system has been developed for SIS100 synchrotron of the FAIR facility and is tested at the synchrotron SIS18. The heart of the COFB hardware is Libera Hadron platform B consisting of dedicated modules for BPM data processing, timing event decoding and trigger generation, orbit data exchange and correction algorithm and communication with the corrector power supplies. In order to incorporate the ORM variation resulting from the machine settings variation during the acceleration ramps, a double buffering is implemented in the FPGA. A classic PI controller is implemented with the possibility of different gains for each SVD mode. The initial beam-based tests were performed with promising results.

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