DAMC-UNIZUP: Universal MPSoC-based Controller Board

Michael Fenner April 17th 2024

Libera Workshop 2024, Dobro

© DESY 2024





Agenda

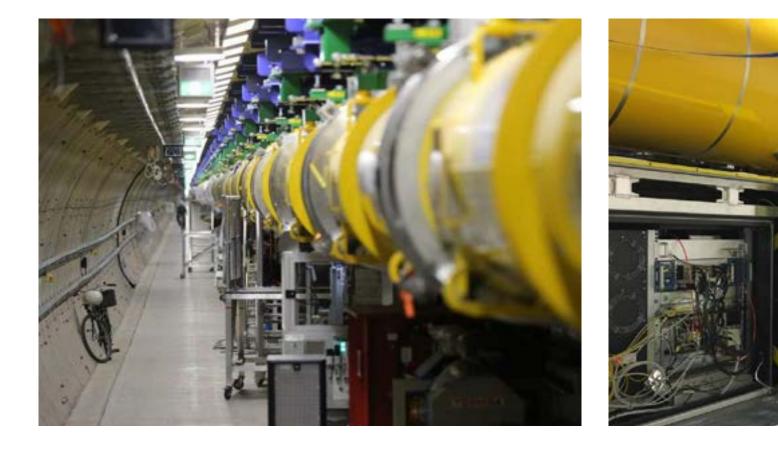
Our Background DAMC-UNIZUP "Tool Boxes" for the Community





Background

- DESY MSK = Accelerator Beam Controls
- Responsible for LLRF electronics of large FLASH and XFEL (and other) accelerators:
- As part of large DESY team: concept, design, installation, operation and maintenance
- Compl. development "in-house": hardware (schematics, board, test), firmware and software design
- 10 years+ of electronics life time (hostile environment), 24/7 operation, limited access to electronics





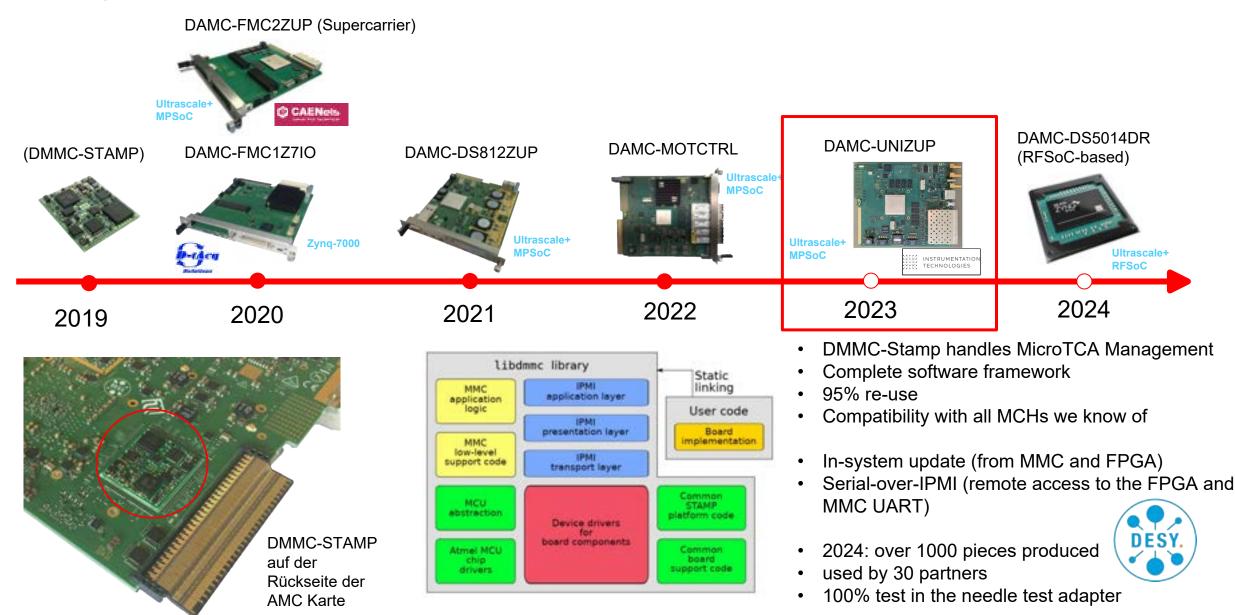
Licensing Strategy

- We promote an ecosystem
- DESY has licensed almost all developments: components are available for us and for third parties
- Strategy: Concentrate on the application; purchase all "unexciting" infrastructure



All SoC developments of the last few years

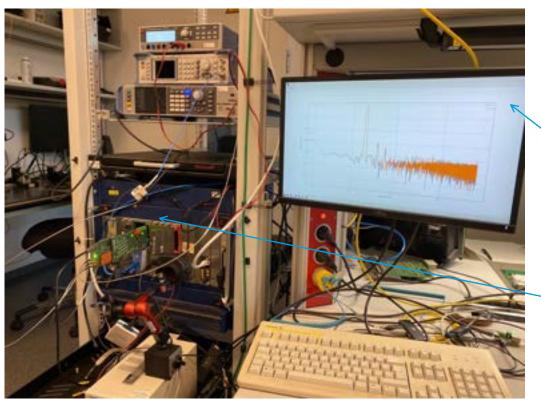
Similarity 1: Boards are all based on DMMC-STAMP



Why MPSoC?

Similarity 2: Processor inside FPGA

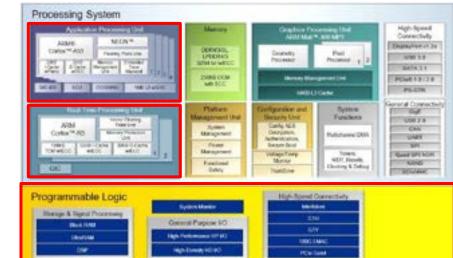
- Everything is SoC-based
- Processor-centric approach ("Raspberry Pi in FPGA")
- Changed development method towards: "on-thefly", "re-use", "modular" and "low-code"
- Keywords: IP modules, Linux, Python



Courtesy of J. Marjanovic and S. Farina

DESY DAMC-FMC2ZUP Board







- DAMC-FMC2ZUP board runs graphical Linux desktop (Displayport)
- Additionally: Web server with Jupyter
- DAMC-FMC2ZUP collects data from FMC-DS500; Output via
 Python Mathplotlib



Processor-centric Platform





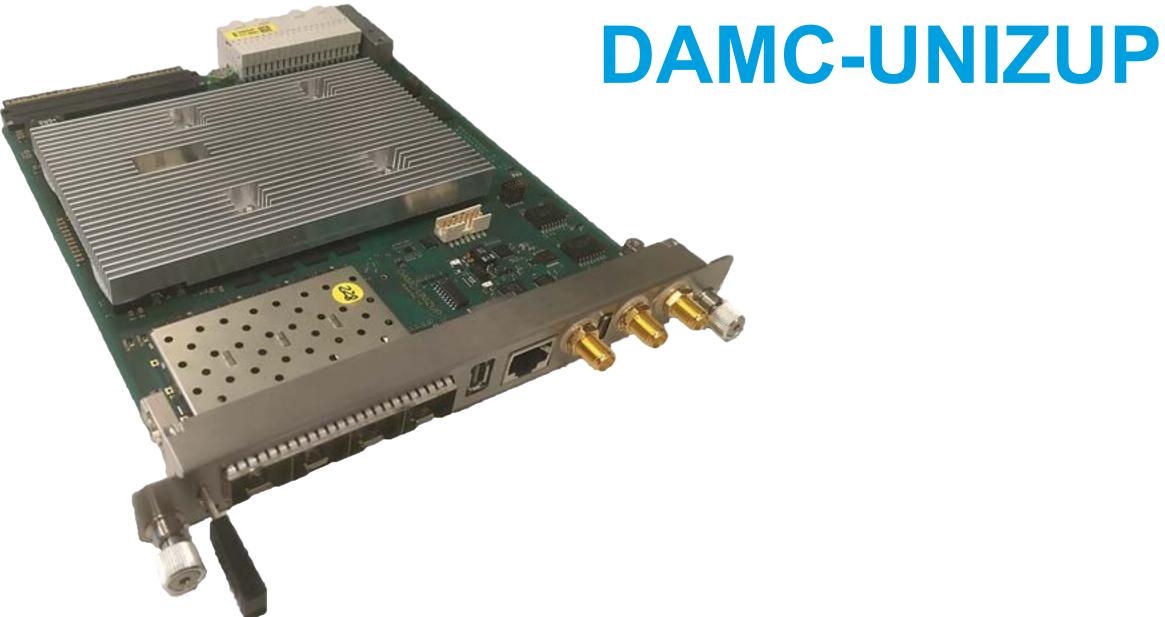
https://www.delock.de/produkt/87297/merkmale.html?g=1107



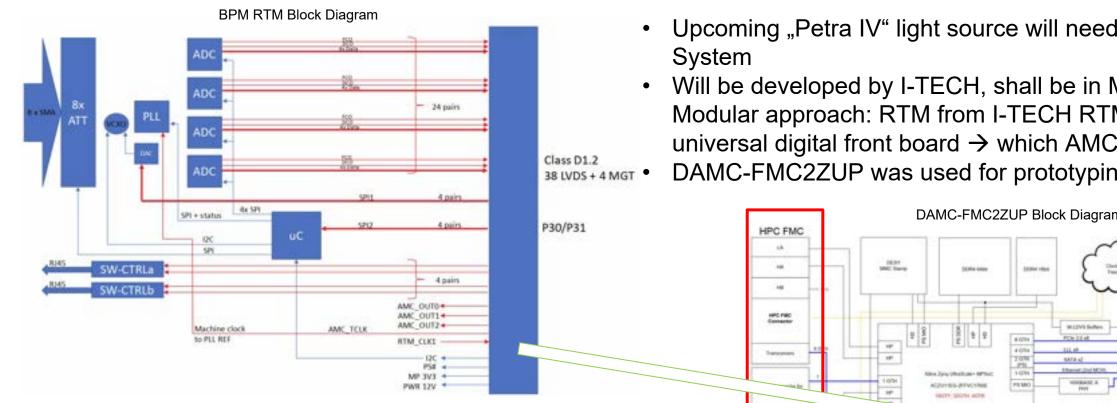
- In the future there will be no more high-end FPGAs without a processor
- Magic is invisible at first glance
- From the outside: Micro-SD slot, USB-C port
- From the inside:
 - "Big" ARM Cortex-A53 processor
 - Dual or quad core CPU up to 1.5GHz per core
 - Board runs Yocto Linux
 - USB-C connection enables complete PC functionality
 - Display via HDMI
 - USB for keyboard, mouse and USB sticks
 - Ethernet connection
 - FPGA can be fully managed processor
- PCle Root complex: Board can replace entire CPU module (depending on computing power requirements)







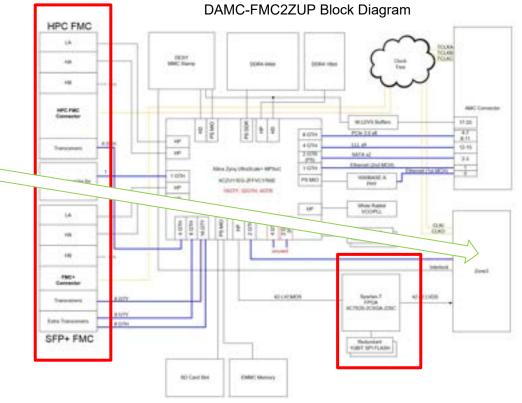
Motivation



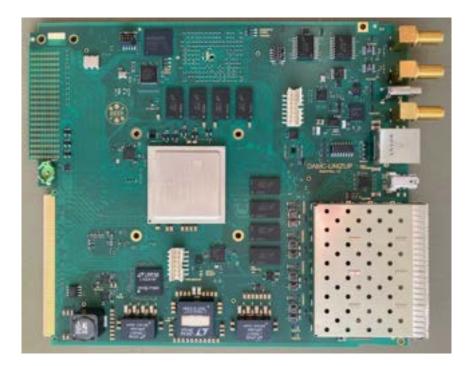
Courtesy of I-Tech

- Dual-FPGA with Spartan-7 based interface is a little overpowered
- FMCs provide flexibility \rightarrow but application needs fixed SFP+ modules instead
- Central FPGA has no direct access to RTM

- Upcoming "Petra IV" light source will need BPM
- Will be developed by I-TECH, shall be in MicroTCA Modular approach: RTM from I-TECH RTM plus universal digital front board \rightarrow which AMC to choose? DAMC-FMC2ZUP was used for prototyping, but...



DAMC-UNIZUP



Inherited features:

Vivado[™] HLS

 Quad-Core ARM Cortex-A53 @1.5 GHz, Dual-Core ARM-R5 RT @600 MHz and Mali-400 MP2 graphics

INSTRUMENTATION

TECHNOLOGIES

- PCle x4 (x8 option on supported systems); Gen.3 supported
- USB type-C Alternate Mode Display Port for standalone operation (no need for additional AMC CPU Module)
- Flexible clocking scheme and front panel connector for external clock input and White Rabbit support
- Supported by all Xilinx development tools (e.g. Vivado HLx)

"Little Sister" of DAMC-FMC2ZUP

- Lower-cost-board with smaller FPGA: hundreds of units will be needed at Petra IV
- 14 instead of 16 layers, 0402 components, (only 0201 capacitors)

Facts

- Board inherits the technology of DAMC-FMC2ZUP
- Universal MPSoC board with high-performance RTM connectivity
- Large FPGA (in smaller package): Zynq Ultrascale+ ZU7CG...ZU11EG

New:

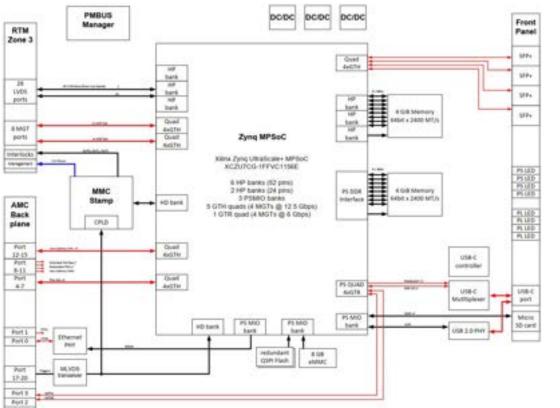
- 2 x 64bit wide DDR4 interfaces (in total 8GiB RAM)
- 4 integrated SFP+ slots with 16.375 Gbps (not 28 Gbps GTY)
- Connectors for "slow trigger" (RS485 for machine protection) and "fast trigger" on Front Panel
- 2 Front panel clock inputs via SMA, 1 Output



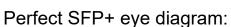
DAMC-UNIZUP

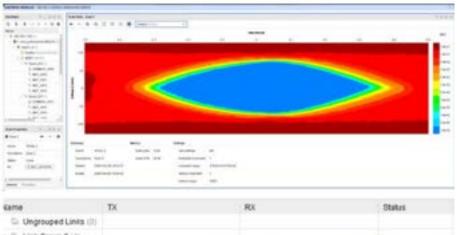
Board was designed specifically for high-bandwidth RTM-Applications

- First 3 prototypes built
- Perfect results in Rev. 1.0, all tests 100% positive, 100% specified performance
- RTM Class D1.2 or D1.3 connectivity to MPSoC (assembly option)
 - D1.2: **38 LVDS** pairs and **4 MGTs** \rightarrow e.g., parallel ADCs on RTM (I-TECH)
 - D1.3: 28 LVDS pairs and 8 MGTs → e.g. serial JESD204B ADCs on RTM



DAMC-UNIZUP Block Diagram



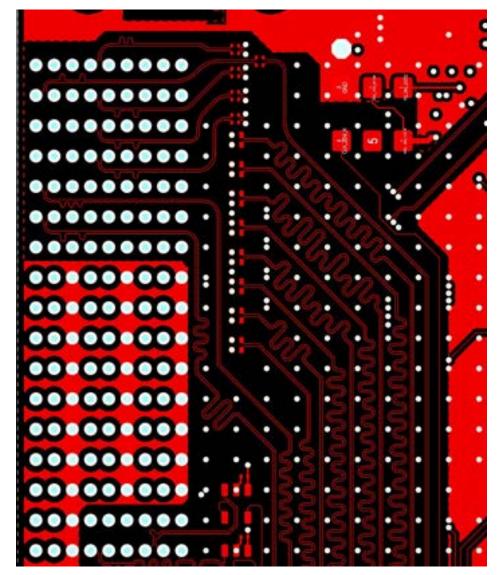


Link Group 0 (4)			
S Link 0	Quad_228MGT_X0Y16TX (x2x11_0) Quad_228MGT_X0Y16RX (x2x11_0)	10.313 Gbps	
% Link f	Quad_228MGT_X0Y17/TX (vcsu11_0) Quad_228MGT_X0Y17/RX (vcsu11_0)	10.313 Gbps	
% Livit 2	Quad_228MGT_X0Y18TX (rcsu11_0) Quad_228MGT_X0Y18RX (rcsu11_0)	10.313 Gops	
% Link3	Quad_228MGT_X0Y19TX (xzu11_0) Quad_228MGT_X0Y19RX (xzu11_0)	10.307 Gbps	

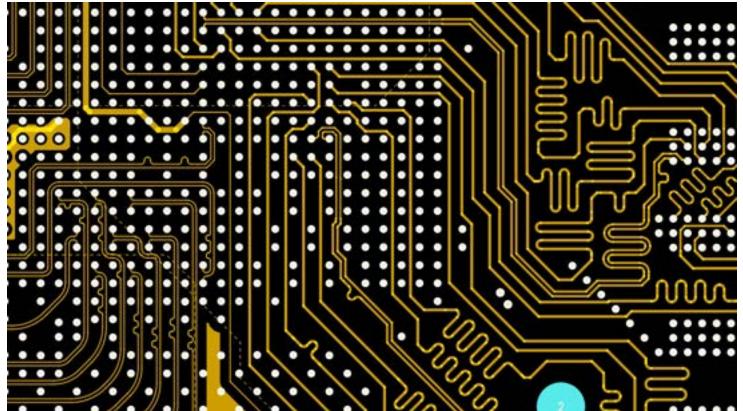


Layout-Details

Nothing is trivial, everything is fast



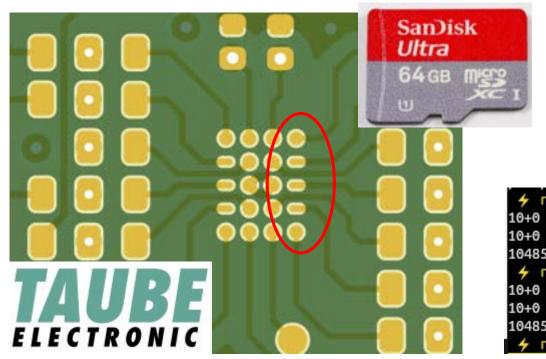
- 14 layers, 2729 components, 10030 pads, 6217 vias, 76216 tracks
- Challenge: "wide" 100µm technology, no HDI (only complete "through" vias)
- LVDS: 1250 Mbps (625 MHz): DDR4: 2666 MT/s (1.3 GHz), Serial Transceivers (MGTs): 16.375 Gbps
- Almost everything in the layout is designed "rounded off"
- 100% length compensation (usually better 1ps / 0.15mm)
- Via in Pads, "GSS-Vias", taking into account the stub length per layer
- Sandwich structure: SIG-GND-SIG-GND ... Power, Power, ... GND, SIG

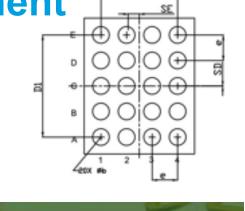


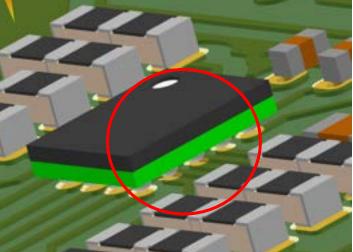
Board was testbed for new Component

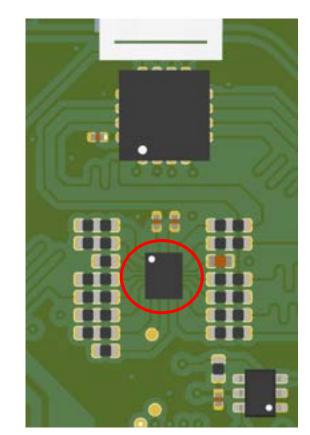
Challenge: PI4ULS3V4857GEAEX SD 3.0 Translator

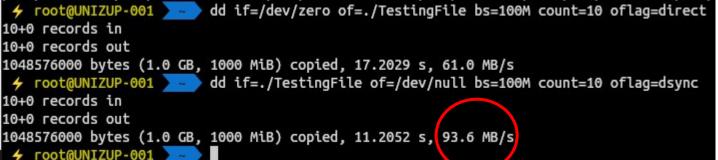
- Bidirectional level converter with variable voltage required (SD3.0)
- BGA pitch: 0.4mm (only "cell phone components" on market)
- Impossible to route in 100um technology (0.8mm pitch required)
- Approach: "Shave the pads" and hope it works
- Reward: 100 Megabytes per second SD card transfer rate (depending on card)
- Common Components strategy: This block will be re-used for all other new boards







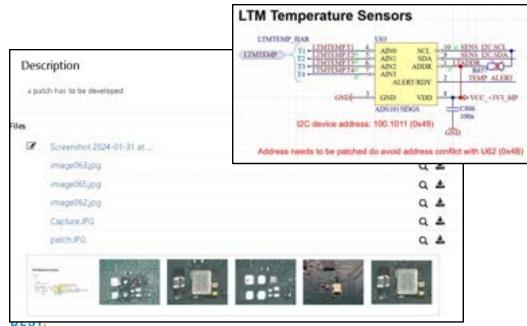




Quality Strategy

What we have achieved...

- Very proud of our team achievements during last years
- All SoC prototype boards achieved 100% functionality and performance in first revision, mostly without any patch wire
- Shared component database (Altium Vault) with 4-eye-checks on each component
- "Common Building Blocks" strategy (all boards share pages)
- "Design Input Review", "Design Output Review"
- 100% Issue tracking in Redmine (we track "everything")
- Complete patch documentation in schematics (only a few....)
- All design data storage with git
- DESY has it's own on-premise *gitlab* server



Estimated time: 0.00 Spent time: 0.00

Estimated	time: 0.00 Spent time: 0.00	2					
	- TRACKER	STATUS	PRIORITY	SUBJECT	ASSIGNEE	UPDATED	PROJECT
130	7 Bug	New	Normal	Front Panel: Lightpipes du not fit into holes		2024-04-04 14:59	DAMC-UNIZUP
129	18 Improvement	New	Normal	Fast trigger connector should be moved		2024-03-22 19:02	DAMC-UNIZUP
0 129	17 Improvement	New	Normal	Fron Panel, Fast Trigger hole is not shaped nicely		2024-04-04 15:00	DAMC-UNIZUP
129	16 Bug	New -	Normal	SMA connectors are mounted too collie to front.	2	2024-03-22 19:00	DAMC-UNI20/P
0 1297	15 Bug	New	Normal	Front Panel: SMA holes are too small		2024-04-04 15:00	DAMC-UNIZUF
1218	io Bug	New	Normal	SELTCUKABRYM must not be push-pull driven		2024-03-14 18:54	DAMC-UNI20.P
0.129	9 Improvement	New	Normal	Front Pannel can be improved		2024-03-14 1848	DAMC-UNIZ6#
0 1254	Bug Dug	New	Normal	SMA connectives too close to front panel		2024-03-14 14:14	DAMC-UNIZUP
0,129	5 Improvement	New	Normal	Increase eMMC from BGE to 1608		2024-03-08 17:01	DAMC-UNIZUP
129	3 Improvement	New	Normal	Review USB capacitors		2024-03-08 11:09	DAMC-UNDUP
D 1290	3 Bug	New	Normal	Board temperature sensors in wrong place		2024-03-06 17:04	DAMC-UNIZUP
128	ka Improvement	New	Normal	Type in Schematics on page 24		2024-03-05 17:11	DAMC-UNIZUP
128	8 Implementation	New	Normal	SD2.0 Translator can be set to DNP in Nev. 2.0		2024-03-01 1857	DAMC-UNIZUP
0 128	rt Bug	New	Normal	Wrong net names on Zone 3 OUT buffer		2024-02-28 19:28	DAMC-UNIZUP
□ 12E	5 Implementation	New	Normal	LTCHISTIMS-2 IN EQL		2024-02-28 16:32	DAMC-UNIZUP
128	a improvement	New	Normal	SV Power increase request		2024-02-23 22:43	DAMC-UNIZUP
128	S7 Bug	New	Normal	Power witchoff with Certain USB-C docks		2024-02-23 22:22	DAMC-UNIZUP
128	9 Improvement	New	Normal	Better P/N maldring on DDR4 Detectrobe		2024-02-23 22:23	DAMC-UNIZUP
128	16 Improvement	New	Normal	Batter PMBUS connective location requested.		2024-02-23 22:44	DAMC-UNIZOP
128	ts Improvement	New	Normal	SD Butter to opprive improvement for mass pro-		2024-02-23 22:23	DAMC-UNIZUP
D 128	I Improvement	New.	Normal	DESY Logo is partially covered by Neabirk		2024-02-21 10:37	DAMC-UNIZUP
128	2 Improvement	New	Normal	10k PU ive SD Card DAT3 line		2024-02-23 22:44	DAMC-UNIZUP
0 127	i9 Bug	New .	Normal	Unwanted SD card power injection		2024-02-23 2245	DAMC-UNIZUF
127	ile Bug	New	Normal	SDQ.0 boot mode is not supported		2024-02-16 22:05	DAMC-UNIZUP
0.127	87 Improvement	New	Normal	SerDes Ethernet Lanes need P/N matching		2024-02-13-09-48	DAMC-UNIZOP



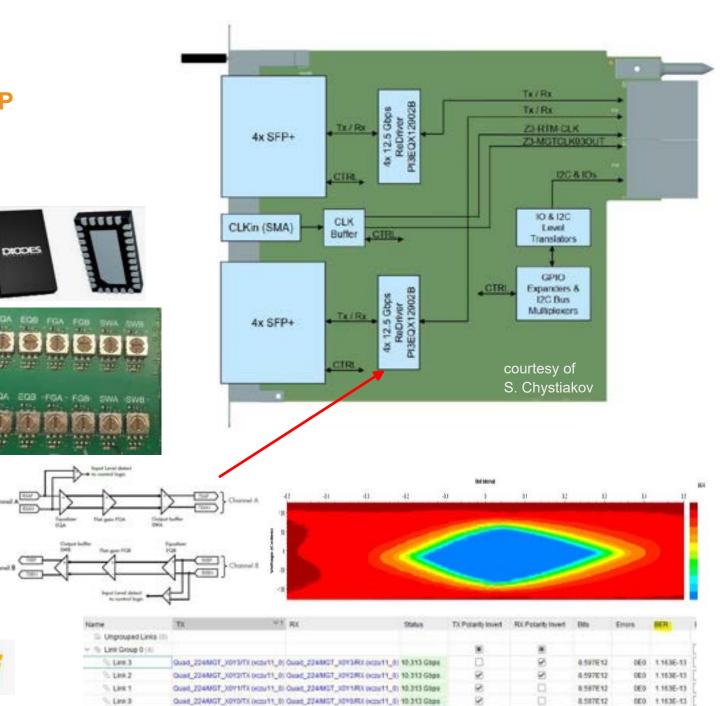
DRTM-8SFP+

DAMC-8SFP+

Fan-out of MGT Channels from DAMC-UNIZUP

- We needed to verify UNIZUPs 8 MGTs to RTM
- We designed a 8-SFP+ RTM
- Board works on all other Digital Class AMCs
- Brings 1 to 8 MGTs to RTM **12.5 Gbps**: not trivial
- First use of "analog" equalizer
- Development time: 3 months
- Low-cost circuit board and components
- Manufactured in the "**PCB pool**" from Leiton (Berlin)
- Material: Panasonic R-1566W (Dk=0.010 !!!)



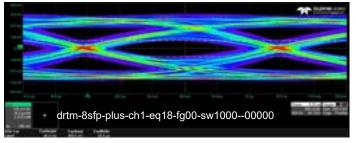


Improving of signal integrity by using a Re-Driver

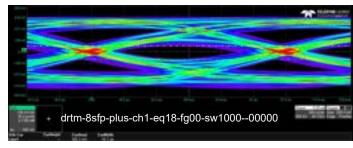
First use of an analog equalizer

- Super critical RTM MGT routing on DAMC-UNIZUP
- 10.315 Gbps (up to 12.5 Gbps)
- Bad channel:
 - two 0-ohm bridges
 - Erni connector
- "Warning: it doesn't work" but it does, *if you do it right...*

Good channel: 5 GHz: +6.6dB



Bad channel: 5 GHz: +6.6dB

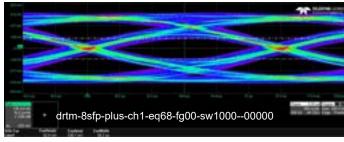


PI3EQX12902B: 4 Configurations possible

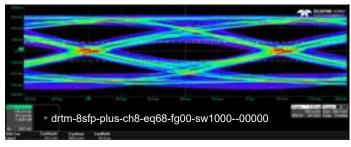
1	Equalizer setting (dB)							
	@2.5GH;	@3GH:	@4GH:	@5GH:	@6GH:			
	1.8	2.6	4.5	6.6	8.9			
2	3.7	4.7	6,7	9.4	11.7 (Definit)			
3	.5.1	6.3	8.7	11.2	13.5			
1	6.8	8.2	10.8	13.2	15.3			

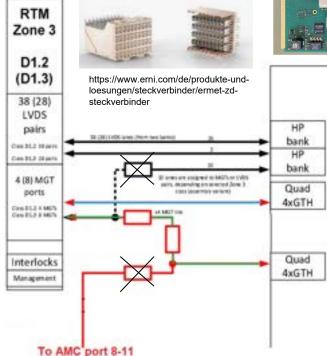
DAMC-UNIZUP RTM Class D1.3 verification successful!

Good channel: 5 GHz: +13.2dB

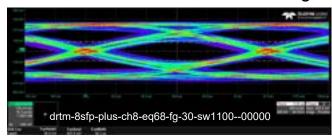


Bad channel: 5 GHz: +13.2dB





Bad channel, 13.2dB, 1100mV Level, -3.0dB "flat gain"

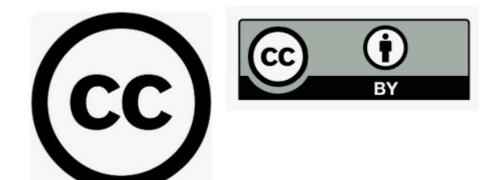




We invite everybody to be part of the MicroTCA ecosystem

What we can offer...

Creative Commons License







MicroTCA.4 Template

Community Support

Idea: Jump-Start with MicroTCA as you would with any other board

Fully MicroTCA compliant "empty" board

- Already "fully functional"
- Start with correct mechanical shape
- AMC and RTM "only" get power
- All the management is done on DMMC-STAMP

Purpose: facilitate development

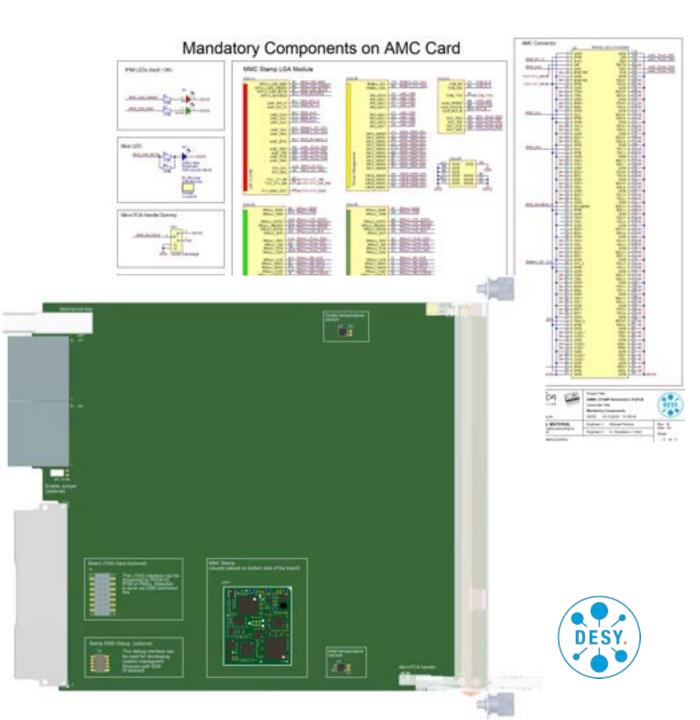
- Allows design migration (e.g. from VME)
- Source design files (Altium Designer) are provided
 - Schematics

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

• PCB

Components:

- MMC SoM, LEDs, Connectors, Temperature Sensors
- USB Interface for management and status



RTM Template Community Support

DESY MicroTCA.4 RTM Implementation Proposa Preview. Do not distribute Raiar page Attions Decemptor Internet Vermalinete 300 000 Charige Lief ingle-ended IO expport. Javoid, if possi HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

- We also provide a RTM Template
- Complete guide and "empty board" for own MTCA RTM designs → Altium Designer Template
- MTCA Standard leaves freedom for RTM interface implementation (vendorspecific) → risk of non-interchangeable AMC-RTM pairs
- DESY has a "class concept" → Interchangeable boards
- DESY collected and documented best design practices beyond the standard



Tools: MicroTCA Bring-up Adapter

Community Support





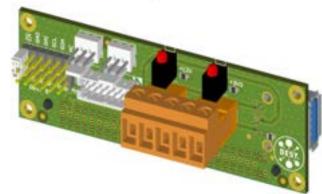
https://rk.edu.pl/en/risers-and-adapters-non-standard-gpu-connection/



Bottom view

Top view





- Allows to connect power and PCIe to boards on the bench
- Mechanically compatible with RTMs
- PCIe option allows operate a MTCA board "inside a PC"

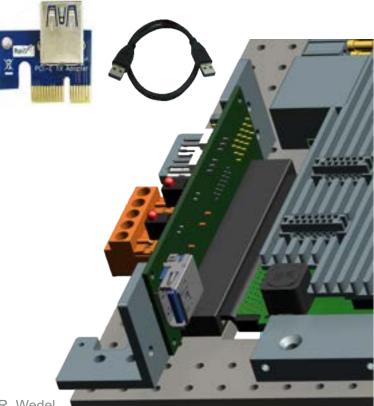


Typical Lab bring-up Setup



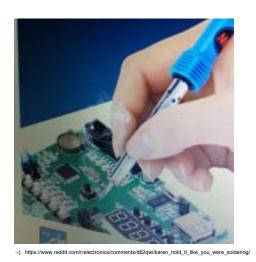
- Flexible and handy development tools
- DESY provides them (Creative Commons)
 - bring-up PCB production files
 - Aluminium frame production files

Write an email to me if you are interested in these designs.



HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

Thank you!



Contact

www.desy.de

DESY. Deutsches Elektronen-Synchrotron

Michael Fenner MSK michael.fenner@desy.de +49 (0) 40-8998-1885

Backup





DMMC-STAMP

System on Module (SoM)

- 25.5 x 29.5 x 2.3 mm
 Pre-programmed firmware
- Evaluation board available (BoB)

Software Development Kit (SDK)

MMC firmware customization

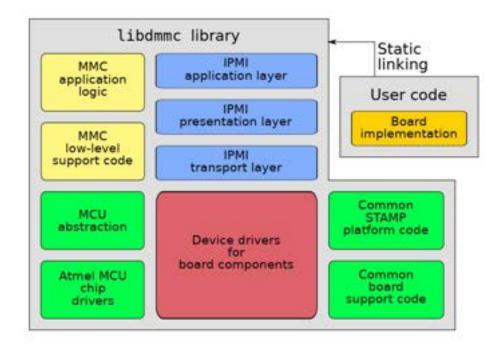
- DESY MMC Software Library (libdmmc)
- Example implementations (BoB, DAMC-FMC2ZUP)

Open Source Tools and Templates

- AMC and RTM Altium Designer Templates
- mmcterm: serial over IPMB
- bin2hpm: create HPM files for IPMI upgrade
- frugy: read and write FRUs
- cpld-img-tools: bitstream conversion for Lattice CPLDs



Post-Production test of DMMC-STAMP



Courtesy of Patrick Huesmann

DMMC-STAMP BoB (Break-out-Board)







