Libera

Preliminary results from a wide-band 500MSps digitizer prototype

Manuel Cargnelutti, Libera Workshop, 17/05/2018

Outline

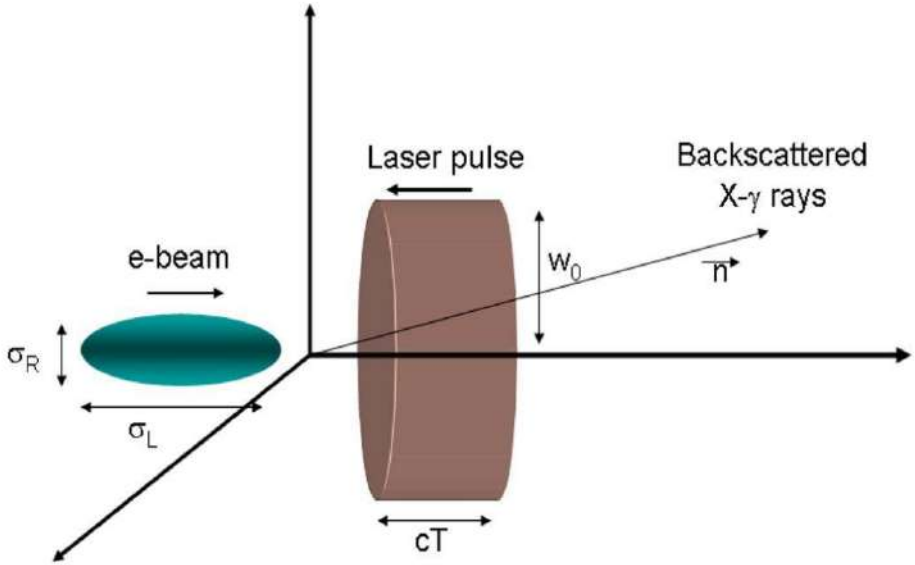
- Motivation and Target specifications
- First results from the front-end prototype
- Next steps and timeline

2017: CavityBPM project

- ELI-NP: Compton back-scattering source

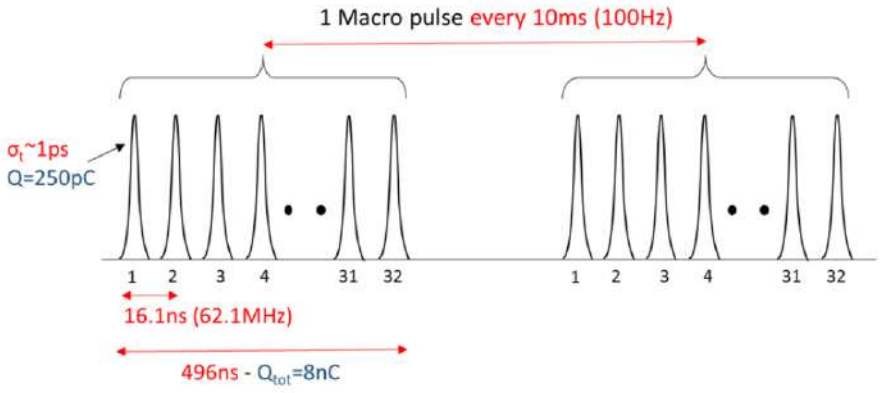
Magurele - Romania

Compton back-scattering → γ beam



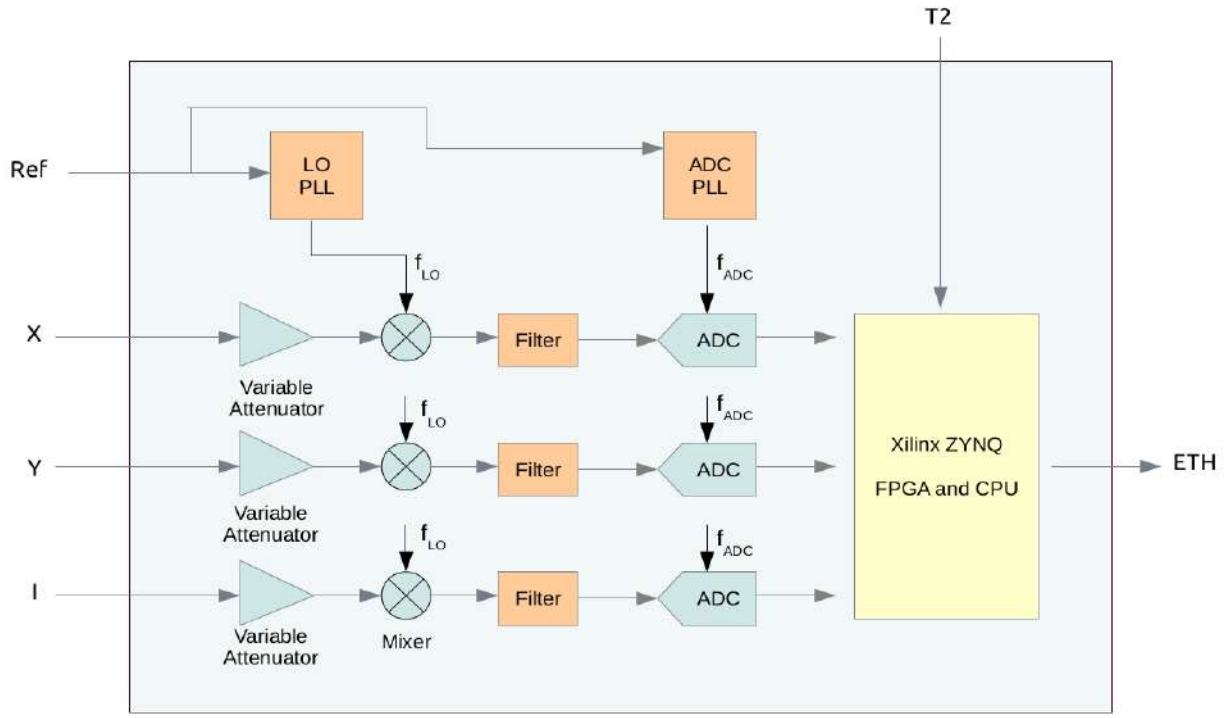
2017: CavityBPM project

- Need to measure bunch-by-bunch beam position at the IP
  - → Low-Q Cavity BPM pickup (PSI-BPM16)
  - → Fast and accurate electronics

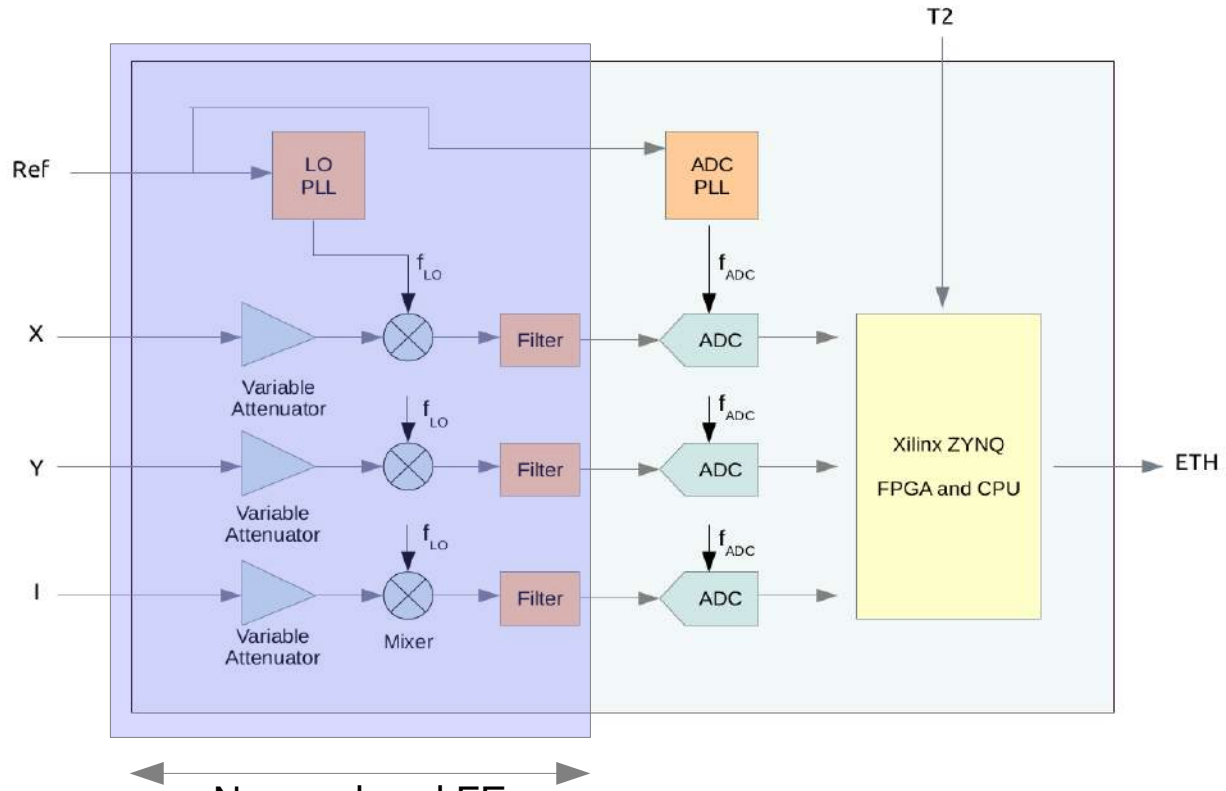


Libera CavityBPM

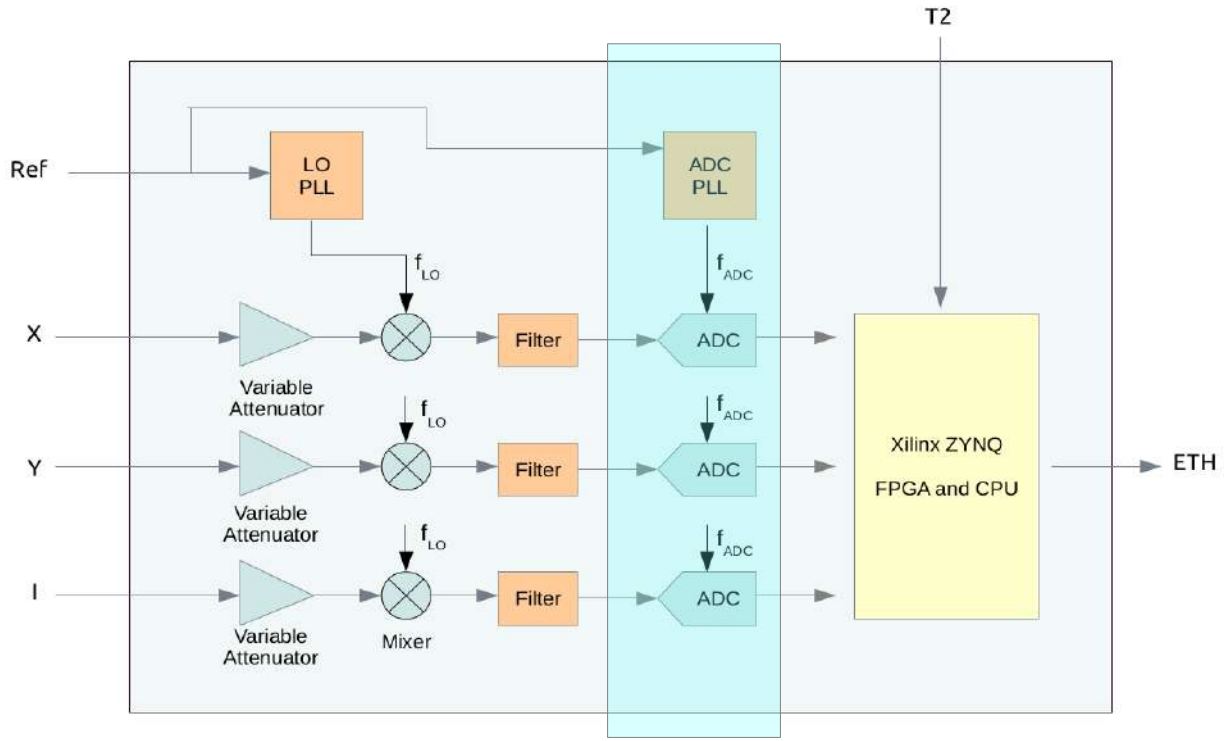
Libera CavityBPM architecture



Libera CavityBPM architecture

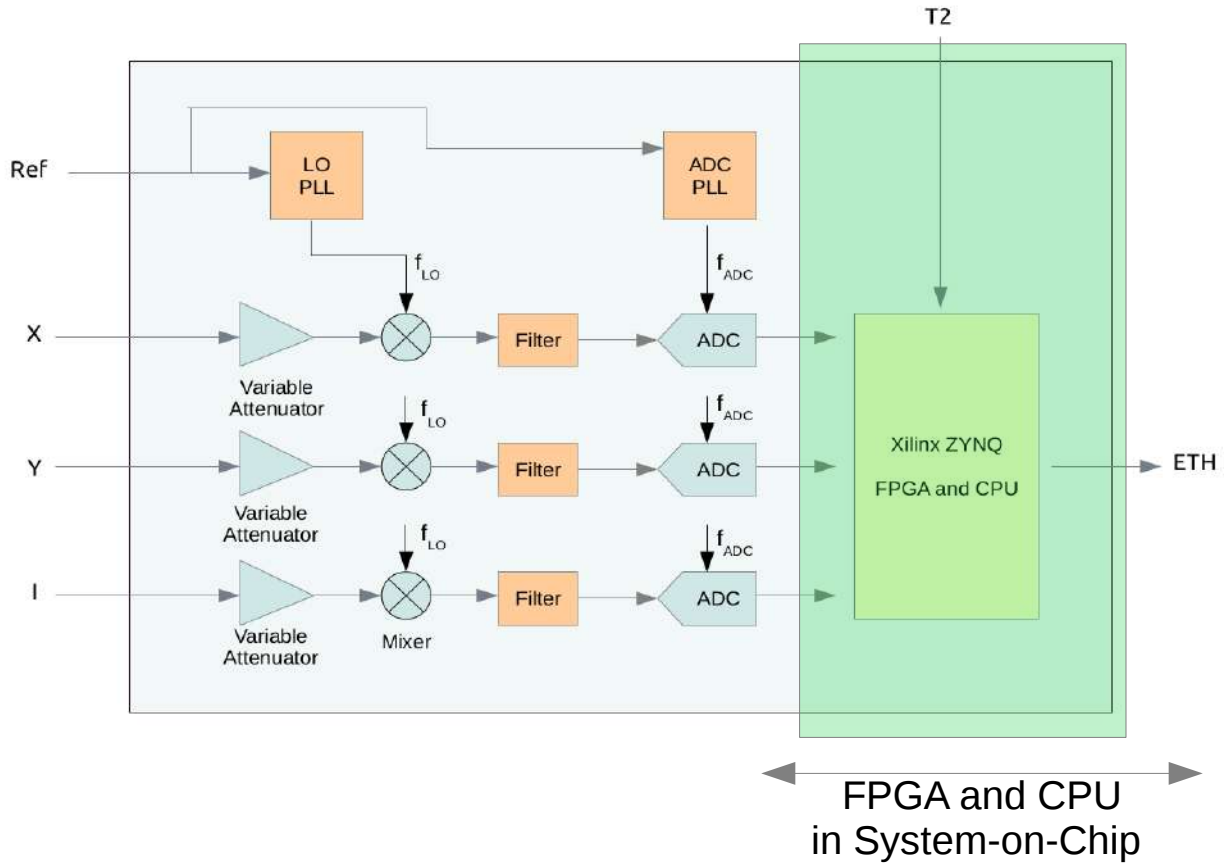


Libera CavityBPM architecture

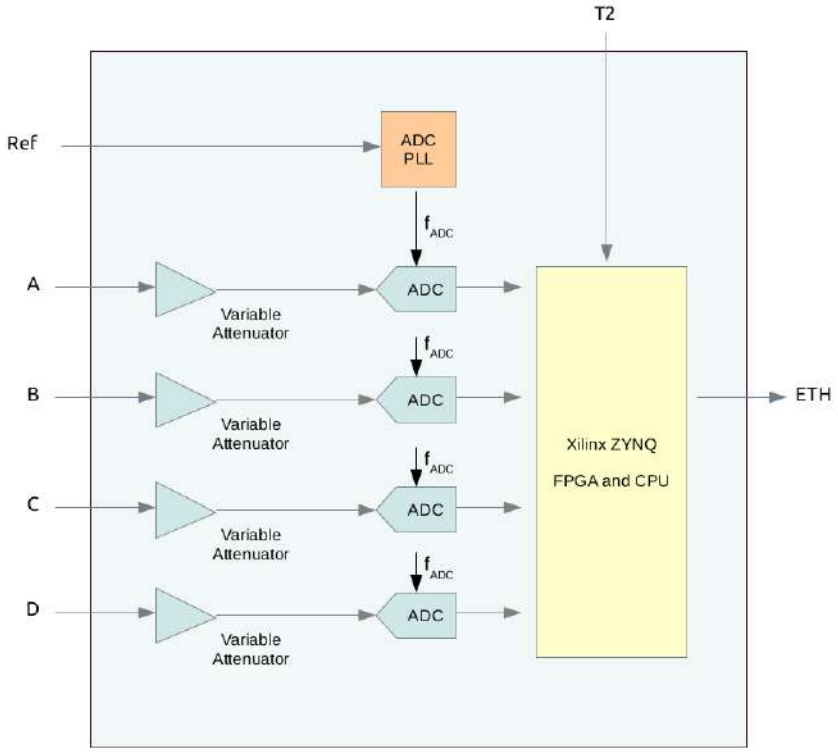


500MSps – 14 bit ADCs
Locked to external Reference

Libera CavityBPM architecture



Digitizer Block scheme



Design goals:

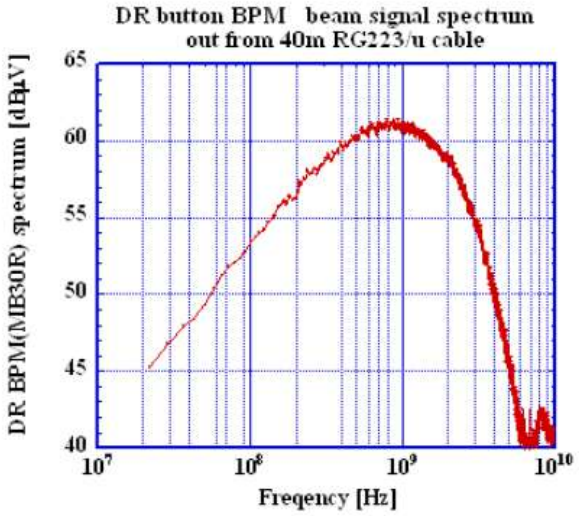
- Wide-band front-end as versatile as possible. Only SW controlled attenuators and amplifiers.
- ADC and FPGA clocks derived from a HW PLL locked to the external reference signal (up to 250MHz)
- DDR3 memory with storage capability of 500MS of ADC data per channel
- SoC Platform advantages: passive cooling, no fans, temperature stability.

Target specifications

Parameter	Target Specification
N of channels	4
ADC sampling rate - bits	500MSps – 14 bit
PLL locking	Up to 250MHz (500MHz with divider)
Variable attenuation	0-32dB, SW controlled
Input impedance	50Ohm
Bandwidth	DC - 2GHz
Memory	Segmentable 500MS/channel
FPGA	Xilinx ZYNQ 7035
Supply/Cooling	PoE / Passive

Possible use-cases

- Bunch-by-Bunch BPM
  - the wide-band front-end enables the user to measure the BPM signal properties at different Nyquist zones
  - control of the ADC sampling phase through the external reference, enables to sample each bunch on its top
  - Bunch-by-bunch position and charge



Should still be able to process data at lower rates (Turn-by-Turn, FA, SA)
Potentially compatible with the pilot-tone front-end.

Possible use-cases

- Bunch-by-Bunch BLM (recent idea from discussions at LBNL)

Requires a Beam Loss Detector fast enough not to generate pile-up between different bunches!

Possible use-cases

- Readout from Current transformers
- Readout from Magnet power supplies
- Readout from phase probes
- Digitizer for 15GHz cavity BPMs

Outline

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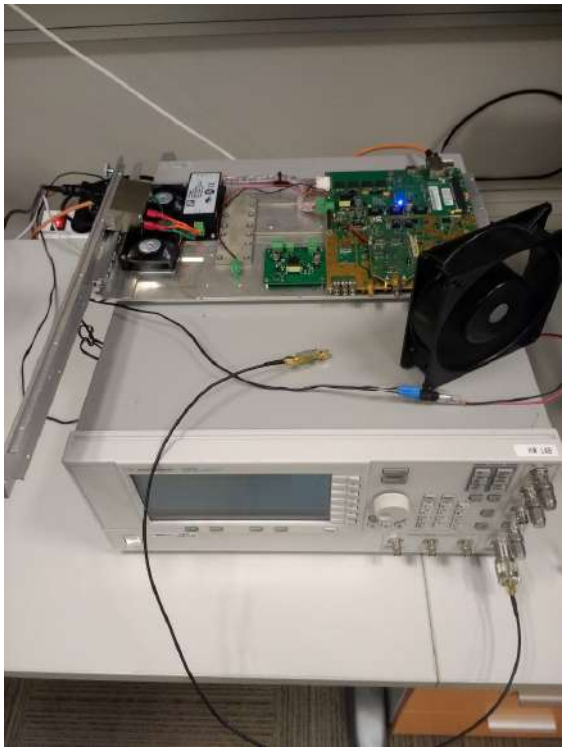
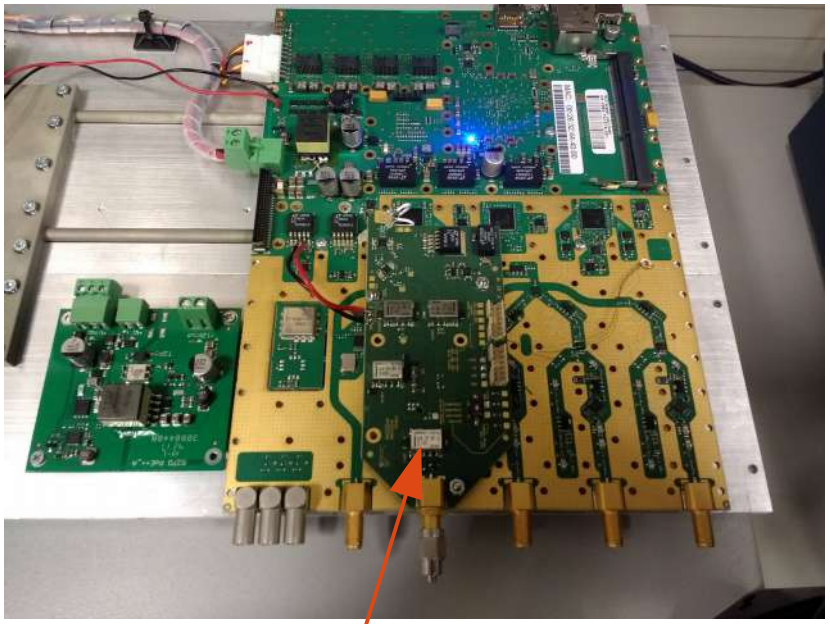
The prototype (I)

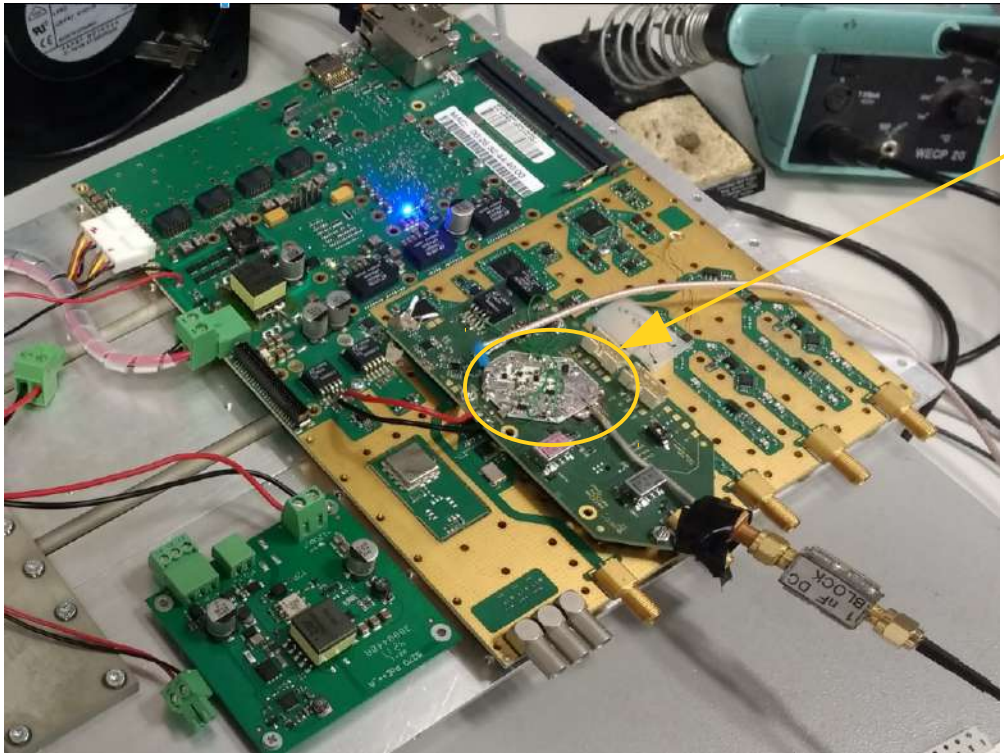
- Libera CavityBPM with new front-end attached





Front-end prototype:
- 1 channel board mounted on top of the CavityBPM PCB.
- Connection to the ADC with coaxial cable

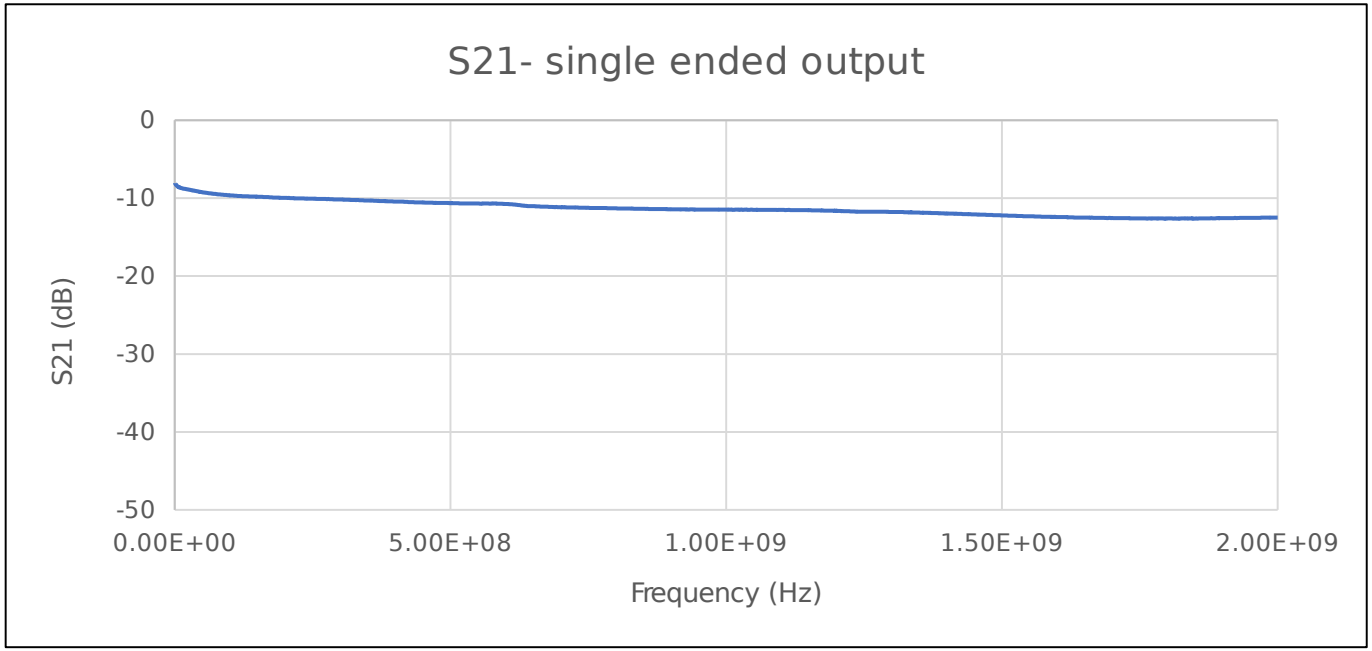
The prototype (II) – improving DC characteristic



Front-end extension:

- Additional buffer stage to match the DC input impedance to 50Ohm

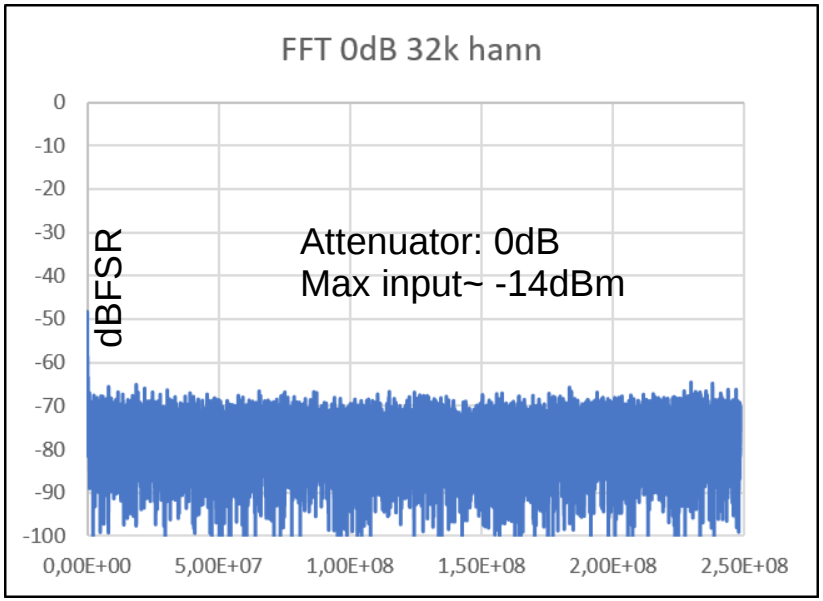
Front-end transfer function |S21|

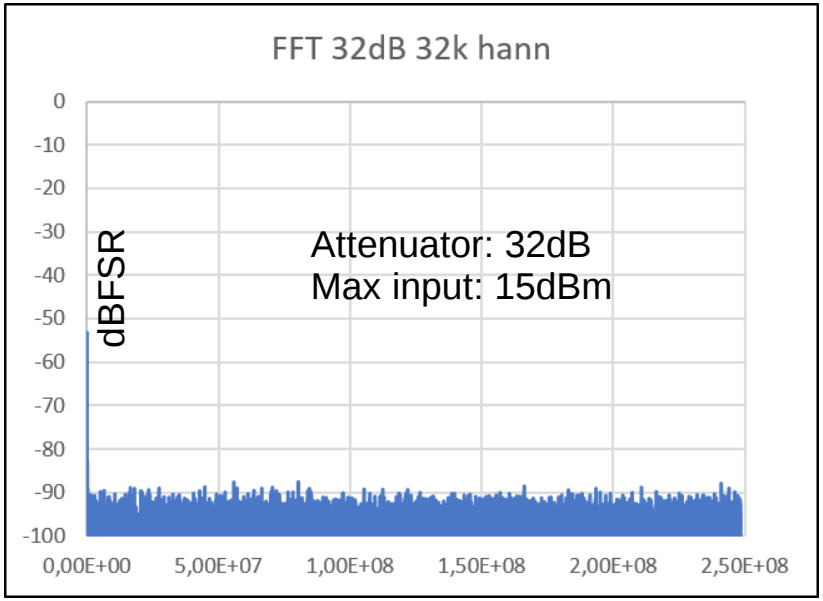


- Measurement from 300kHz (VNA lower limit) to 2GHz
- Flat and uniform characteristics
- Measured on one of the differential amplifier outputs

AC input impedance: 50Ohm

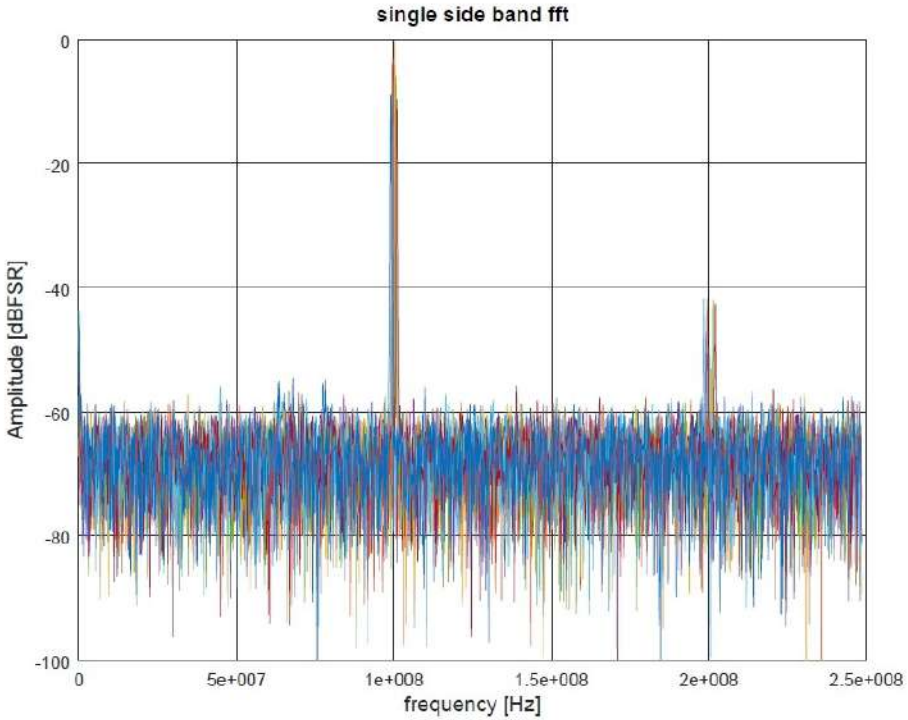
Noise floor





- Measurement in the first Nyquist zone [0-250MHz]
- Input was 50Ohm terminated
- Amplitudes are expressed with reference to the ADC input full-scale

Frequency down-conversion

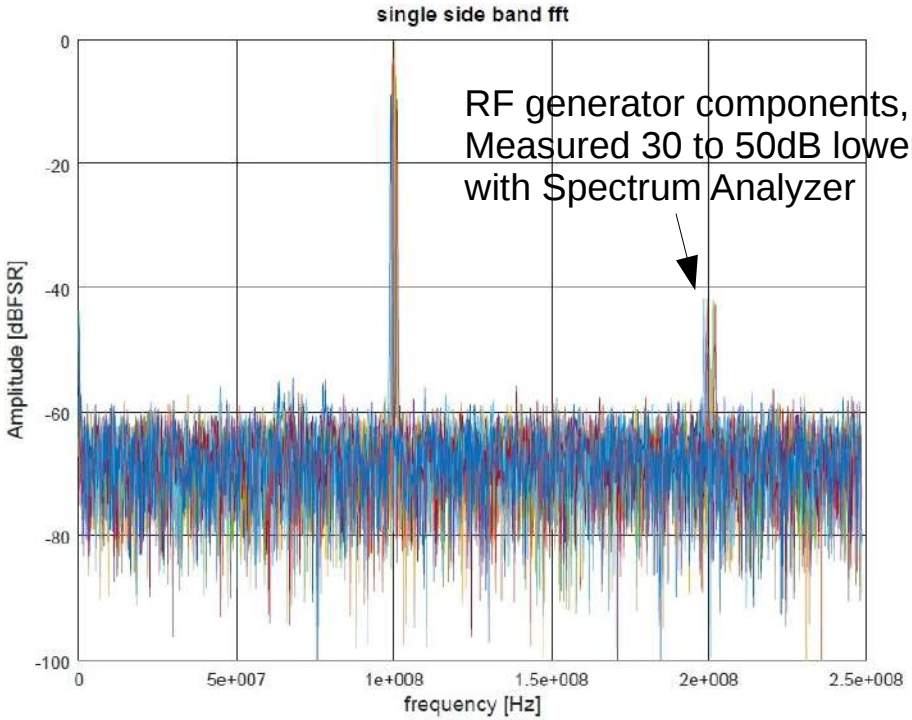


- Internal attenuator: 0dB
- Input signal power: -20dBm
- ADC sampling: 497MHz

- Input signal frequencies chosen to down-convert roughly at the same frequency (100MHz):

  100 MHz
  397 MHz
  597 MHz
  894 MHz
  1094 MHz
  1391 MHz
  1591 MHz
  1888 MHz

Frequency down-conversion



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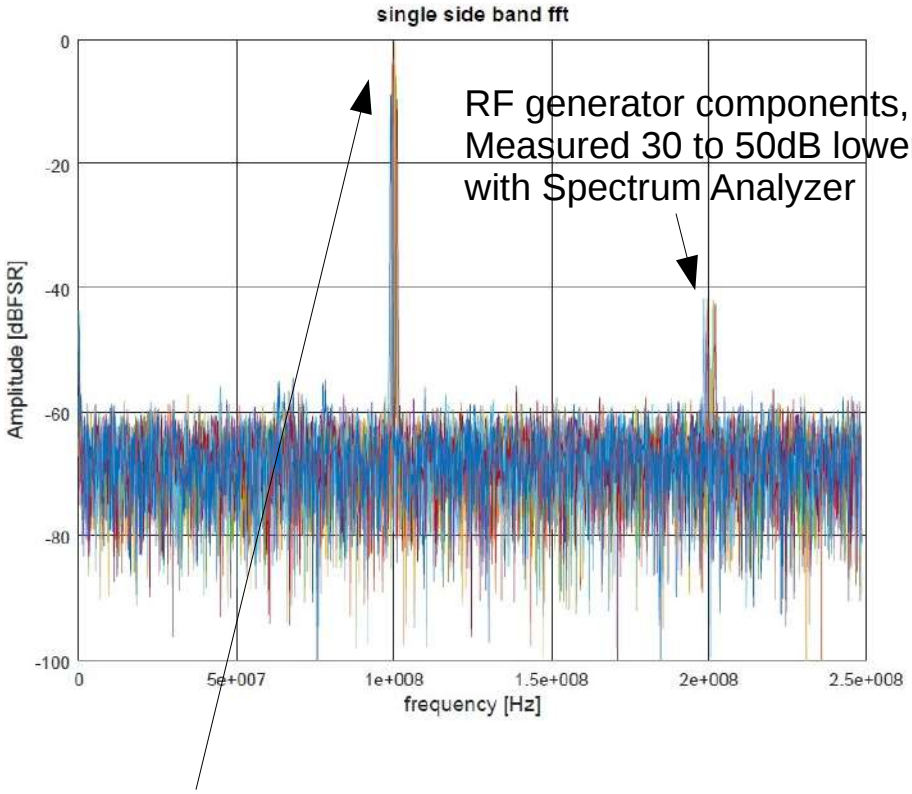

Deviations in amplitude among different frequency components are mostly caused by the cable connecting the front-end to the CavityBPM board

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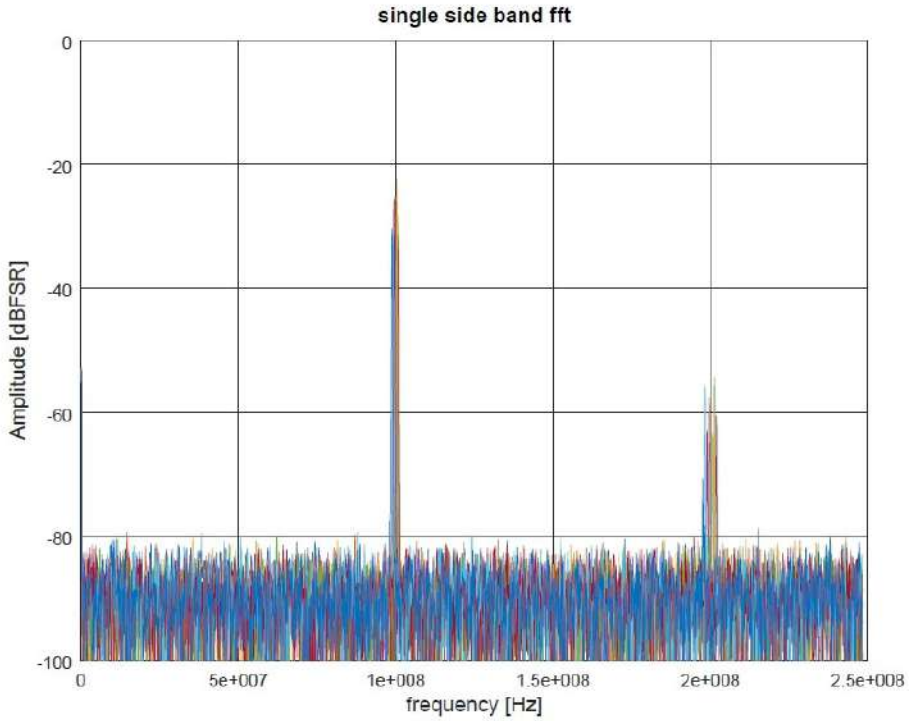
Frequency down-conversion (II)



- Internal attenuator: 32dB
- Input signal power: -10dBm
- ADC sampling: 497MHz

- Input signal frequencies chosen to down-convert roughly at the same frequency (100MHz):

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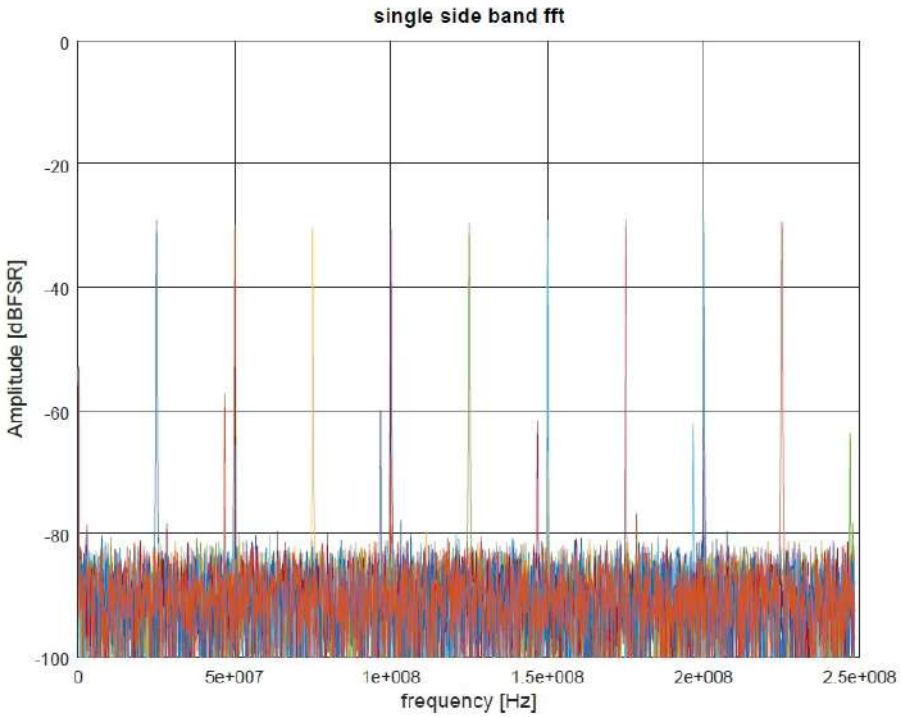
  1391 MHz
  1591 MHz
  1888 MHz

Frequency sweep (I) – 1st Nyquist zone

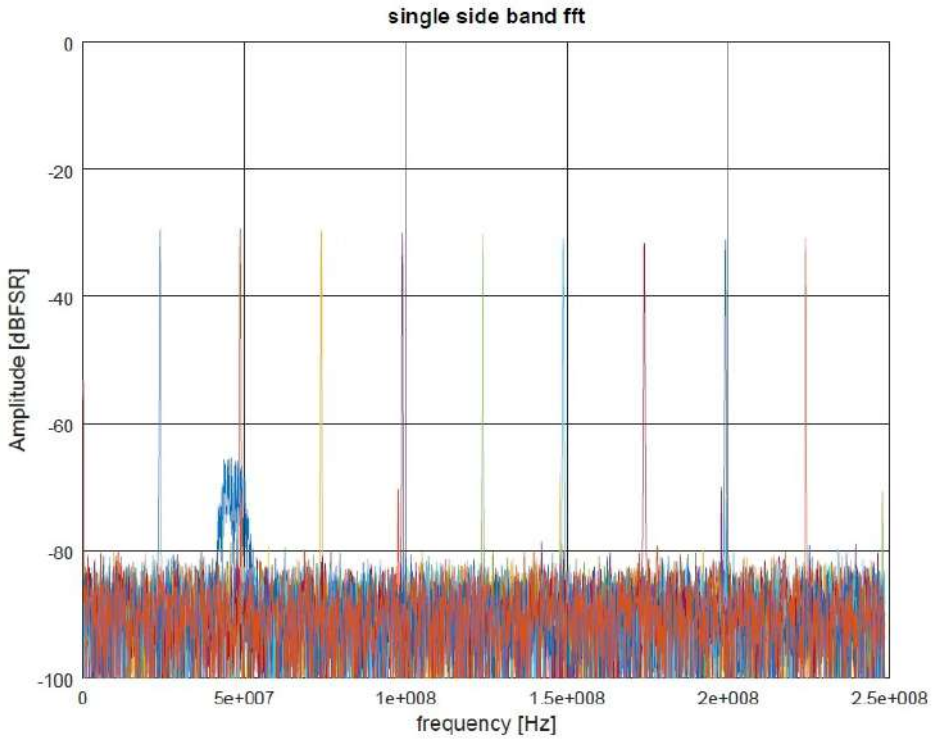


- Input signal power: -10dBm
- Internal attenuator: 32dB
- ADC sampling: 497MHz

- Input frequencies in the 1st Nyquist zone:

  25 MHz
  50 MHz
  75 MHz
  100 MHz
  125 MHz
  150 MHz
  175 MHz
  200 MHz
  225MHz

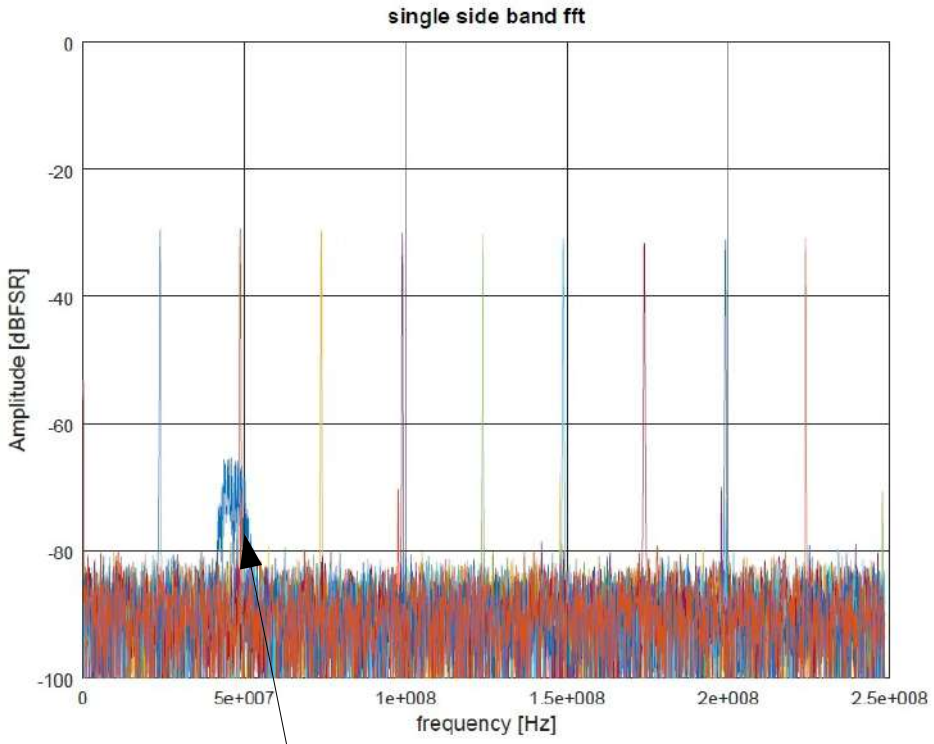
Frequency sweep (II) – 8th Nyquist zone



- Input signal power: -10dBm
- Internal attenuator: 32dB
- ADC sampling: 497MHz

- Same analysis done on the 8th Nyquist zone in steps of 25MHz:
  - 1763 MHz
  - 1788 MHz
  - 1813 MHz
  - 1838 MHz
  - 1863 MHz
  - 1888 MHz
  - 1913 MHz
  - 1938 MHz
  - 1963 MHz

Frequency sweep (II) – 8th Nyquist zone



External disturbance appeared in one measurement

- Input signal power: -10dBm
- Internal attenuator: 32dB
- ADC sampling: 497MHz

- Same analysis done on the 8th Nyquist zone in steps of 25MHz:
  - 1763 MHz
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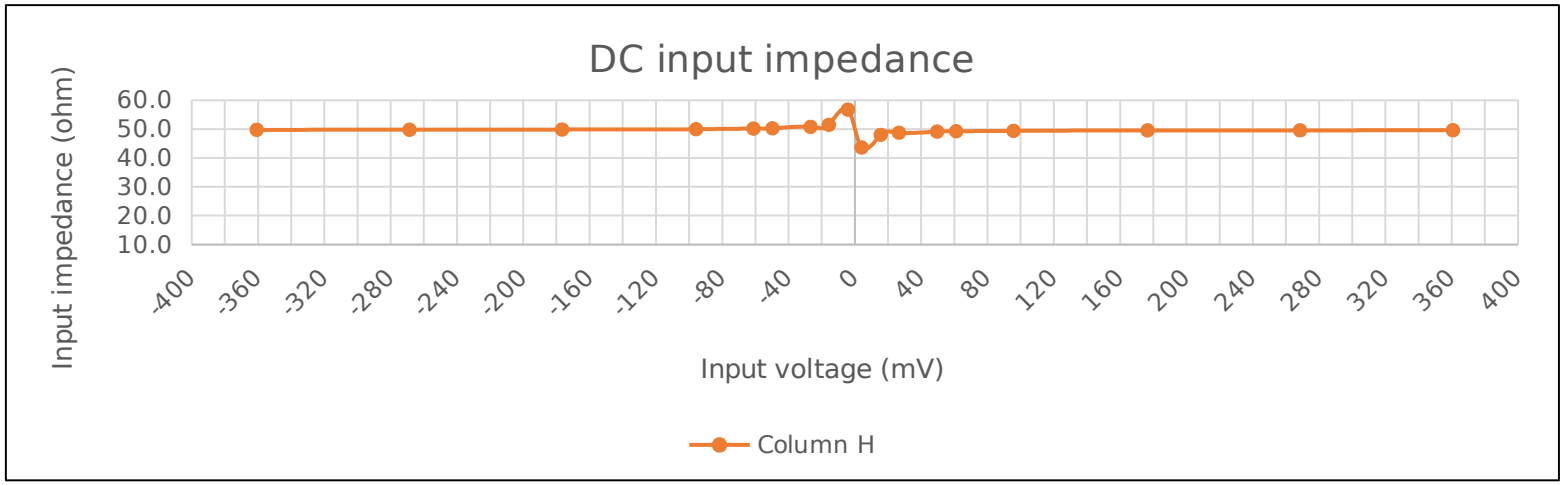
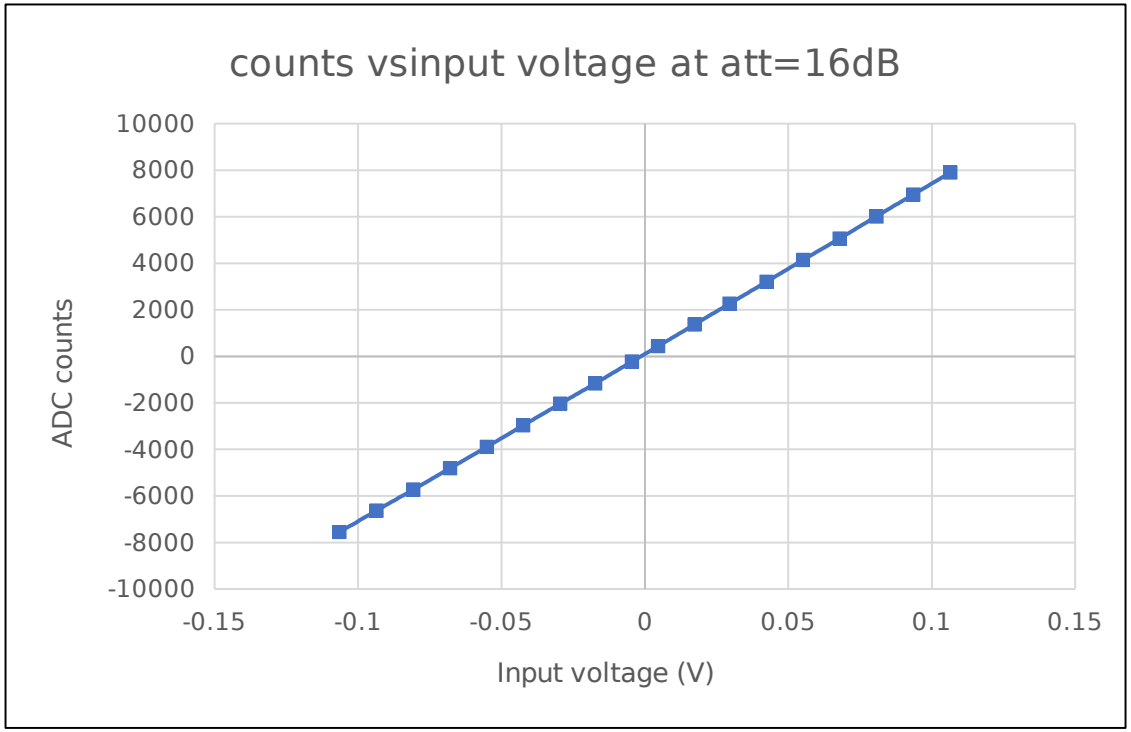
DC characteristics: input impedance



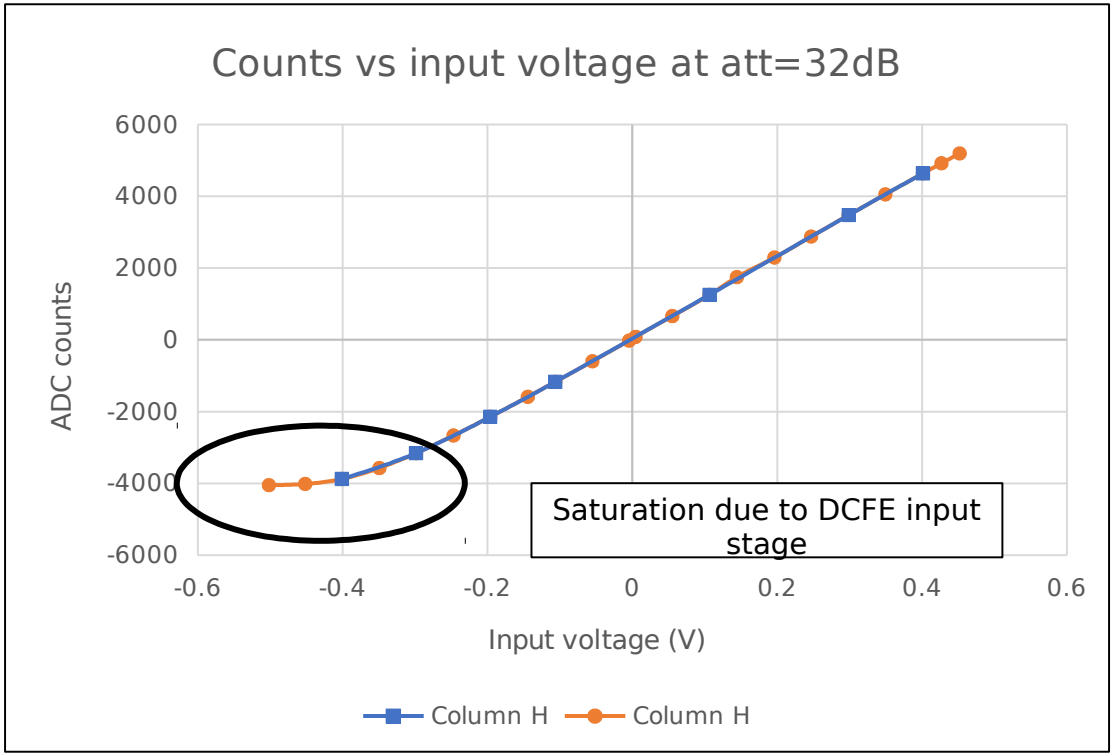
- Stable 50Ohm impedance was the goal of the additional stage on top of the prototype. Old one had variable DC impedance.

DC characteristic (I)



- Linear DC characteristic with 16dB internal attenuation.
- Decreasing the internal attenuation would make the instrument very sensitive

DC characteristic (II)



- Linear DC characteristic with 16dB internal attenuation.
- Decreasing the internal attenuation would make the instrument very sensitive
- Increasing attenuation to 32dB does not increase the input DC range due to analog saturation and upper limits defined by the bias voltages.

Outline

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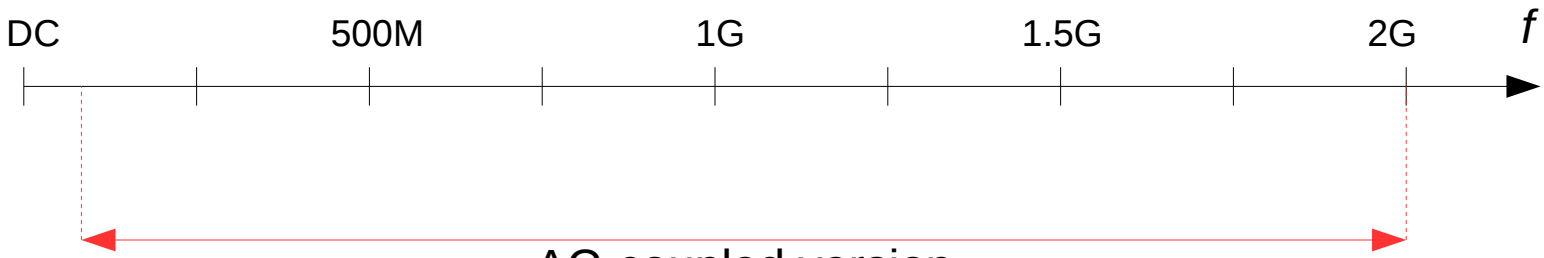
Observations

- Achieving good DC characteristics and wide flat bandwidth at the same time is a challenge.
- This prototype was stretched to achieve both but at the expenses of more complexity (additional FE stage) and need of tuning
- Same AC behavior was achieved with previous prototype
- DC Characteristics are probably sensitive to component tolerances
- No application requires both DC measurements and wide bandwidth

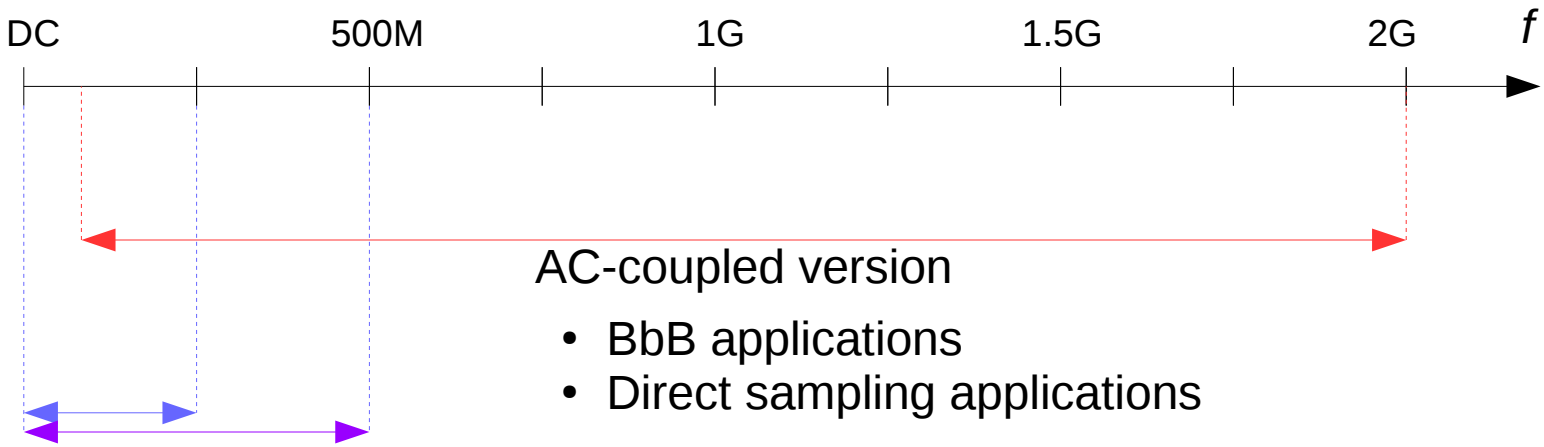
Plan: 2 board versions



AC-coupled version

- BbB applications
- Direct sampling applications

Plan: 2 board versions



AC-coupled version

- BbB applications
- Direct sampling applications

Possible DC-coupled versions

- Time domain analysis

Timeline

- Today: AC version is confirmed, will be produced in regular PCB
- Mid 2018: DC version will be conceptualized
- Late 2018: AC version development is finished
- 2019: First measurements with beam in 2019 in different laboratories
- Late 2019: finalization of the Bunch-by-Bunch BPM concept

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Thanks for your attention!