Libera

Libera Photon 2016

Peter Leban, June 9, 2016

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History and Motivation

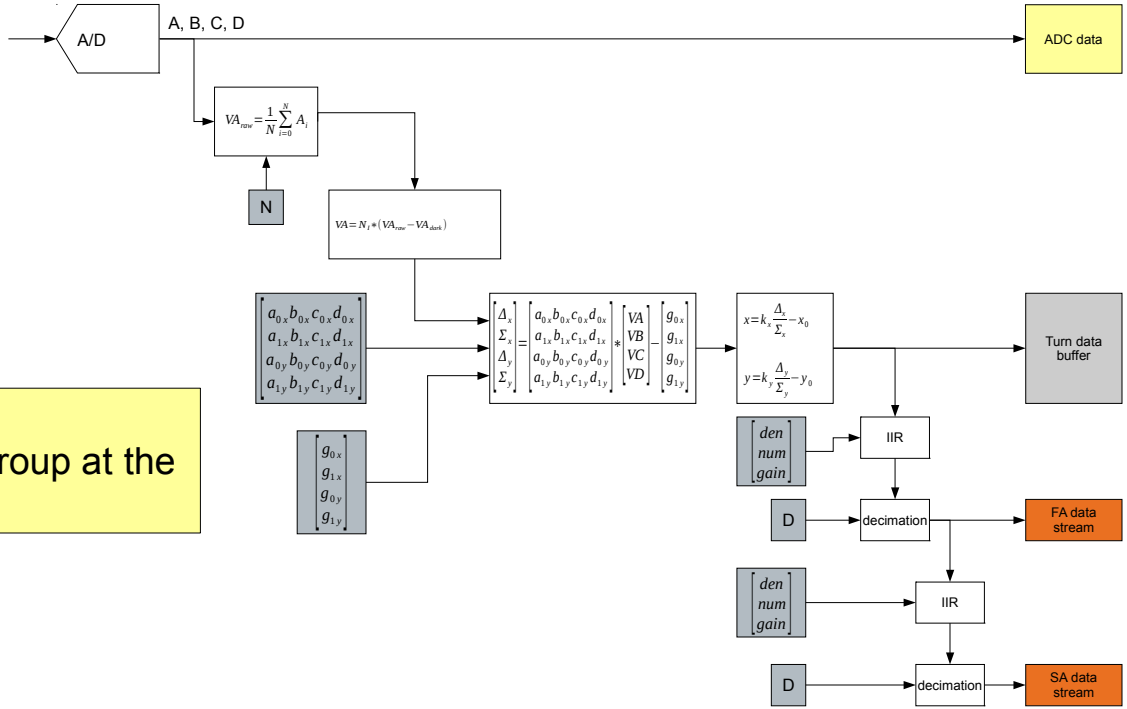
- Proposed by SOLEIL
- Tested with closed orbit feedback
- Used by non-electronic experts in experimental stations
- Several improvements proposed (external BIAS, »current monitor«, general simplification, cost, etc.)
- In 2015, stop of production
- New development started using platform C concept

Challenges

- Measurement performance!

	Libera Photon 2010	**Libera Photon 2016**
5 Hz bandwidth RMS	1.7 nm	**1.7 nm**
2 kHz bandwidth RMS	4.2 nm	**< 4 nm**
Temperature stability	< 10 nm / °C	**< 10 nm / °C**

Signal Processing



Proposed by diagnostics group at the APS

Default processing scheme

- TBT data rate equals the actual TBT frequency (if possible)
- FA data rate approximately 5 kS/s with ~2 kHz bandwidth
- SA data rate approximately 25 S/s with ~5 Hz bandwidth
- Position calculation equation:

$$X = \frac{K_X * (A + B) - (C + D)}{(A + B + C + D)} - X_{offset}$$

$$Y = \frac{K_Y * (A + D) - (B + C)}{(A + B + C + D)} - Y_{offset}$$

Configurable processing scheme (1)

- Position calculation equation:

$$\begin{bmatrix} \Delta_x \\ \Sigma_x \\ \Delta_y \\ \Sigma_y \end{bmatrix} = \begin{bmatrix} a_{0x} b_{0x} c_{0x} d_{0x} \\ a_{1x} b_{1x} c_{1x} d_{1x} \\ a_{0y} b_{0y} c_{0y} d_{0y} \\ a_{1y} b_{1y} c_{1y} d_{1y} \end{bmatrix} * \begin{bmatrix} VA \\ VB \\ VC \\ VD \end{bmatrix} - \begin{bmatrix} g_{0x} \\ g_{1x} \\ g_{0y} \\ g_{1y} \end{bmatrix}$$

$$x = k_x \frac{\Delta_x}{\Sigma_x} - x_0$$

$$y = k_y \frac{\Delta_y}{\Sigma_y} - y_0$$

Controlled by user

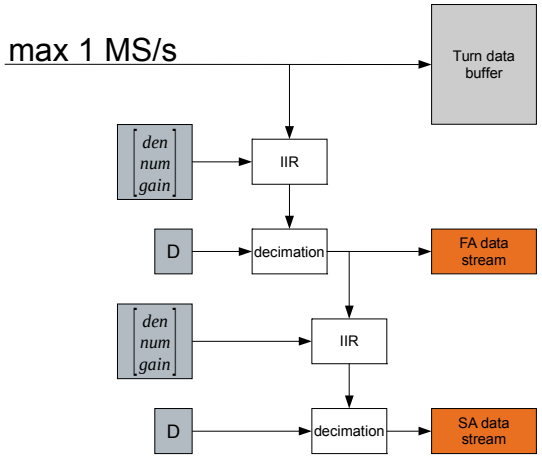
$$\begin{bmatrix} a_{0x} b_{0x} c_{0x} d_{0x} \\ a_{1x} b_{1x} c_{1x} d_{1x} \\ a_{0y} b_{0y} c_{0y} d_{0y} \\ a_{1y} b_{1y} c_{1y} d_{1y} \end{bmatrix} \qquad \begin{bmatrix} g_{0x} \\ g_{1x} \\ g_{0y} \\ g_{1y} \end{bmatrix}$$

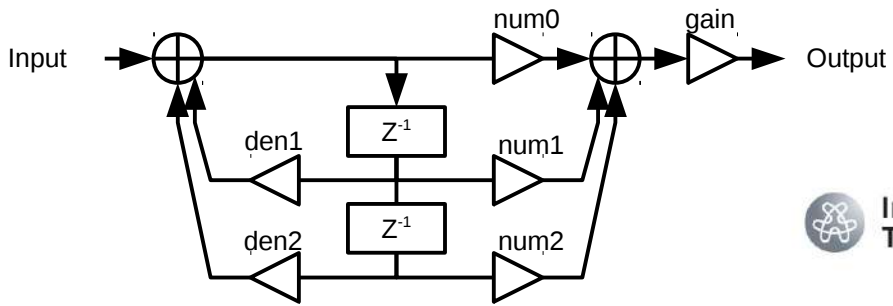
Configurable processing scheme (2)

FA and SA filtering

- IIR, 2 bi-quads
- Input data rate < 1 MS/s (from TBT)
- Detailed limitations in documentation
- Gain normalized to 1

  (TBT → FA → SA)





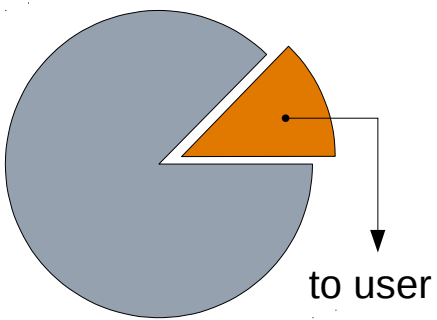
Instrumentation Technologies

Data buffers

ADC buffer

8 Msamples/channel

8 segments

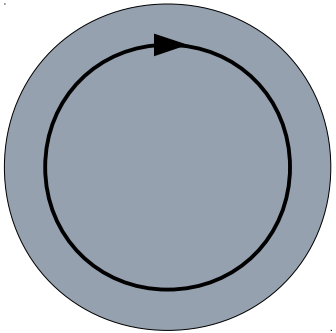


16 MSB

TBT buffer

4 Msamples/channel

circular buffer



32-bit

FA data

Continuous data stream

through RJ-45

32-bit

SA data

Continuous data stream

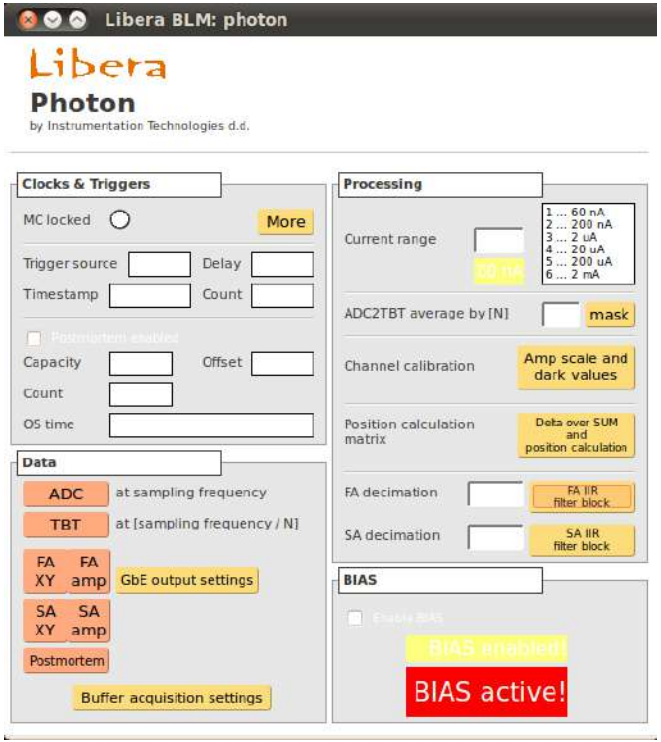
to software clients

32-bit

Instrumentation Technologies

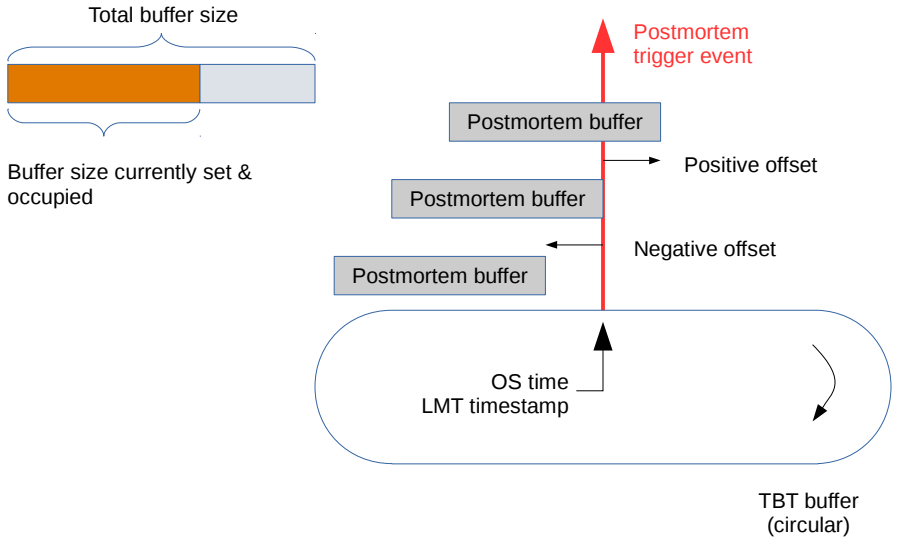
Functionalities

- ADC, TBT buffers
- Fast, slow data streams
- Real-time data output (dedicated interface)
- Postmortem
- Dark current compensation, channel scaling
- Detailed timestamping (for data buffers, trigger events, etc.)
- Synchronization mechanism
- Configurable signal processing scheme



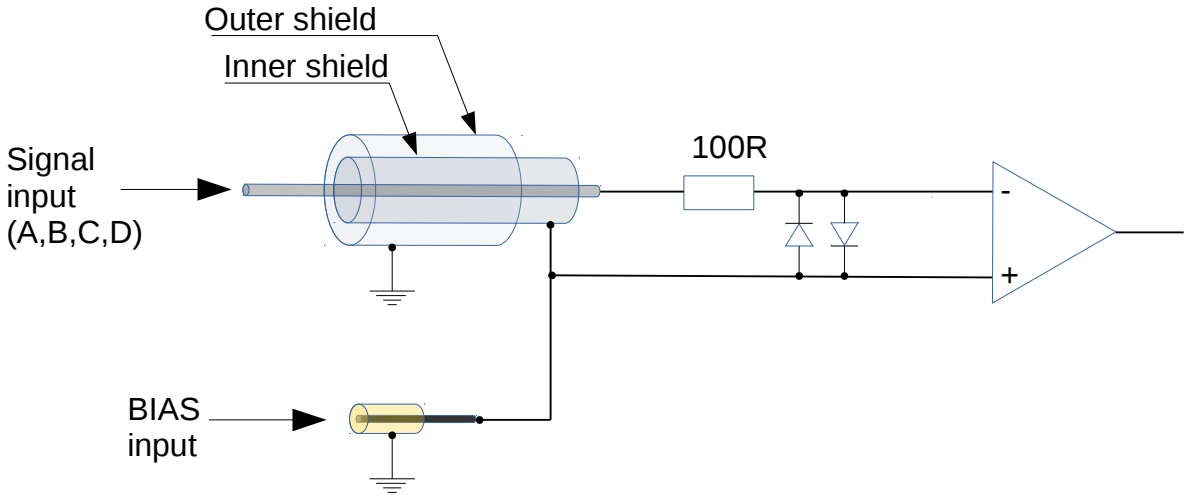
Postmortem

- External trigger (T1)
- 1 million data samples/ch
- Configurable offset
- Configurable buffer size/readout
- Absolute time timestamp
- Oscillator clock timestamp

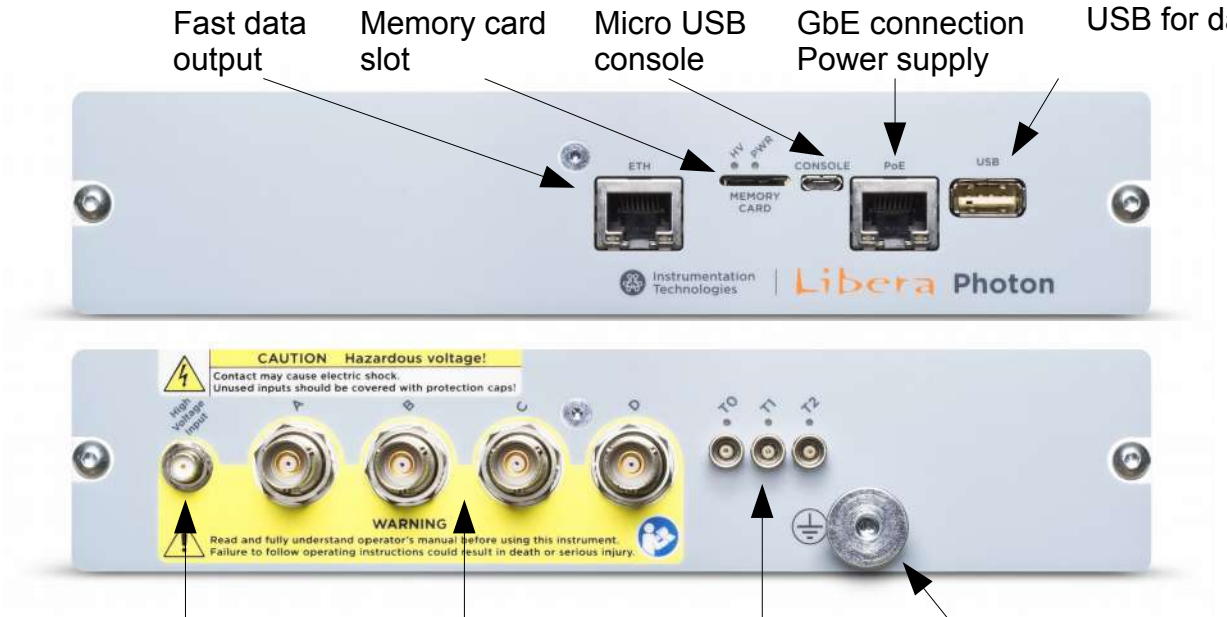


BIAS input / output

- No internal BIAS source
- BIAS from external source supported
- +/- 150 V can be applied
- BIAS voltage is applied to the inner shield of each of the 4 input connectors
- Red LED illuminates (front and back panel) when BIAS voltage over +/-15 V (for safety!)



The instrument

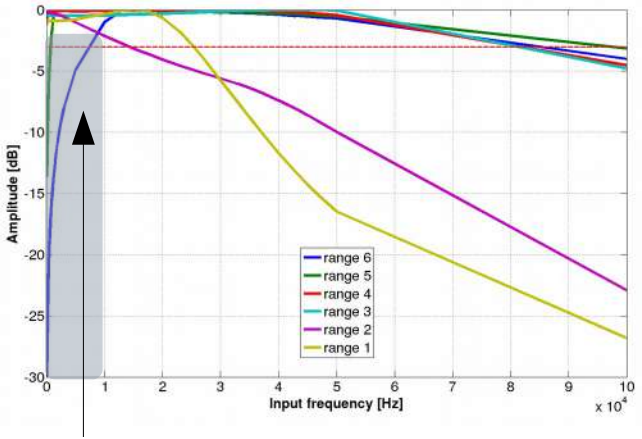


Instrumentation Technologies

Input characteristics

Nominal range	Feedback resistance	Measured current range	Analog 3 dB bandwidth
±60 nA	33 MΩ	59 nA	25 kHz
±200 nA	8.2 MΩ	230 nA	15 kHz
±2 uA	1 MΩ	2.01 uA	> 80 kHz
±20 uA	100 kΩ	19.5 uA	> 80 kHz
±200 uA	10 kΩ	200 uA	> 80 kHz
±2 mA	1 kΩ	1.96 mA	> 80 kHz
±20 mA*	100 Ω	20.9 mA	> 80 kHz

* will be disabled through software



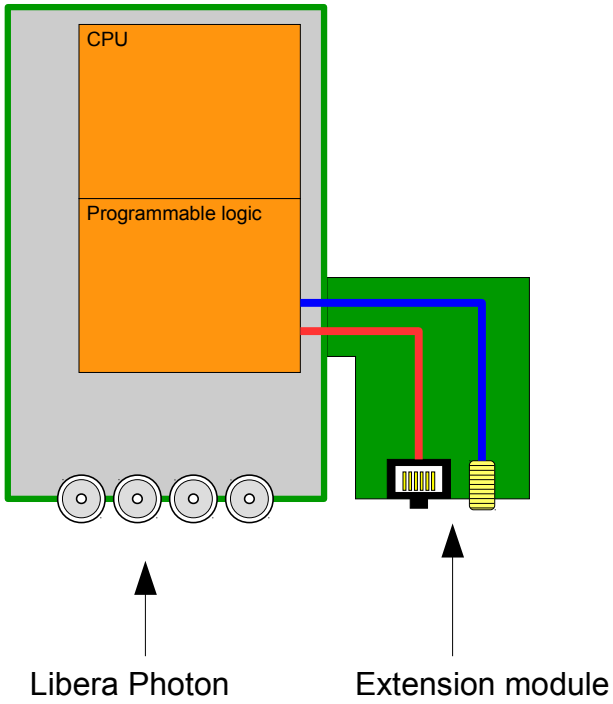
Instrumentation Technologies

Specification

- Max input current: ±2 mA
- Analog bandwidth: **> 80 kHz** @ > ±2 µA
- Latency (step response): < 10 µs
- A/D conversion at ~2.5 MS/s, 18 bits
- Fast data rate: ~5 kS/s (2 kHz bandwidth)
- Slow data rate: 25 S/s (5 Hz bandwidth)

Extension module (no avail yet)

- To offer analog output for feedback purposes
- Planned from design phase, instrument can be upgraded, space was allocated already
- Type of connector (SMA, BNC, LEMO?) and DAC still to be specified
- Space available for 2 connectors (e.g. SMA and RJ-25); serial data output possible as well
- Data pins directly controlled by the Programmable Logic (FPGA) from Zynq



First shipments

- Northwestern University (beamline at APS)
- SSRF
- NSRRC

Conclusion

- Lightweight and compact
- Powered over Ethernet (PoE), ~10 Watt
- Wide analog bandwidth
- Easy to access and manage