Libera

Extensions and common points of the platform C instruments

Peter Leban, June 1, 2017

Libera

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Instrumentation Technologies

Platform C hardware

Libera **Spark**
ERXR / EL / HL / HR

Libera **Digit**
AC / DC

Libera **BLM**

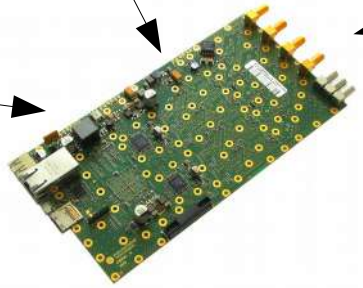
Libera **Photon**

Equipped for – Spark EL
Equipped for – Spark HL
Equipped for – Spark HR
Equipped for – Spark ER

Equipped for – DIGIT AC

Equipped for – DIGIT DC in BLM

Equipped for – Photon



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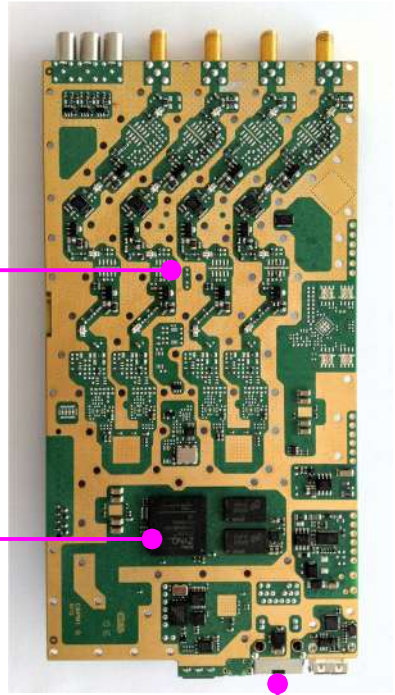
Common hardware points

3x Input / output LEMO

4 channels with various assembly options



2x dual channel ADC

Extension slot

Zynq 7020

PoE

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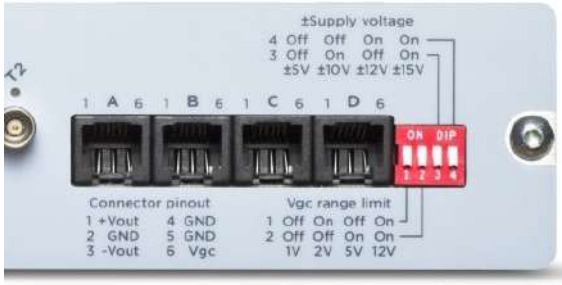
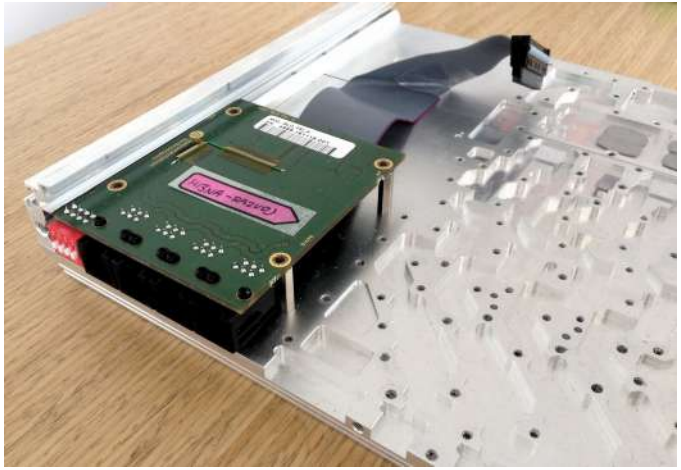
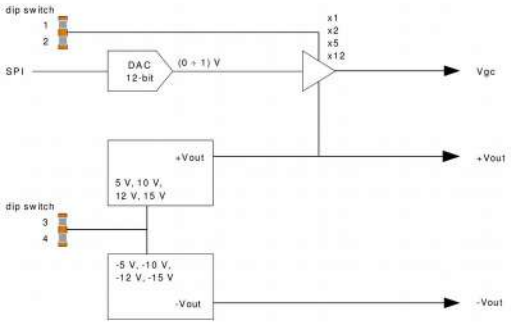
Extension module for BLM

- 4x RJ25 interface
- DIP switch
- Power supply and gain control for the PMTs
- Direct control from Zynq (FPGA and OS)

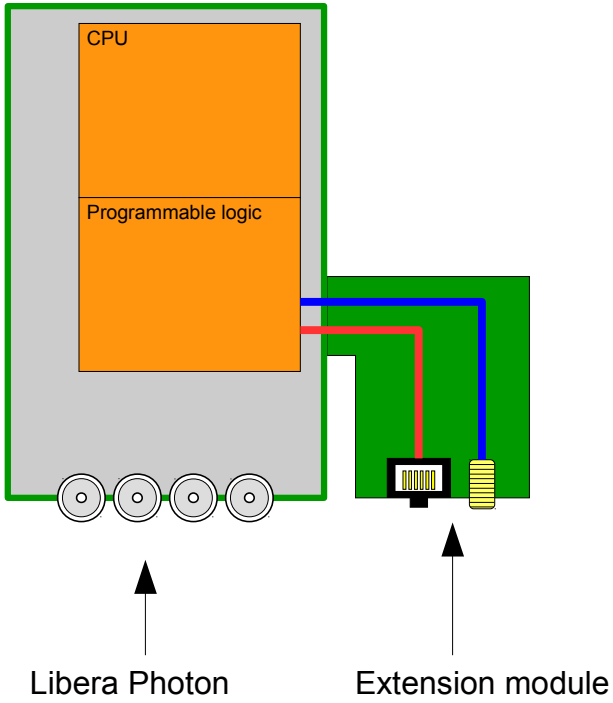






Extension module for Photon (not developed yet)

- To offer analog output for feedback purposes
- Planned from design phase, instrument can be upgraded, space was allocated already
- Type of connector (SMA, BNC, LEMO?) and DAC still to be specified
- Space available for 2 connectors (e.g. SMA and RJ-25); serial data output possible as well
- Data pins directly controlled by the Programmable Logic (FPGA) from Zynq



(Hardware) updates for platform C

Users asked for

- Fast data output (additional dedicated interface)
- Different ADC sensitivity
- Interlock capability

for Spark ERXR

- Several modifications in **ebpm**, **blm** and **photon** applications

for energy ramping application

“oscilloscope” features

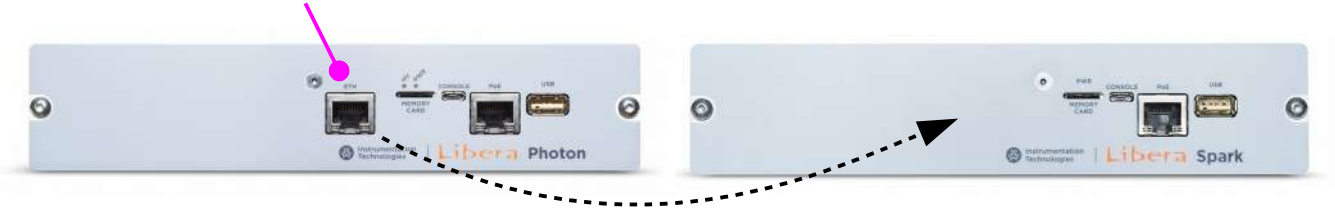
for beam profile monitors

Fast data output

asked by ESRF, APS

It is available in Libera Photon. The PCB is slightly different from the BLM, Spark and Digit

RJ-45 for fast data output (UDP)



Available options:

- TBT streaming data (depends on the data rate)
- FA streaming data
- Other continuous data stream, processed by the FPGA

PCB respin required

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ADC sensitivity

asked by ESRF

It is configured during assembly. For the future, it could be done runtime by user.

Available options:

- 0.5 V full scale
- 1.0 V full scale

PCB respin required

Interlock capability

asked by Cornell

Typical use (all configured as inputs)

- T0 … reference clock (»tbt«)
- T1 … postmortem trigger
- T2 … (acquisition) trigger

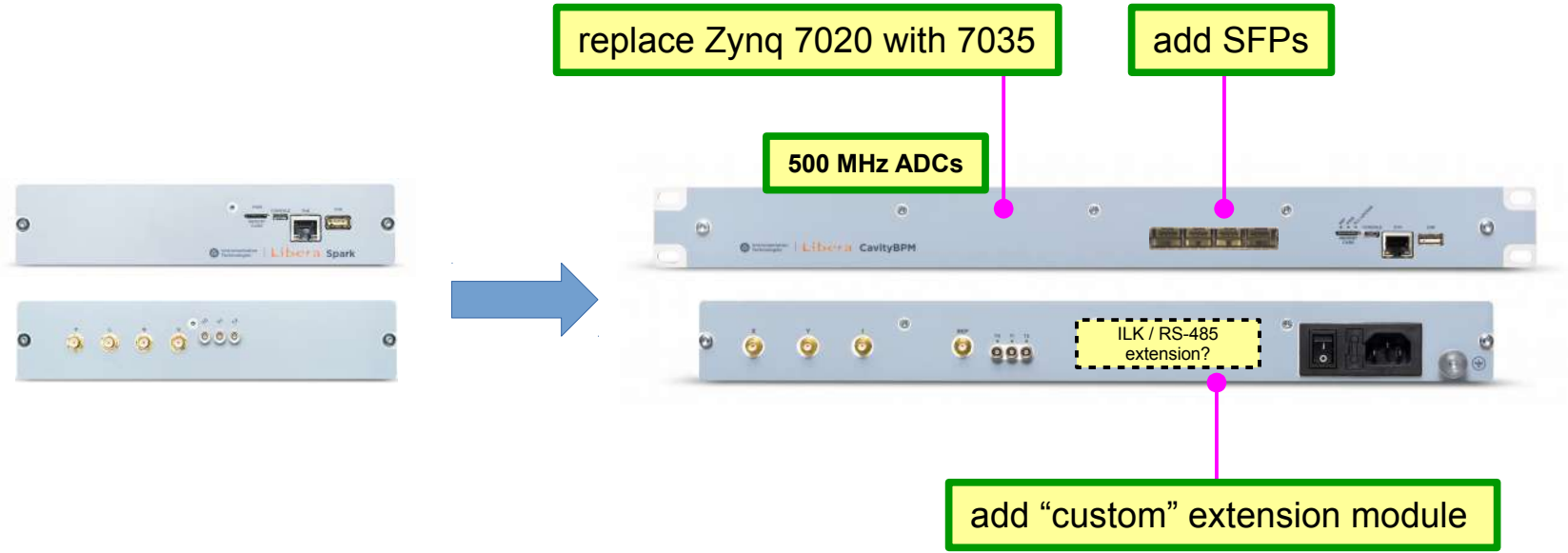
Interlock output on the extension module

- Interlock functionality implementation (FPGA, software)
- Use same circuit as on the Libera Electron / Brilliance / +

PCB respin is NOT required

FOFB capability?

brainstorming



Not cheap anymore!

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Software

- Support for most devices in the general framework: Libera BASE

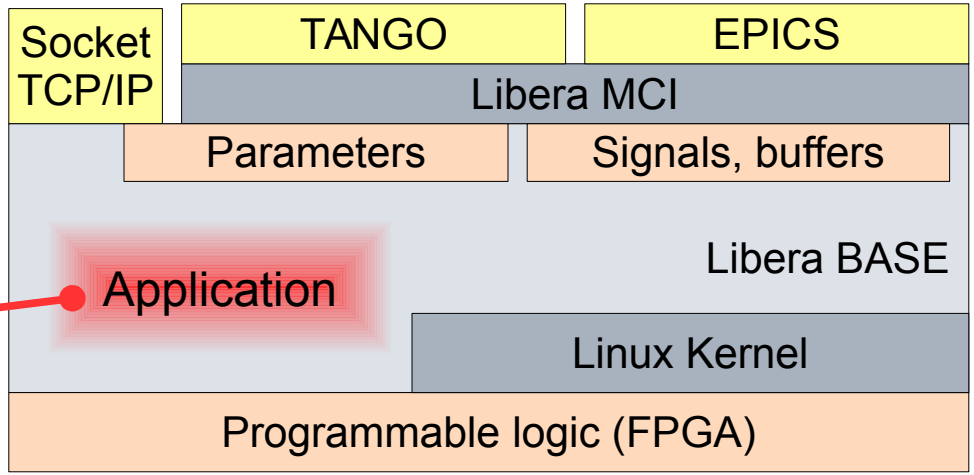
  Continuously developed, currently builds for lucid (32/64), trusty (32/64), CentOS and Zynq

  Interfaces to latest ADCs (500 MHz) and FPGA (Zynq 7035)
- Client application is backward compatible (MCI)
- New application does not interfere (unless required) with the Libera BASE
- EPICS, TANGO and Socket interfaces are cross-platform compatible

Common software points

- FPGA cores
- Libera BASE
- EPICS interface
- TANGO interface
- *Socket TCP/IP interface

Application (digit, beam loss, bpm) is **custom** but uses common blocks.



* Development version available only

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(I-Tech's) TANGO interface

...is called **libera-ds**

- Initial version installed in Libera Brilliance+ (THOM-X)
- Improved version then installed on Libera BLM (ESRF) and Libera Spark EL (ALBA)
- Further debugging by THOM-X and ESRF; latest updates provided by ESRF
- Same code compiled for Ubuntu lucid/trusty and Zynq Linux
- … to be continued

(I-Tech's) EPICS interface

...is called **libera-ioc**

- Several updates since year 2010 (from CA server to IOC)
- Using I-Tech's patched EPICS BASE 3.14.12.2 for optimal CPU consumption
- … complaints / requirements from NSRL, NSRRC and APS
- Migration to the official EPICS BASE 3.15.5; currently under testing at NSRRC and APS
- Requires smarter handling of buffer readout (disable when not in use)
- All use cases not known; yet to be improved

Socket TCP/IP interface

...is called **libera-scpi**

- Bypasses the MCI layer; direct calls to the Libera BASE
- SCPI-like commands
- Tested in MATLAB environment
- ...to be further expanded

```
format longG

t=tcpip('10.0.6.114',5677,'NetworkRole','client')
t.InputBufferSize=100000
fopen(t)
fprintf(t,'dump')

data=fread(t,27)

while t.BytesAvailable > 0
    data=fscanf(t,'%c',t.BytesAvailable)
    %strread(data)
    str2num(data)
end

fclose(t)
```

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Conclusion

- Many instruments based on the same PCB
- Extension slot available for various modules
- Common software framework allows fast development cycles
- Platform upgrade possible with use of faster A/D converters

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