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Libera Electron/Brilliance, release 2.00

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Features for Release 2.00

- Operating system platform upgrade
- Improved stability and robustness of Libera software
- Implementation of new features

What's New – OS Platform Upgrade (1)

- New armel Linux platform
  - More efficient protocol between the kernel and programs
- Upgrade to Linux kernel 2.6.25
  - Newer versions investigated
- Improved multithreading
  - Using Native Posix Threads Library (NPTL)
- FPGA/SBC bus timing fine tuned
- Improved DHCP functionality
  - Setting hostnames to Liberas according to their MAC addresses (not only IPs)

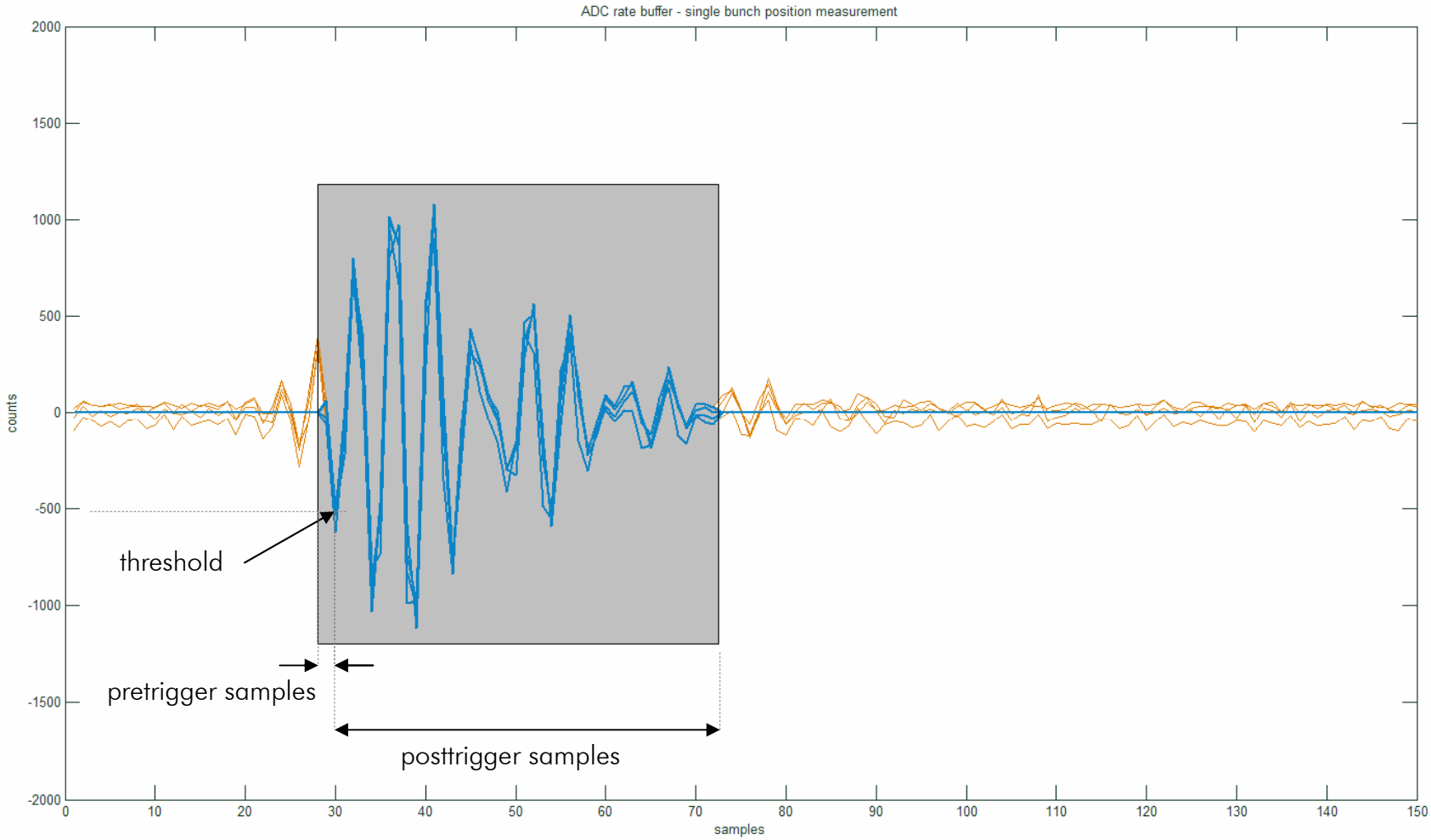
What's New – OS Platform Upgrade(2)

- A lot of effort was put into easier upgrade from previous platform
- Performance improvements:
  - 9x – 10x faster floating point operations
  - FPGA/SBC throughput is higher up to 30 %
  - Faster creation of threads, depending on number of threads
  - Threads use less memory

What's new - functions

- Position calculation from ADC rate buffer at single-bunch filling
- Position calculation from ADC rate buffer at 100 % filling
- Antispike
- Calculation of average SUM between two triggers
- 2nd maximum ADC value (from all 4 channels) is available to read
- Post-mortem triggering

Position Calculation from ADC Rate Buffer at Single-bunch Filling (1)



Position Calculation from ADC Rate Buffer at Single-bunch Filling (2)

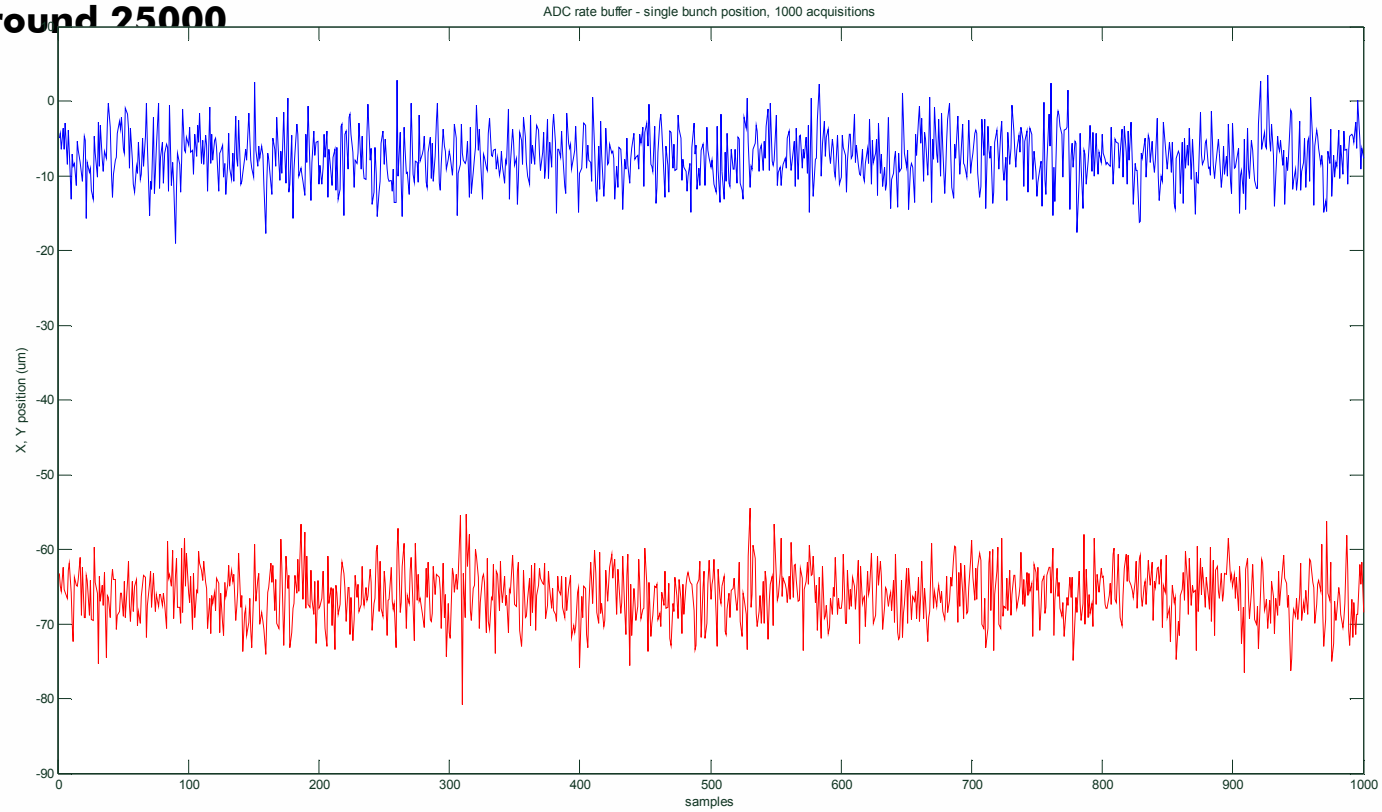
libera -3 1000 --sb
to run single-bunch position measurement directly on Libera

Output:
[threshold position threshold pretrigger posttrigger X Y SUM]

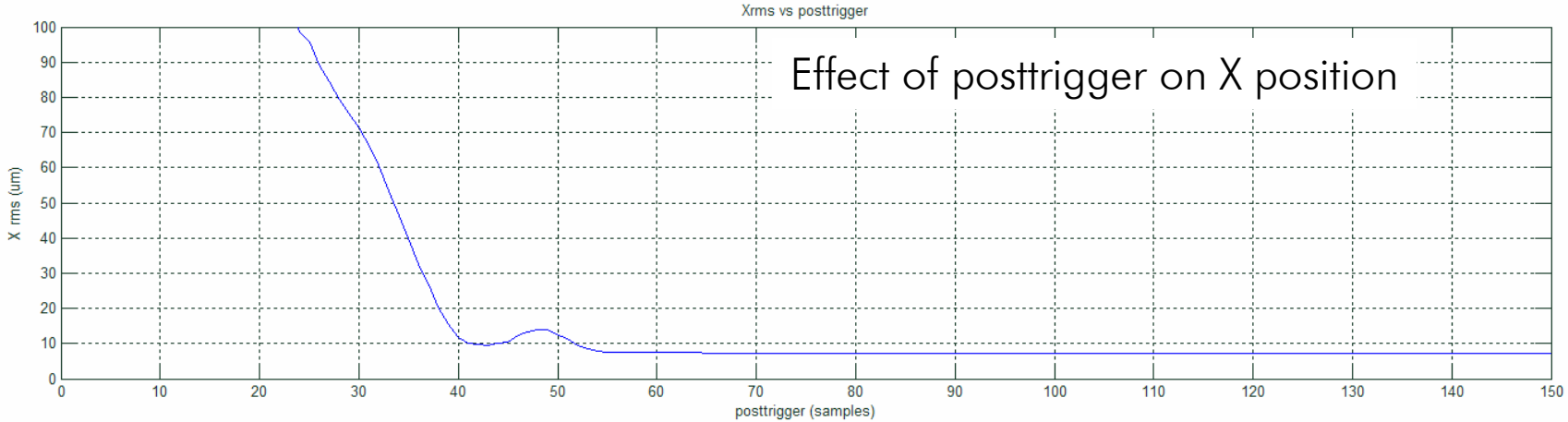
threshold ... not to take into account all noise below useful part of signal
pre/post trigger ... to define useful part of signal
X, Y ... position of bunch
SUM ... related to current

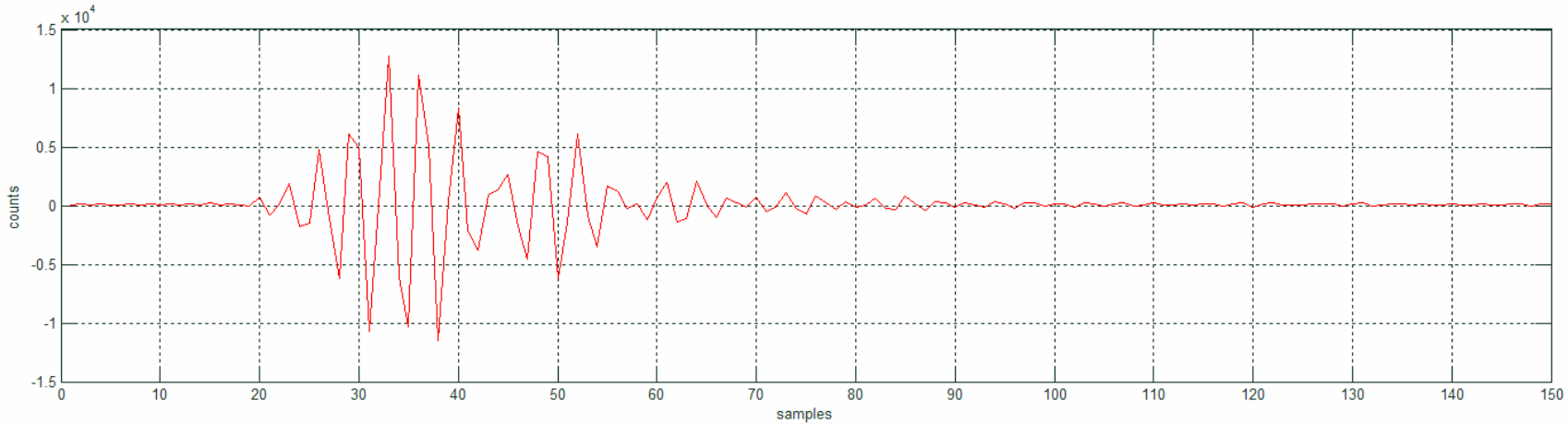
Position Calculation from ADC Rate Buffer at Single-bunch Filling – Test Case 1

- 1000 ADC rate buffers acquired (150 samples each)
- position calculated for each bunch
- number of counts: around 25000
- Xrms = 3,5045 um
- Yrms = 3,5672 um



Position Calculation from ADC Rate Buffer at Single-bunch Filling – Parameter Optimization





Position Calculation from ADC Rate Buffer at Single-bunch Filling – Posttrigger Effect, Test Case

Posttrigger	Xrms [μm]	Yrms [μm]
30	16,87	9,25
80	7,05	6,76

Position Calculation from ADC Rate Buffer at cw (1)

libera -3 1000 --cw
to run position measurement at cw directly on Libera

Output:
[A; B; C; D; X; Y; Q; A′; B′; C′; D′]

Where:
A, B, C, D … original values from bpms
X, Y, Q … calculated position
A′, B′, C′, D′ … recalculated values from bpms

Recalculation is needed because samples are not exactly 1 sample (90deg) apart.

Position Calculation from ADC Rate Buffer at cw - Calculation

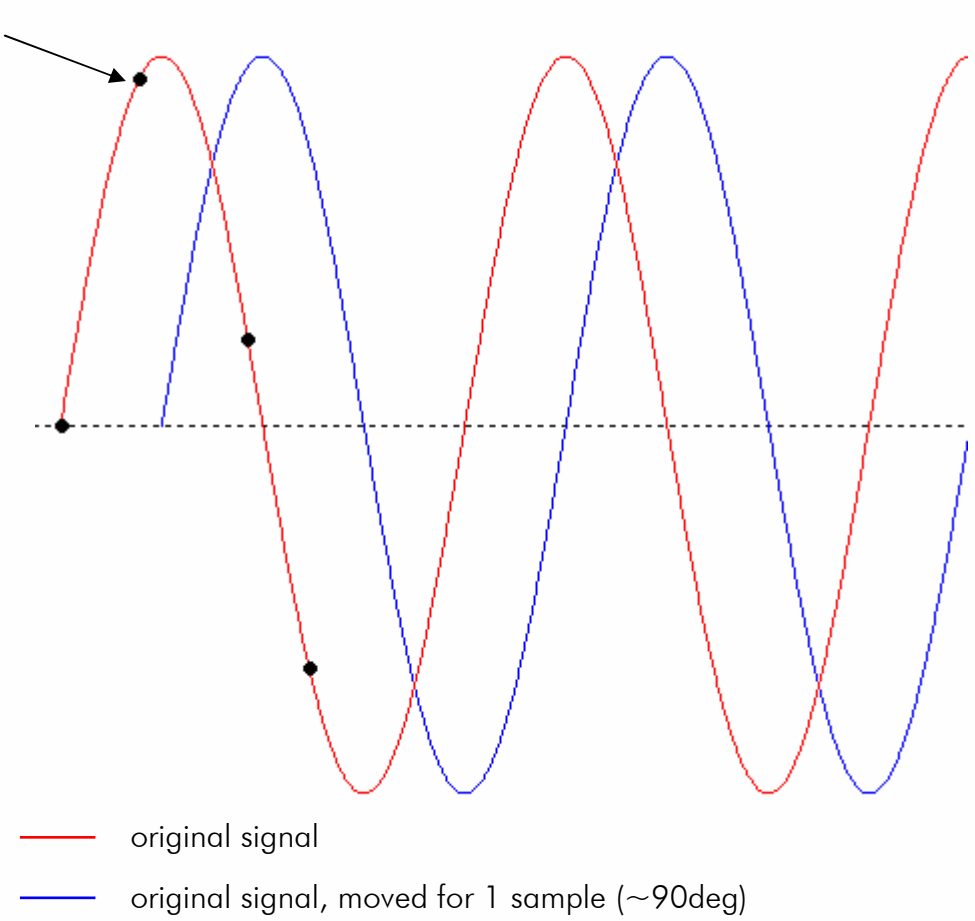
Ia ... original signal

Qa(n)=sqrt[(a*Ia(n))^2+(b*Ia(n-1))^2]

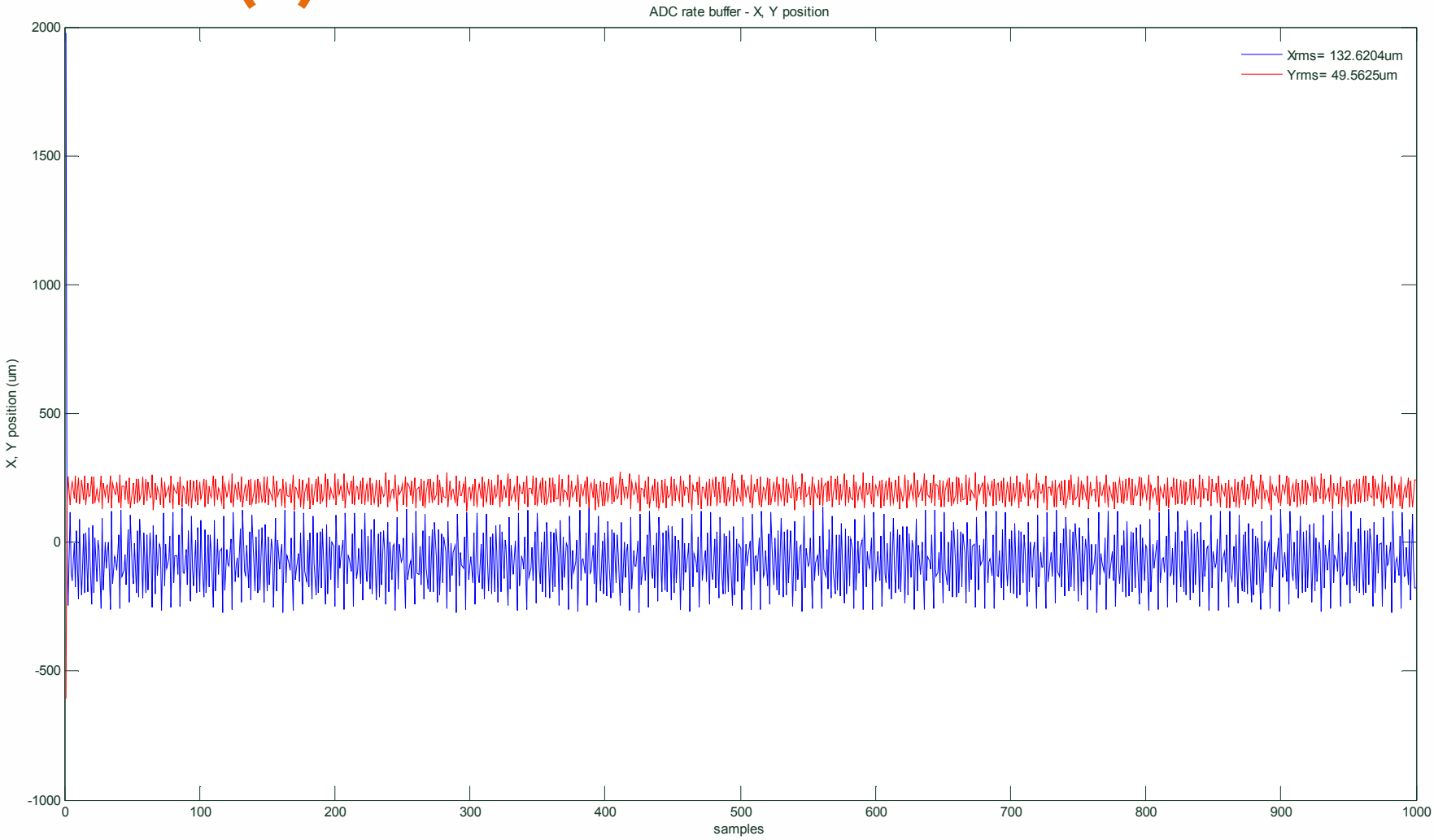
Va(n)=sqrt[(Ia(n))^2+(Ia(n-1))^2]

a=-1/tgθ
b=1/sinθ
θ**=2¶*NCO/VCXO**

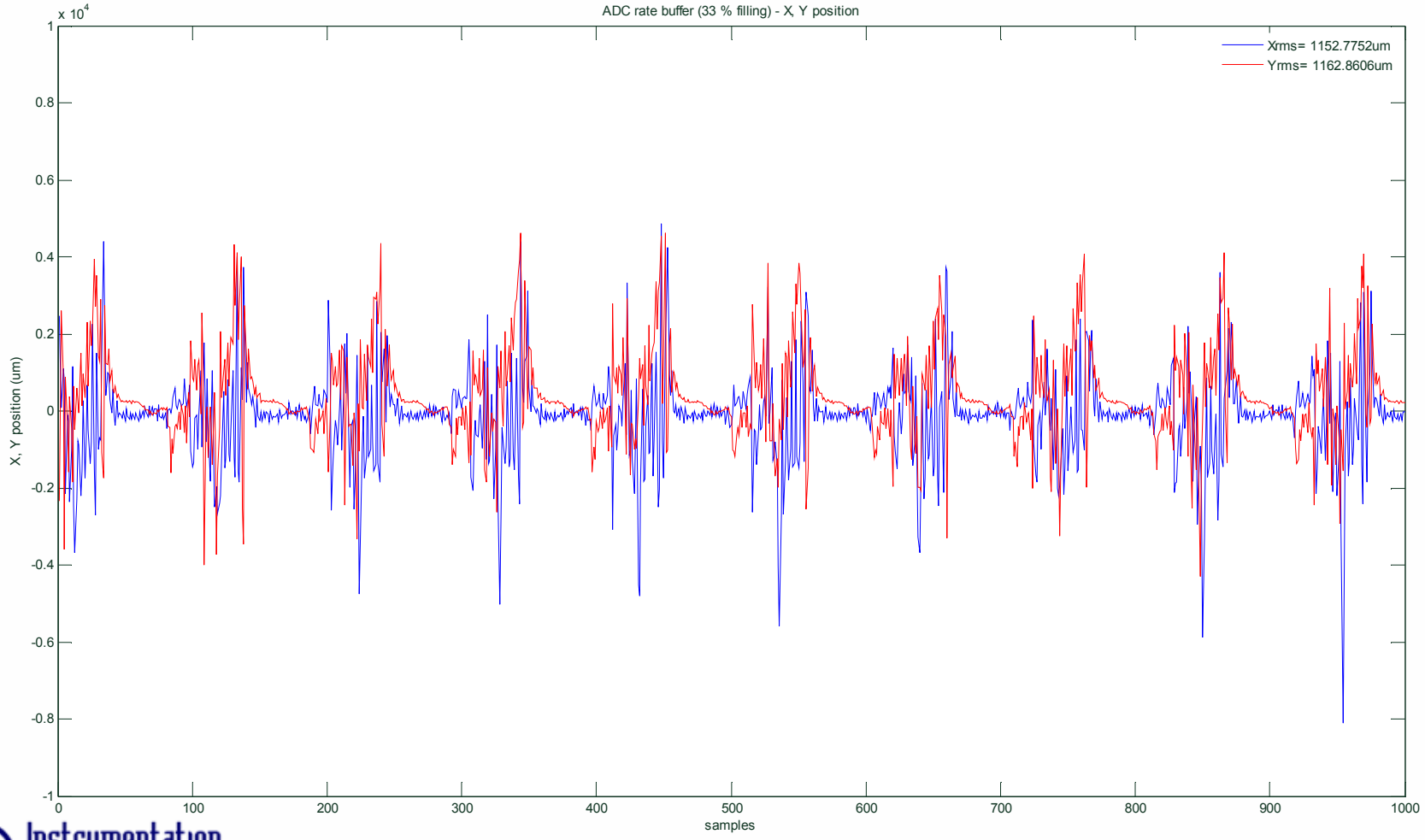
Example: diamond_220_sr
a=0,0286
b=1,0004



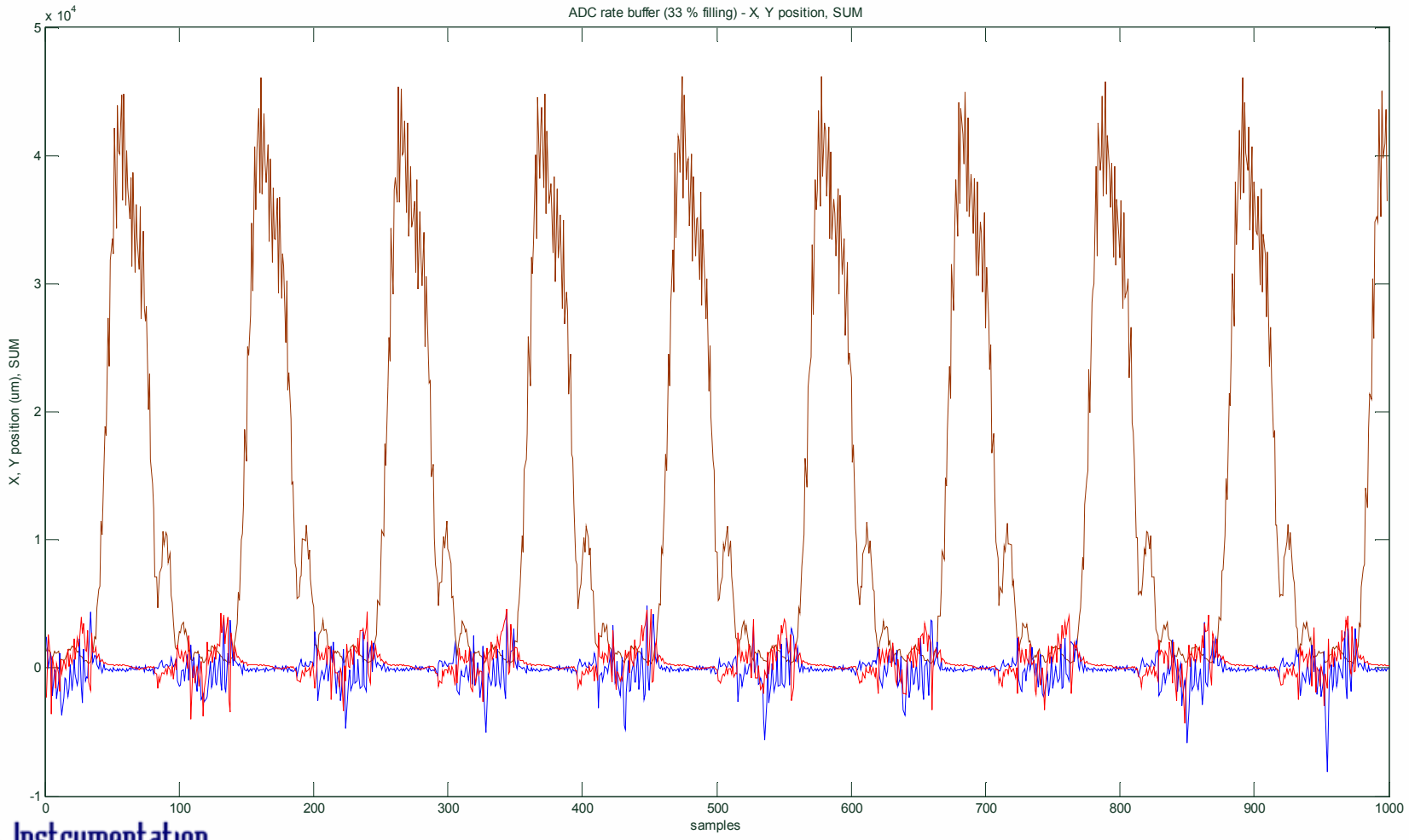
Position Calculation from ADC Rate Buffer at cw (2)



Position Calculation from ADC Rate Buffer at 33 % Bunch Filling



Position Calculation from ADC Rate Buffer at 33 % Bunch Filling – X, Y Position & SUM

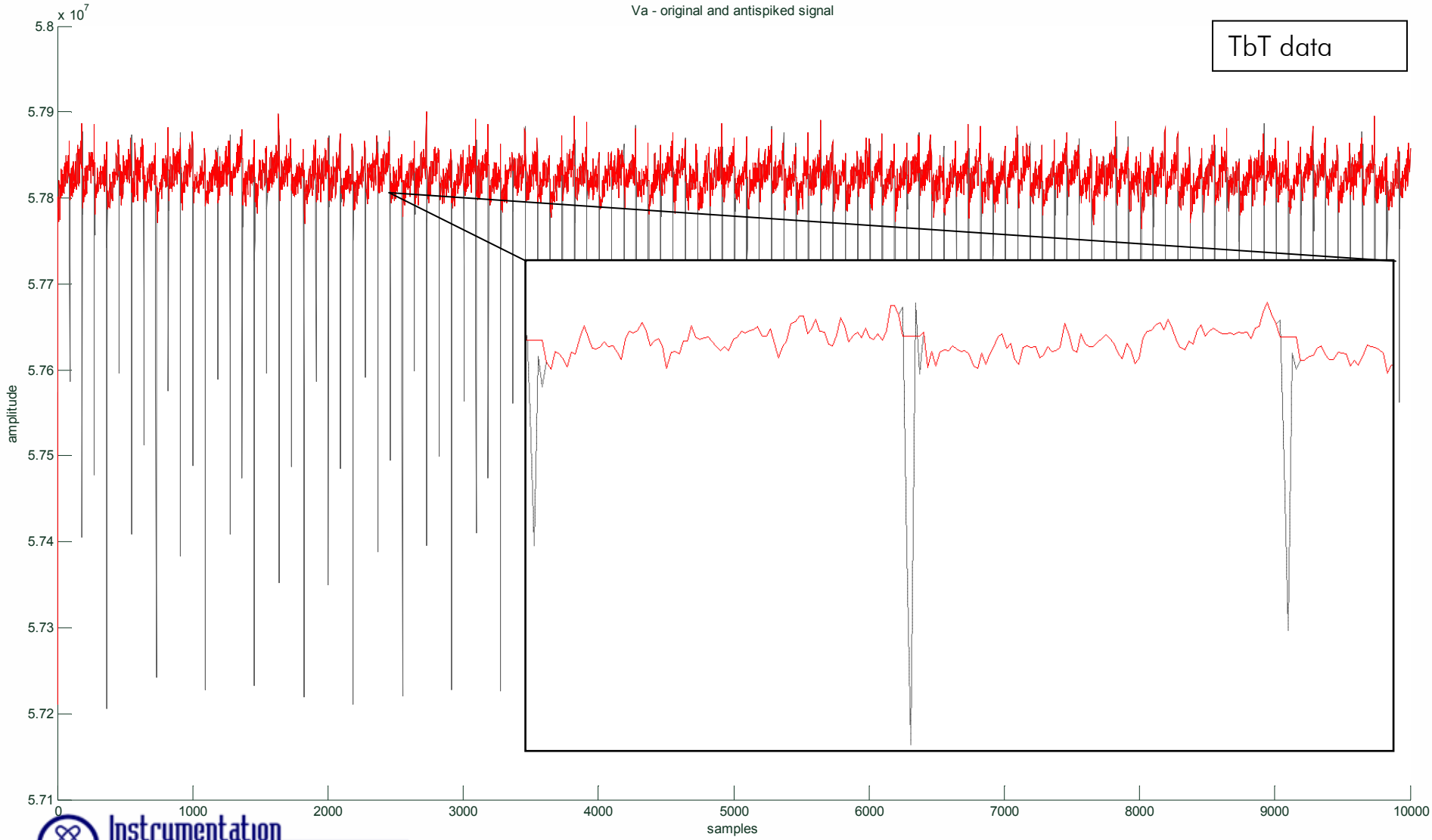


Conclusion – Position Measurement from ADC

- **Position measurement works fine with single bunch fill. When measured on test setup, position RMS under 4 μm was achieved.**

- **It is possible to use single bunch position measurement method to calculate position of cw (100 % or any filling).**

Antispike (1)


Va - original and antispiked signal
x 10^7
5.8
5.79
5.78
5.77
5.76
5.75
5.74
5.73
5.72
5.71
amplitude
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000
samples
TbT data

Antispike (2)

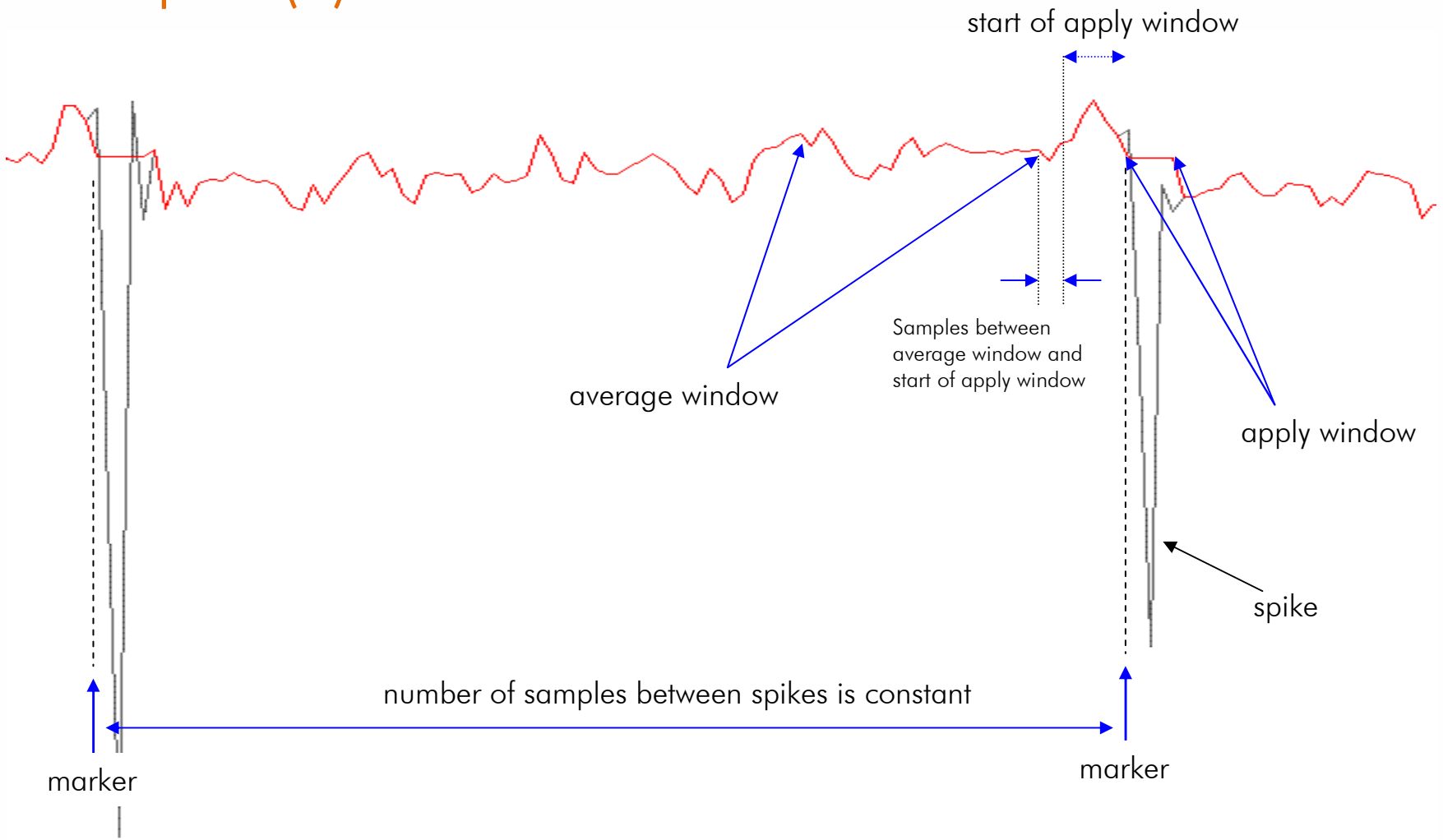
Spikes appear, when switches change position. Their position is well defined.
Antispike function is implemented in FPGA and CSPI.

- by default, antispike function is always on (FPGA and CSPI)
- CSPI:
  - User can acquire raw data without antispike function (libera -0 –r)
  - User can acquire data (amplitudes) with antispike function (libera -0)

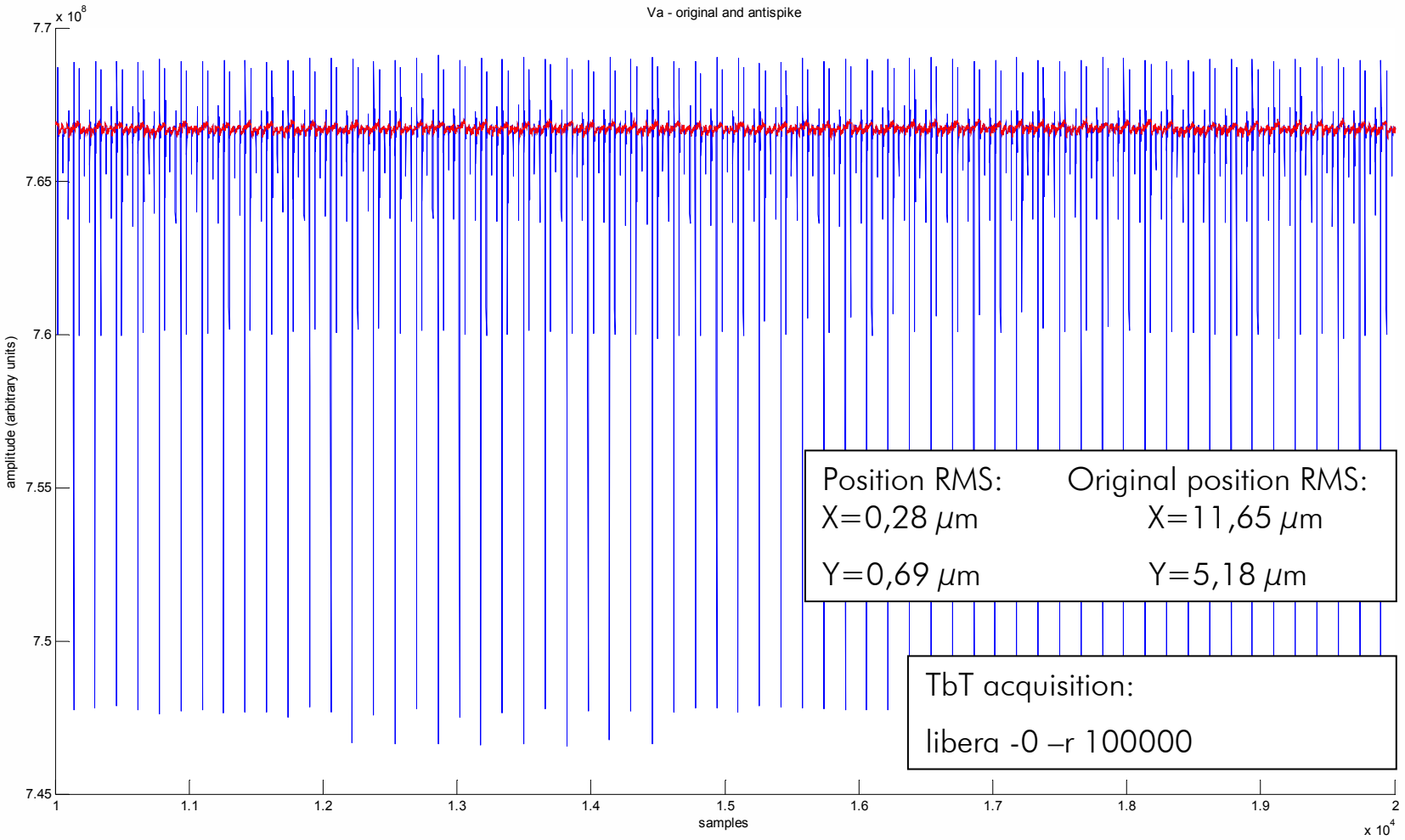
- FPGA:
  - Antispike function is used for FA and SA data output

- it is possible to turn antispike function off (/etc/default/libera)

Antispike (3)

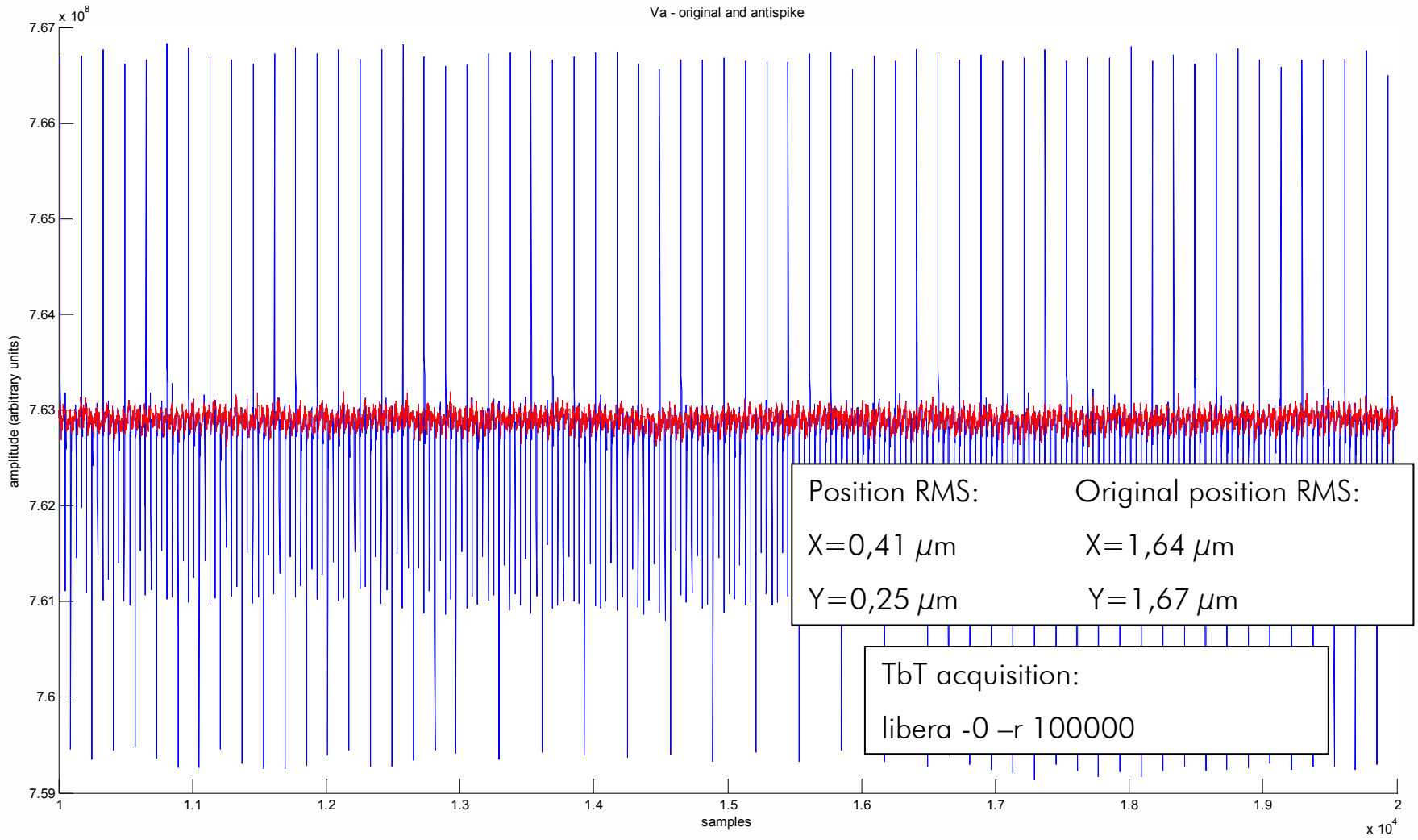

start of apply window
Samples between
average window and
start of apply window
average window
apply window
spike
number of samples between spikes is constant
marker
marker

Antispike – example: phase-matched cables



Design: diamond_220_sr (Brilliance)

Antispike – example: phase non-matched cables



Position RMS:	Original position RMS:
X=0,41 μm	X=1,64 μm
Y=0,25 μm	Y=1,67 μm

TbT acquisition:

libera -0 –r 100000

Design: diamond_220_sr (Brilliance)

Conclusion - antispike

- it is very effective when phase non-matched cables are used
- the effect is more visible with Libera Brilliance
- amplitudes Va, Vb, Vc and Vd are corrected
- X, Y position is more accurate, RMS is lowered
  - up 30x lower RMS on TbT data (phase non-matched cables)
  - up to 5x lower RMS on FA data (phase non-matched cables)
  - up to 25x lower RMS on SA data (phase non-matched cables)

Average SUM between two triggers

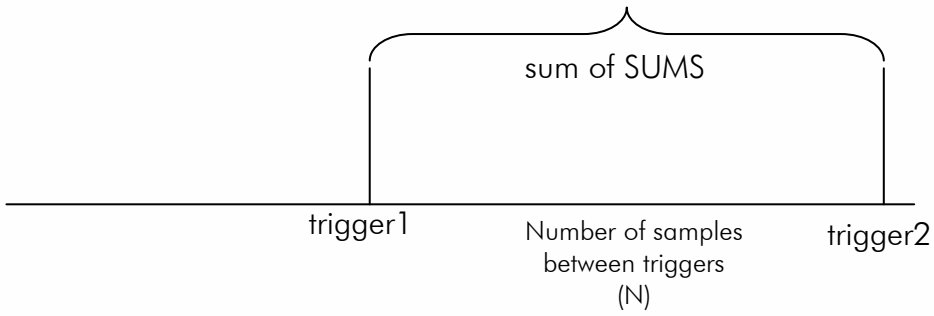
- Goal is to measure current increase between two triggers
- Calculation is done on SUM data @FA data rate

- New switch for libera: libera -4 –n<number of acquisitions>

- Output from Libera: [timestamp_of_current_trigger average_sum]

timestamp=trigger2 (timestamp)

$$\text{average\_sum} = \frac{\text{sum of SUMS}}{N}$$



2nd max value of ADC data rate

- Goal is to continuously check (2nd) max value in ADC data rate
- Correlation with beam current can be done (accelerator specific)

- Value can be seen: libera –l
- Parameter: MAXADC

example:

ADC value [cnt]	Beam current [mA]
1000	5
5000	30
10000	120
25000	300

Post-mortem trigger

- Source of the trigger can be any of:
  - external PM trigger
  - position data (Xmin, Xmax, Ymin, Ymax)
  - overflow_limit
  - overflow_duration

- Limits/mode can be set through libera –s

Parameter: POSTMORTEM <Xmin Ymin Xmax Ymax overflow_limit overflow_dur mode>

Conclusion

- Majority of the features on the final version of the Libera Wish List, (www.i-tech.si/forum) have been implemented
- Release 2.00 will be available beginning of December 2008.
- Users are welcome to visit our forum to share experience and ask questions.