Libera

RECONFIGURABLE INSTRUMENTATION
Historical Overview, New Trends and Challenges

Rok Uršič, Libera Workshop, April 2013, Solkan

RF engineer, Particle Accelerators, Reconfigurability

- 1990: Particle Accelerators: Jean-Claude Denard, Sincrotrone Trieste,
- 1995: DDC concept: Position Monitoring of Low Intensity Beams Using a Digital Frequency Down Converter; Hengjie Ma, Craig Drennan, Beam Instrumentation Workshop, Vancouver, 1995 (Harris HSP50016)
- 1999: First deployed Digital BPM: Swiss Light Source (4 channel DDC ASIC, Intersil HSP50216) 1999
- 2002: BIW talk – Reconfigurable Instrumentation Technologies, Architectures and Trends
- 2003: Launching Libera
- 2013: Libera workshop

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Reconfigurable Instrumentation Technologies, Architectures and Trends

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Instrumentation Technologies
Solkan, Slovenia

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Why to reconfigure

- To build a system that can "grow" with the accelerator and support new requirements or applications without changing hardware.
- In order to do that, we have to liberate radio-based devices from the chronic dependency on hard-wired characteristics of the radio front end.
- To build a system that is standardized in manufacturing (low cost) but customized in application (flexibility).

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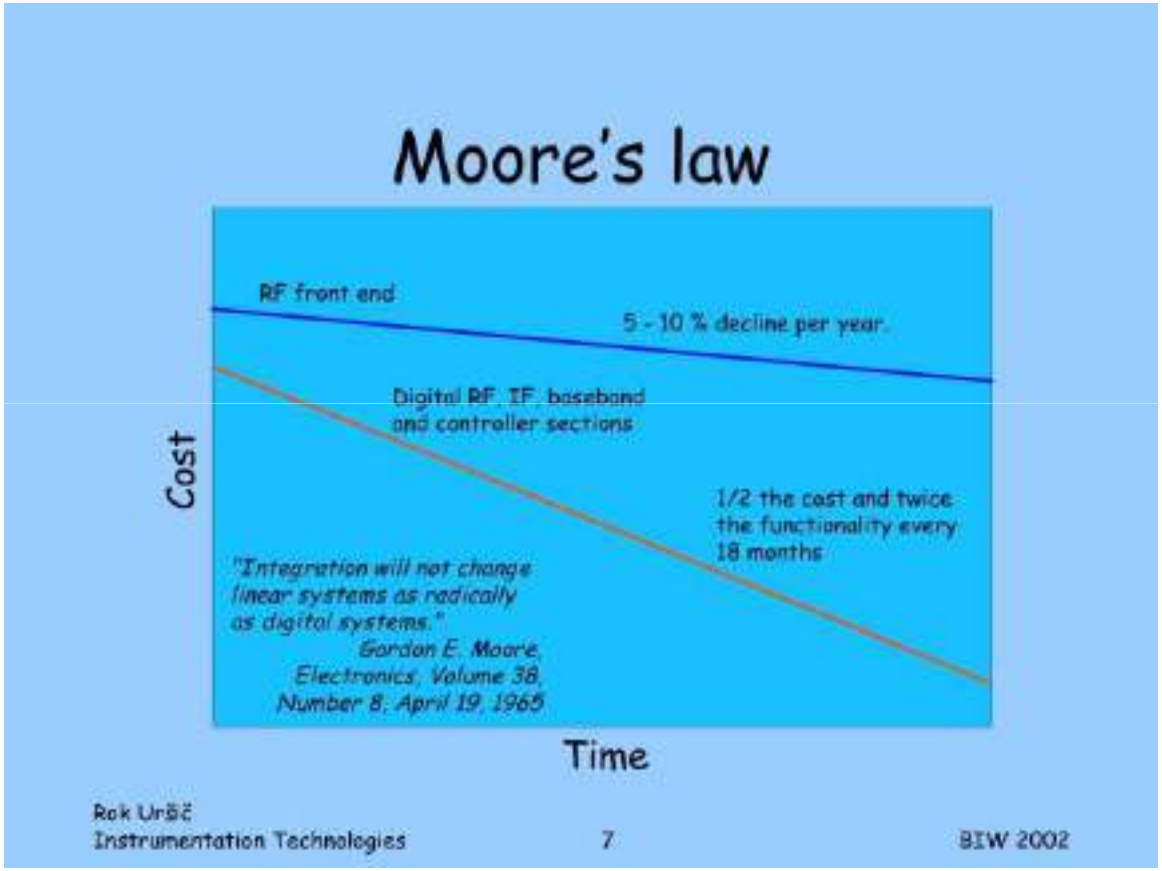
Enablers

- High-performance analog-to-digital converter ICs
- High-performance digital signal processing Ics
- "The future of integrated electronics is the future of electronics itself", Gordon E. Moore, Electronics, Volume 38, number 8, April 19, 1965


Moore's law
RF front end
5 - 10 % decline per year.
Digital RF, IF, baseband
and controller sections
1/2 the cost and twice
the functionality every
18 months
"Integration will not change
linear systems as radically
as digital systems."
Gordon E. Moore,
Electronics, Volume 38,
Number 8, April 19, 1965
Cost
Time
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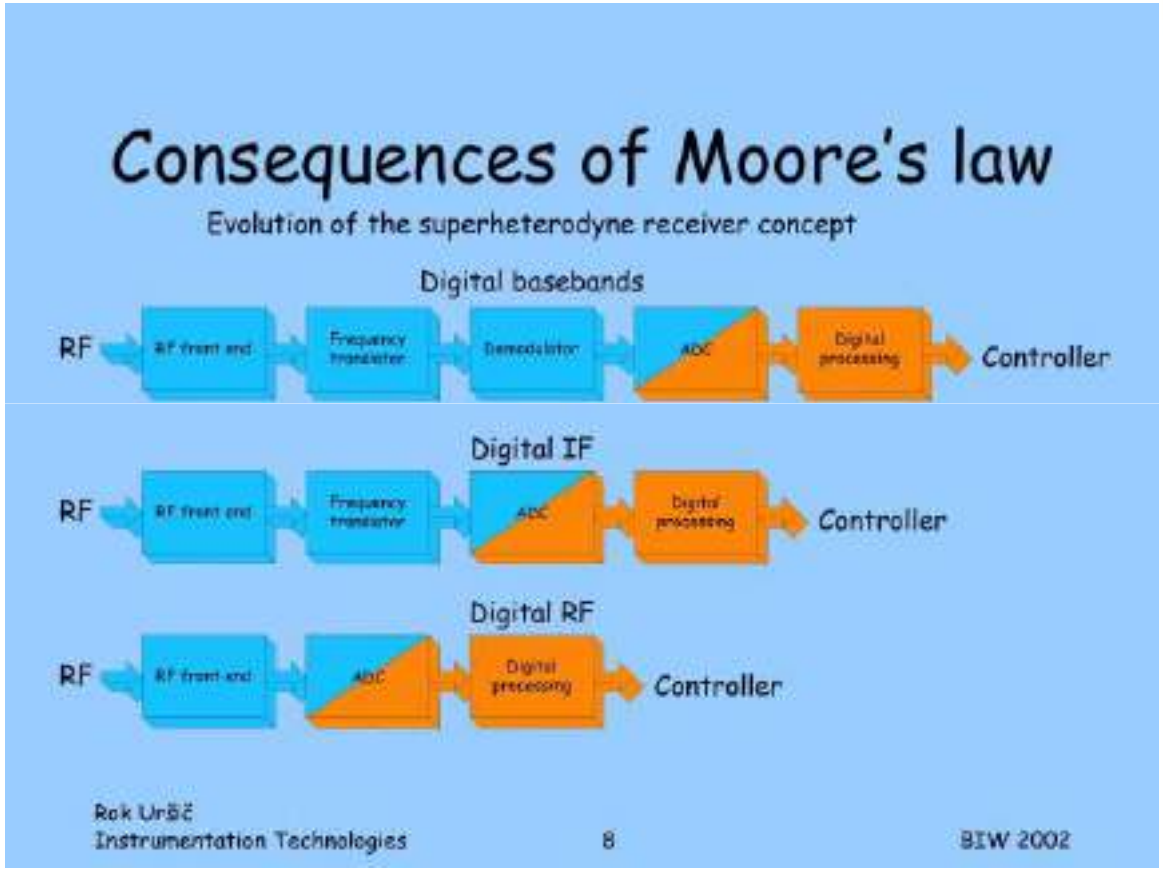
Consequences of Moore's law
Evolution of the superheterodyne receiver concept
Digital basebands
RF
RF front end
Frequency translator
Demodulator
ADC
Digital processing
Controller
Digital IF
RF
RF front end
Frequency translator
ADC
Digital processing
Controller
Digital RF
RF
RF front end
ADC
Digital processing
Controller
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Caveat

- At first glance, the radio frequency front ends are shrinking in size and complexity, however, by making them more generic, new challenges arise.
- Special filters, gain control schemes and very linear amplifiers that provide a large dynamic range are a few of the new requirements that challenge designers.
- Good RF front end design is critical for the performance of the whole system.

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Processing IC families

	ASIC	DSP	FPGA	*Re-configurable computing*
Hardware adaptability	-	-	+	+
Program-mability	-	+	-	+
Performance	+	0	0	+

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The performance question

- What is performance of a reconfigurable system?
- A new set of performance metrics (throughput, latency, real-time capability, batch processing depth, ...) is required in addition to standard ones (accuracy, resolution, bandwidth, ...)
- Performance must always be associated with a firmware revision (new features, systematic error correction algorithms, ...)

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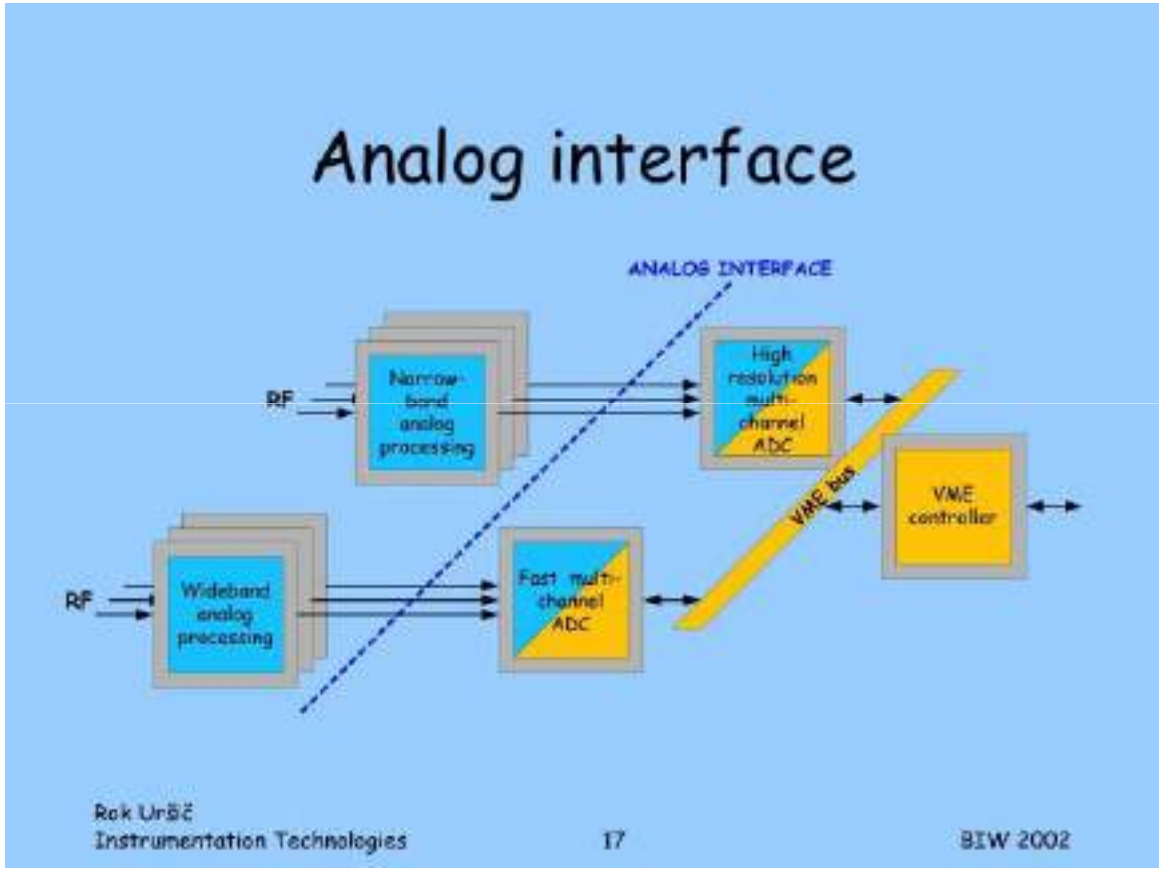
Analog interface
ANALOG INTERFACE
RF
Narrow-band analog processing
High resolution multi-channel ADC
VME bus
VME controller
RF
Wideband analog processing
Fast multi-channel ADC
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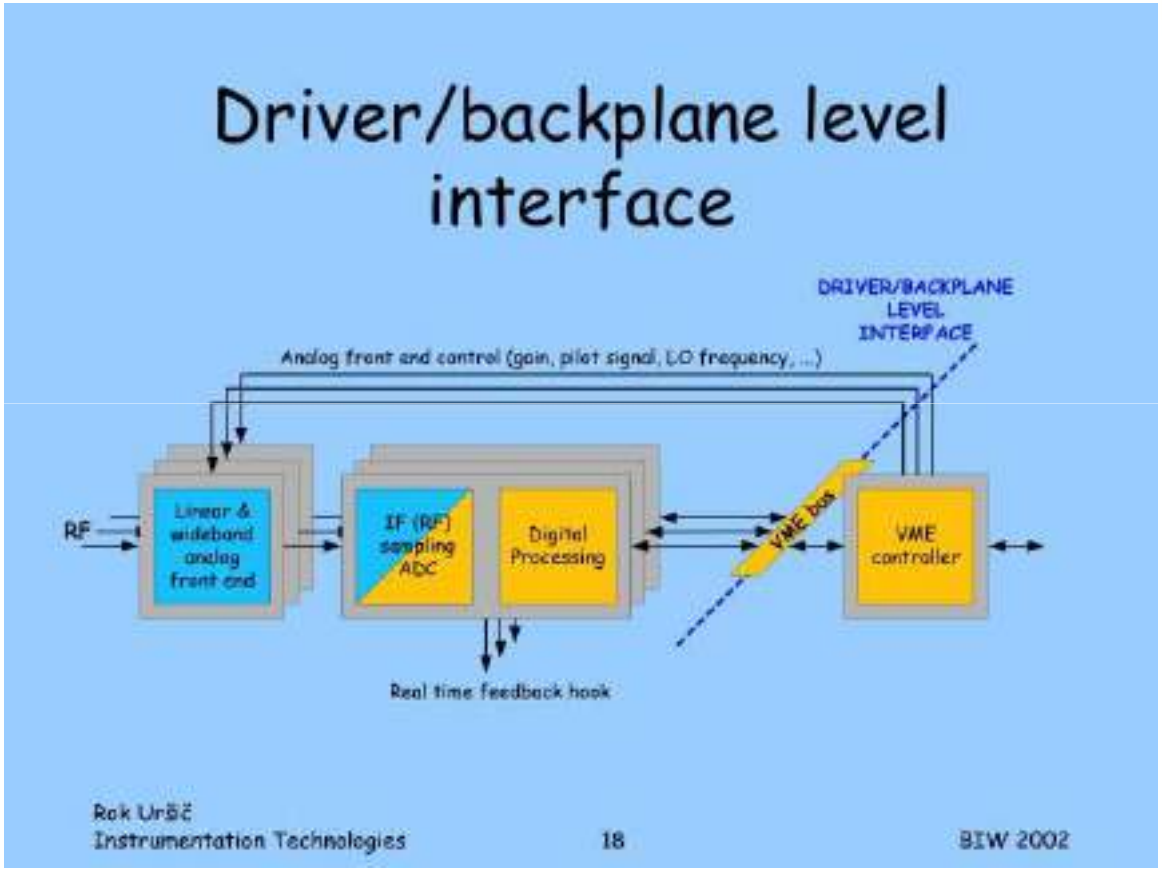
Driver/backplane level interface
DRIVER/BACKPLANE LEVEL INTERFACE
Analog front end control (gain, pilot signal, LO frequency, ...)
RF
Linear & wideband analog front end
IF (RF) sampling ADC
Digital Processing
VME bus
VME controller
Real time feedback hook
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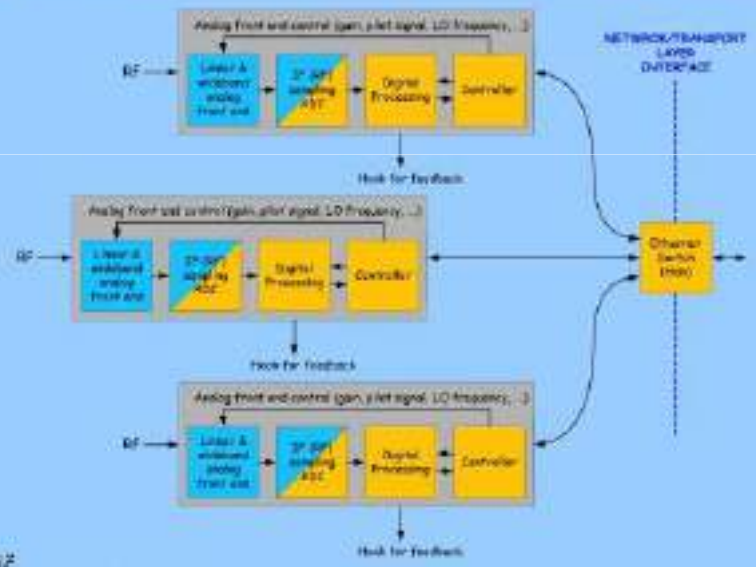
Network/transport layer interface - distributed



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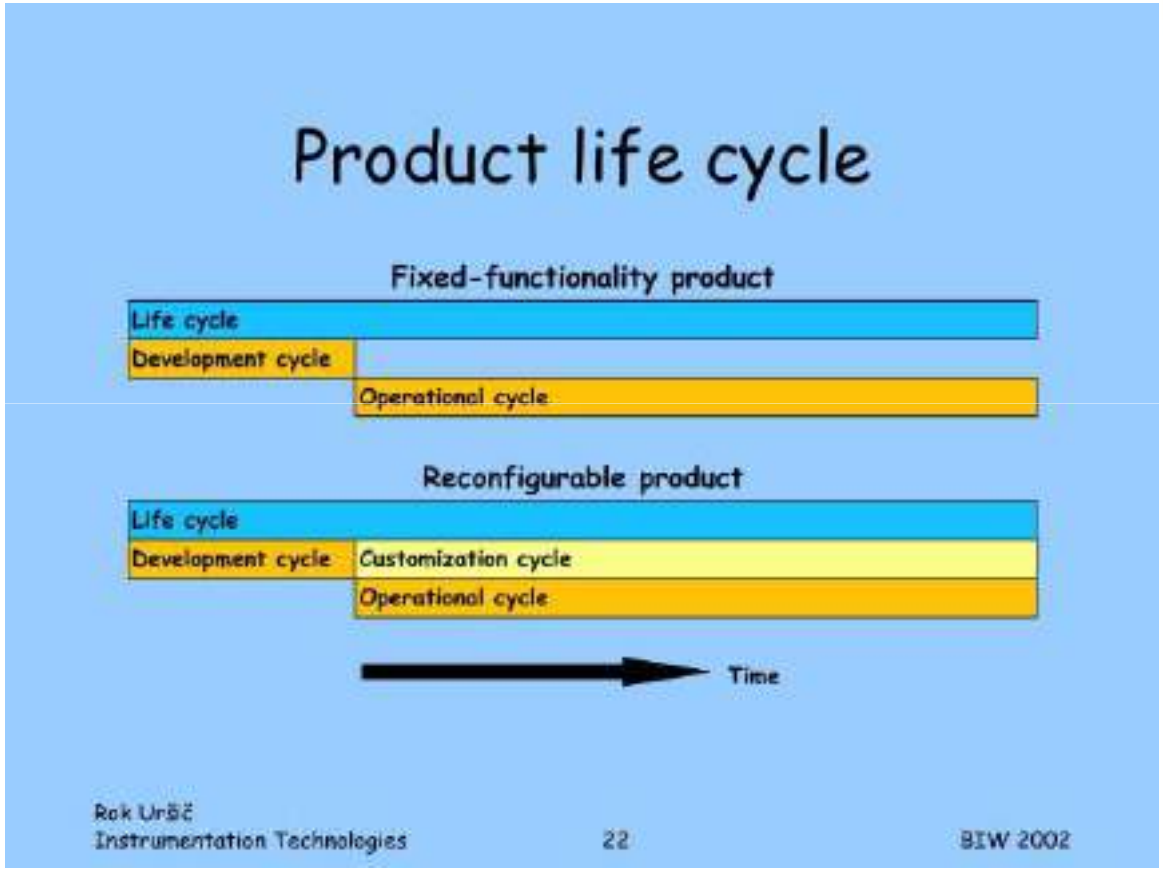
Product life cycle
Fixed-functionality product
Life cycle
Development cycle
Operational cycle
Reconfigurable product
Life cycle
Development cycle
Customization cycle
Operational cycle
Time
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2003: Launching Libera

Reconfigurability (customization) technology: we decided for FPGA

Launch customers (enablers!)

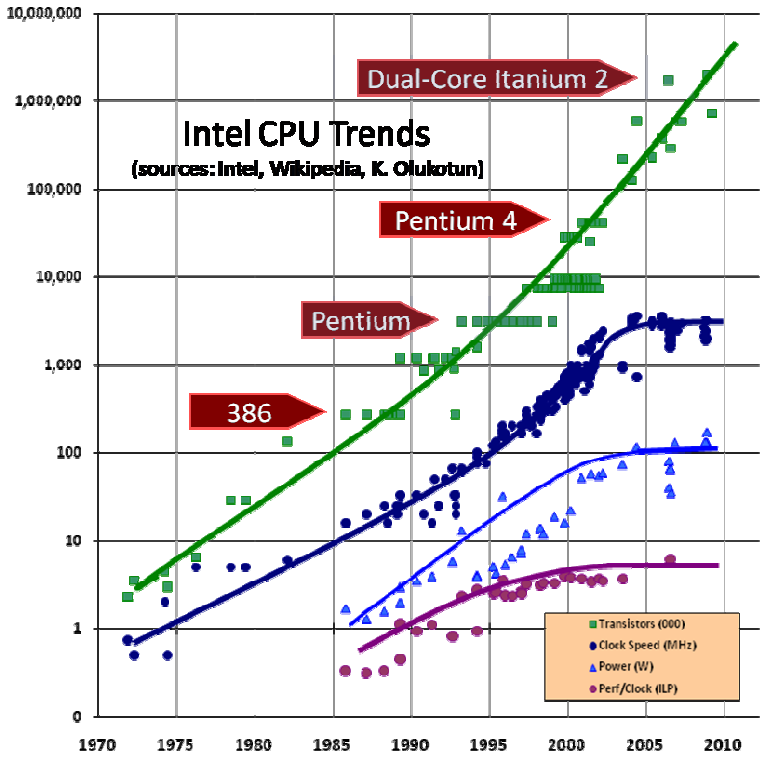
- Soleil
- Diamond
- Blood, Sweat and Tears – thank you for your patience!

2013: Some Trends

- Moore’s Law
- PLD (Programmable Logic Devices) Landscape
- CPU vs. GPU vs. FPGA
- FPGA Combos
- FPRF - Field Programmable RF

Moore's Law

The Free Lunch Is Over
A Fundamental Turn
Toward Concurrency in
Software (2005)
By Herb Sutter



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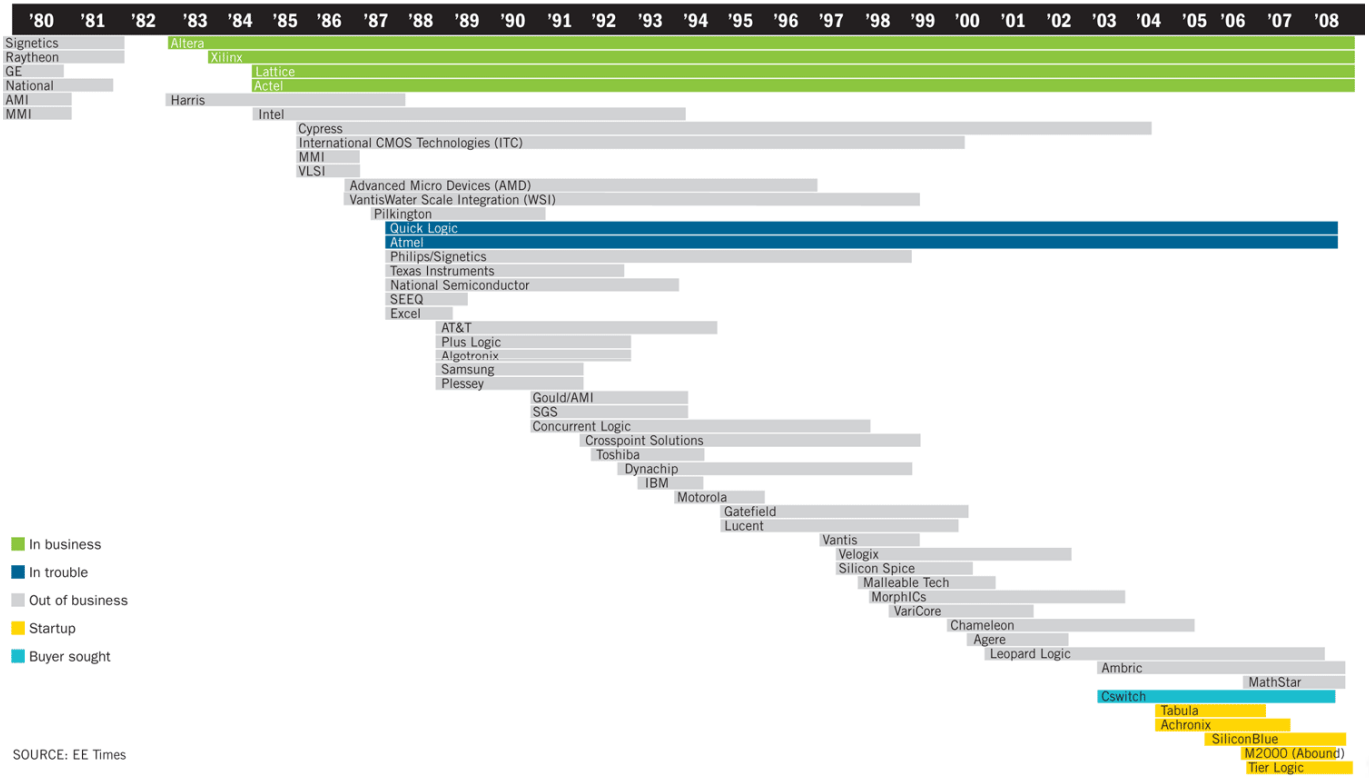
History of PLD startups



SOURCE: EE Times

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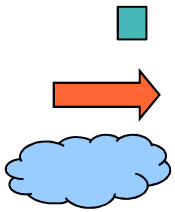
Types of data processing

Large batch, low repetition rate (high-latency, non-real-time)

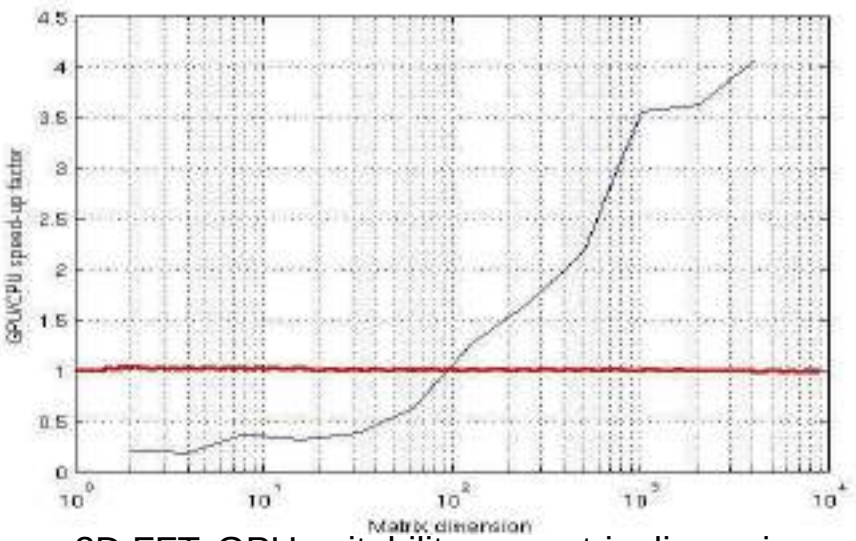
Small batch, high repetition rate (low-latency, real-time)



Data

Transport

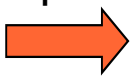
Processing (CPU, CPU+GPU or FPGA)



2D FFT: GPU suitability vs. matrix dimension

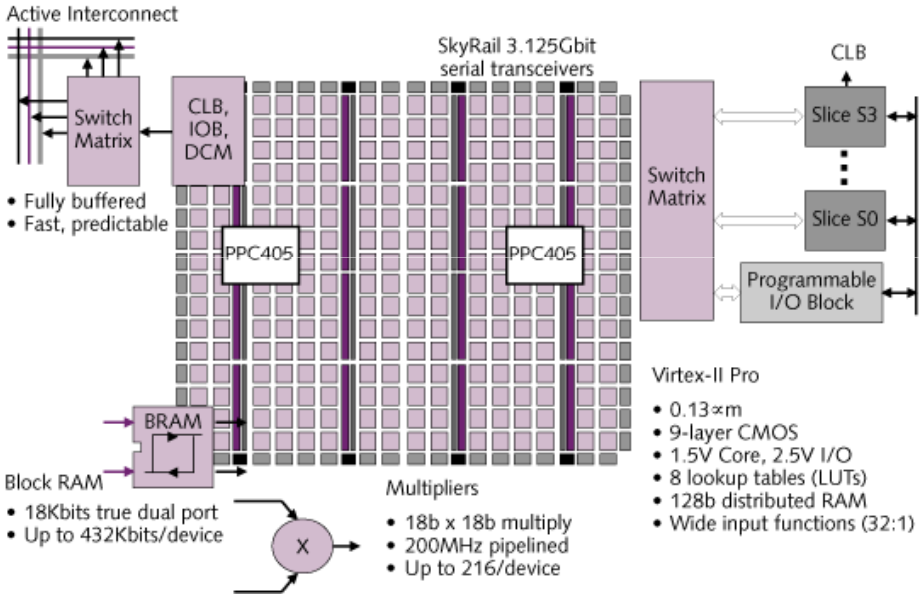
Courtesy Aleš Bardorfer

CPU, GPU & FPGA compared

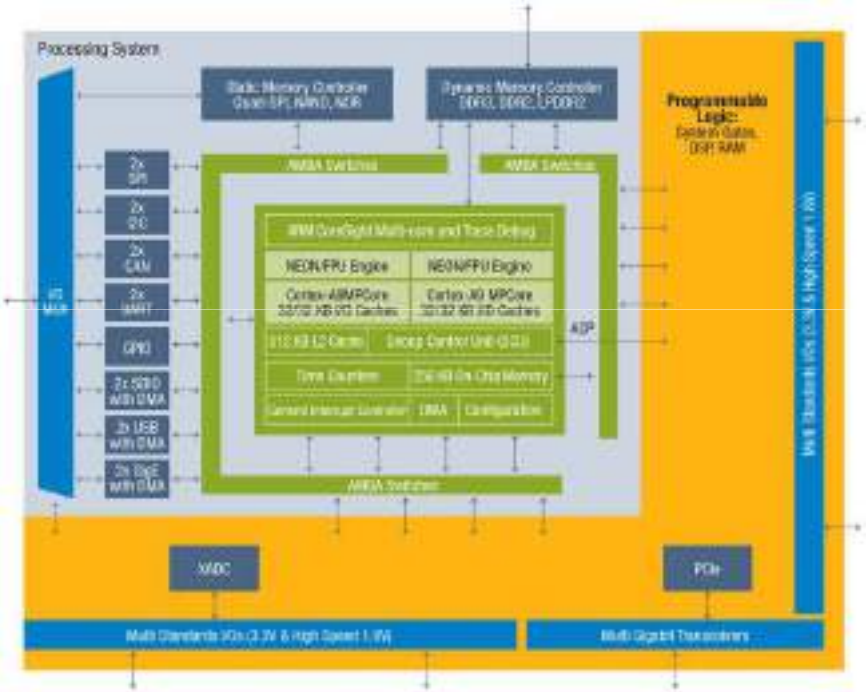
	Transport delay 	Processing power 
CPU	Large	Low
CPU+GPU	Large	High
FPGA	Small	High

Courtesy Aleš Bardorfer

FPGA / MCU combo vs. MCU / FPGA combo



Xilinx™ Virtex™ II Pro



Xilinx™ Zynq™ 7000

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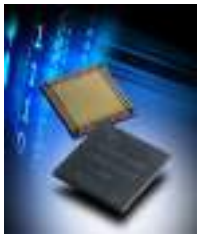
Example of FPRF (Field Programmable RF)



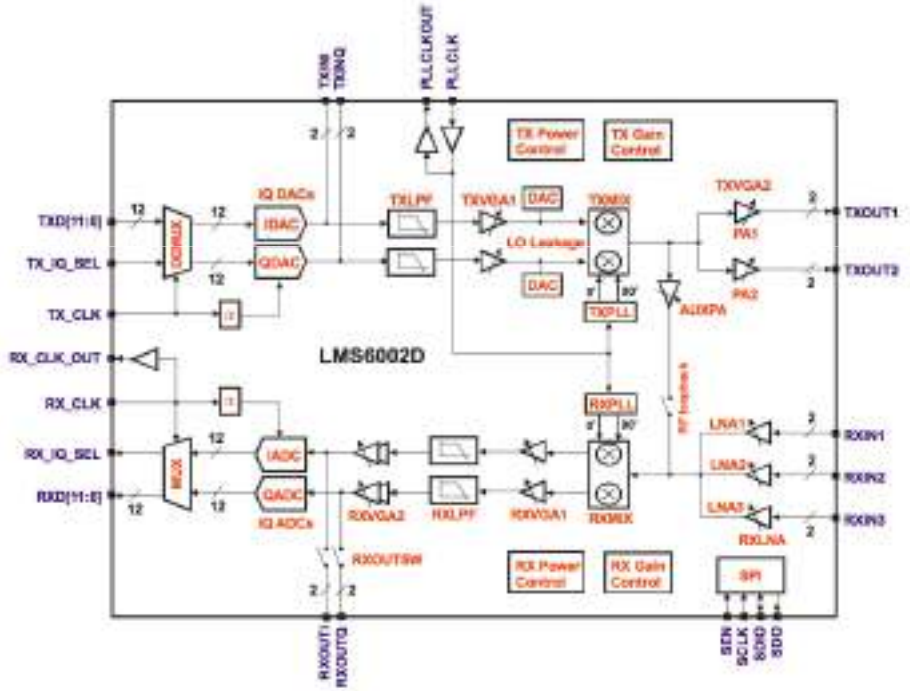


Figure 1: Functional block diagram

LMS6002D by Lime Microsystems

- Single chip transceiver covering 0.3-3.8GHz frequency range
- Digital interface to baseband with integrated 12 bit D/A and A/D converters
- Fully differential baseband signals
- Few external components
- Programmable modulation bandwidth: 1.5 to 28MHz

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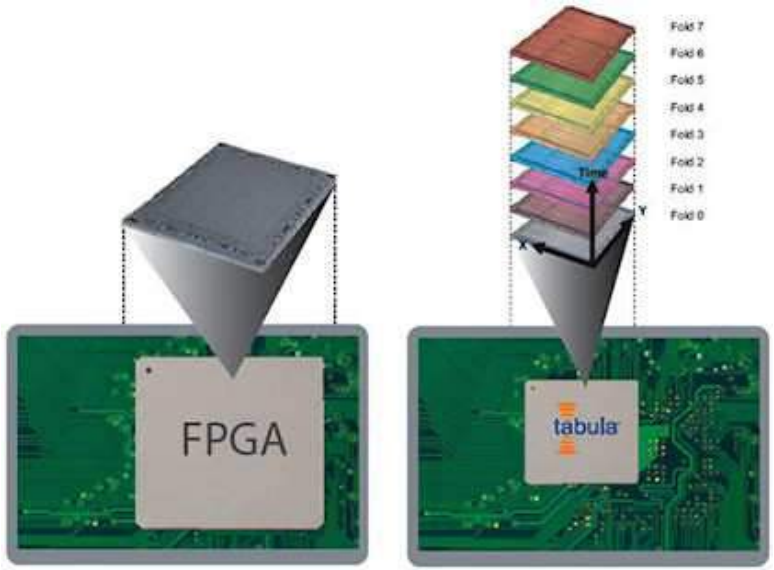
3PLD – Tabula



Tabula's Spacetime™ technology enables a new category of programmable logic device - 3PLD - that is freed from the limitations of FPGA's 2D topologies by using time as a third dimension to create a 3D device.

Summary

- Good RF design is the enabler for high performance
- Good system design extends reconfigurable instrument life-cycle
- FPGAs remain preferred choice for reconfigurable instrumentation
- New MCU/FPGA combos seem an attractive option for high perfromance as well as compact solutions
- Availability of quality tools remains critical
- Moore's Law -> lower cost -> availability of free tools -> wider acceptance of FPGAs
- There are some interesting new reconfigurable technologies to be watched

Thank you for trusting our company.