Presentation with Live Demonstration
Libera GB Ethernet Interface

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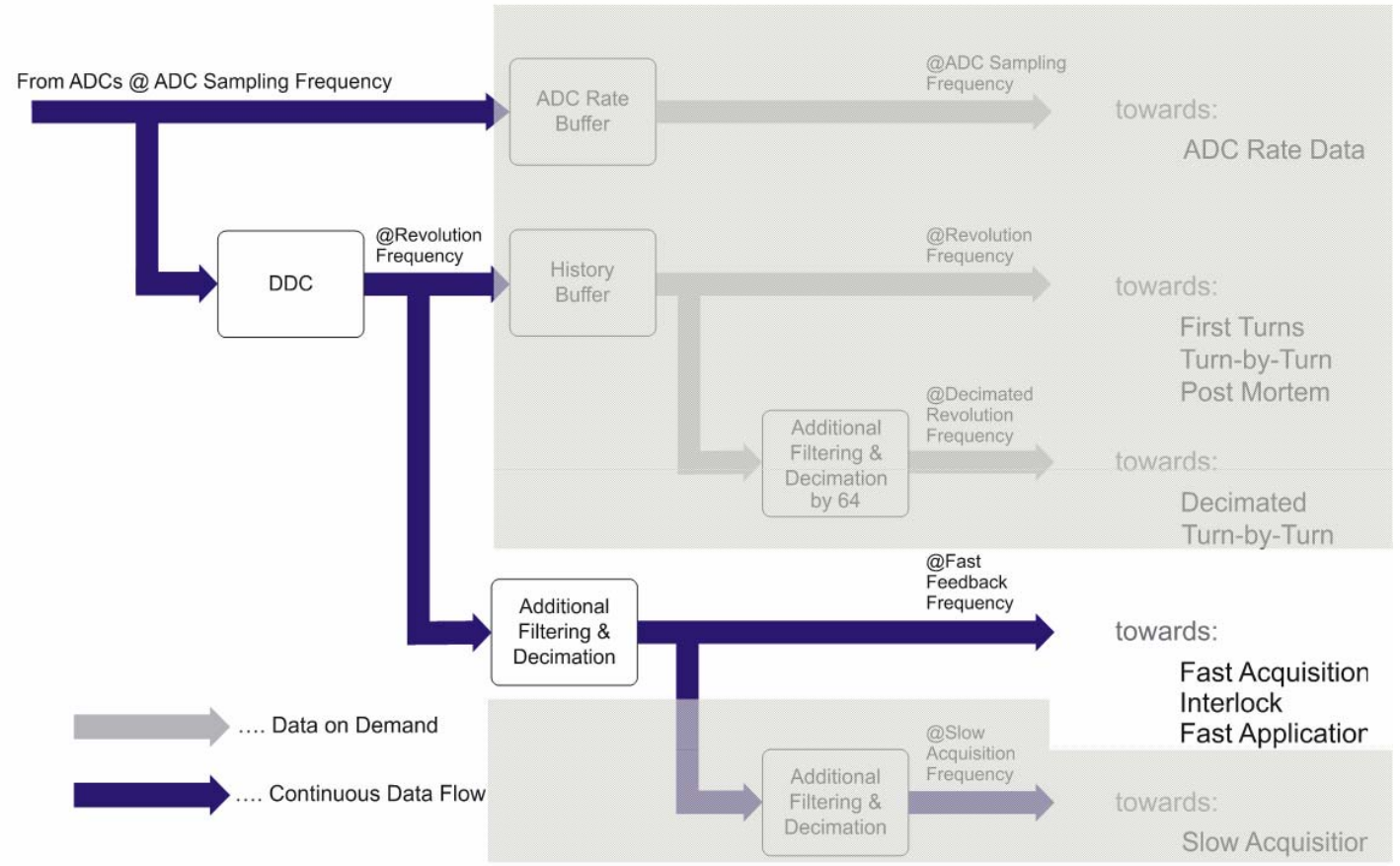
Introduction

- **Libera development followed the needs of accelerators during their lifetime:**
  - **First the Turn by Turn data was available for the commissioning needs.**
  - **The Slow Acquisition data followed for slow monitoring of beam movements.**
  - **In addition, ADC rate data and decimated Turn by Turn data were offered to the user community.**
  - **All these are available as a Libera standard feature.**
  - **FA data flow was there, but the users couldn't use it regularly as they didn't have regular access.**
  - **The decision to offer as standard solution as possible was inevitable.**

Fast Acquisition Data Flow



Properties of FA Data Flow

- It is continuous
- It must be predictable in time
- It must be possible to synchronize it with the flow on other Liberas
- It must have low latency
- It requires predictable, low latency, dedicated type of connection and protocol

Which Protocol to Choose?

- Various protocols and hardware communication layers are possible with Libera thanks to FPGA programmable hardware and pluggable SFP modules.
- Different ways of building Fast Feedback application were proposed, some of them being partially implemented on FPGA within Libera beside main Libera FPGA design.

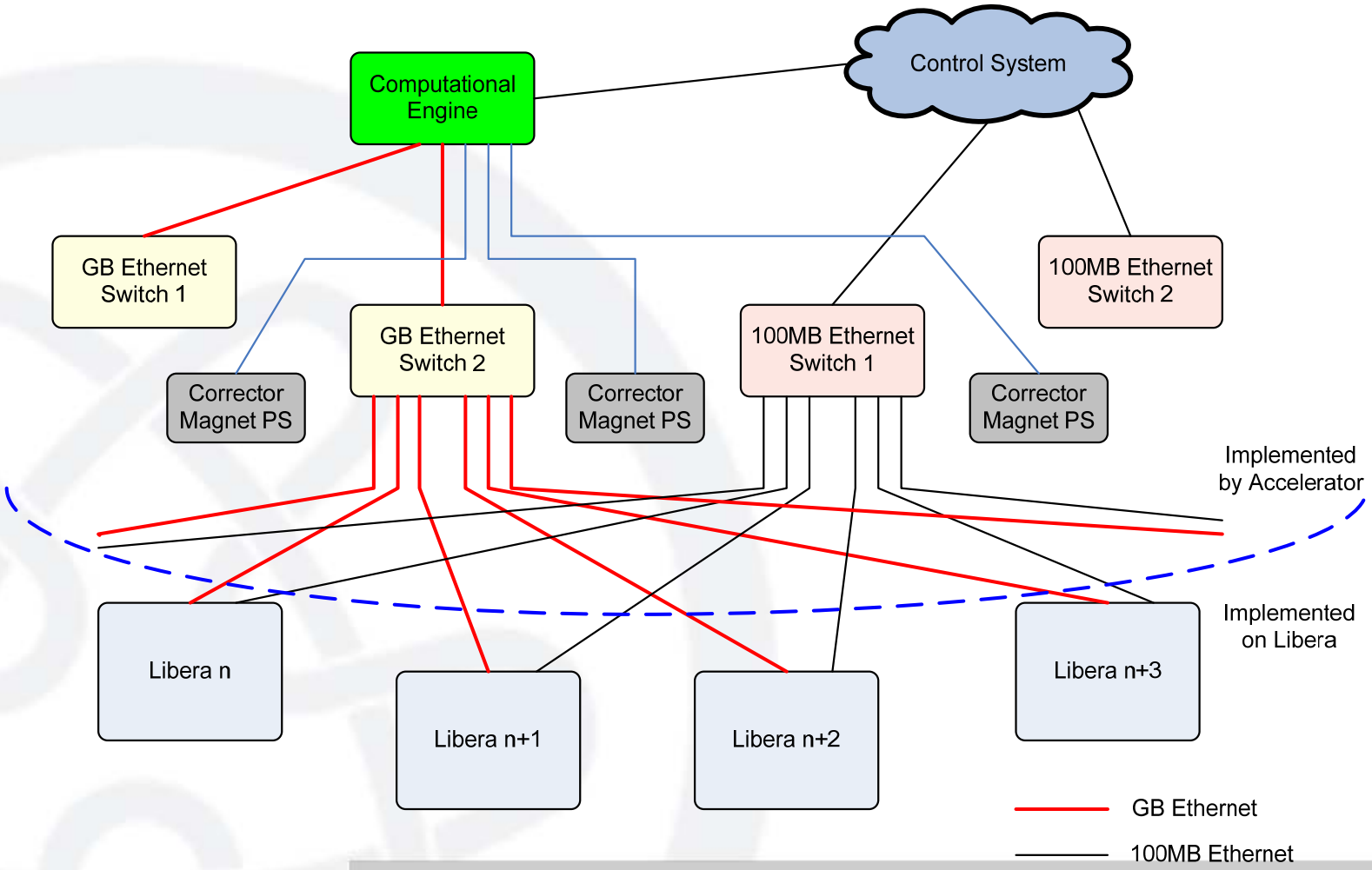
GB Ethernet

- Gigabit Ethernet protocol is well accepted and used in every day life.
- The solution is completely standardized.
- There is a lot of dedicated equipment, switches for example. Almost every new PC has the GB Ethernet port built in.
- The choice of GB Ethernet protocol was then not so difficult at the end.

Main Properties

- The solution is kept as simple as possible.
- The data flow is unidirectional. The FACQ data is simply transmitted from the Liberas.
- Liberas can be synchronized to the +- 1 sampling clock accuracy so they all can deliver the FACQ packets synchronously.

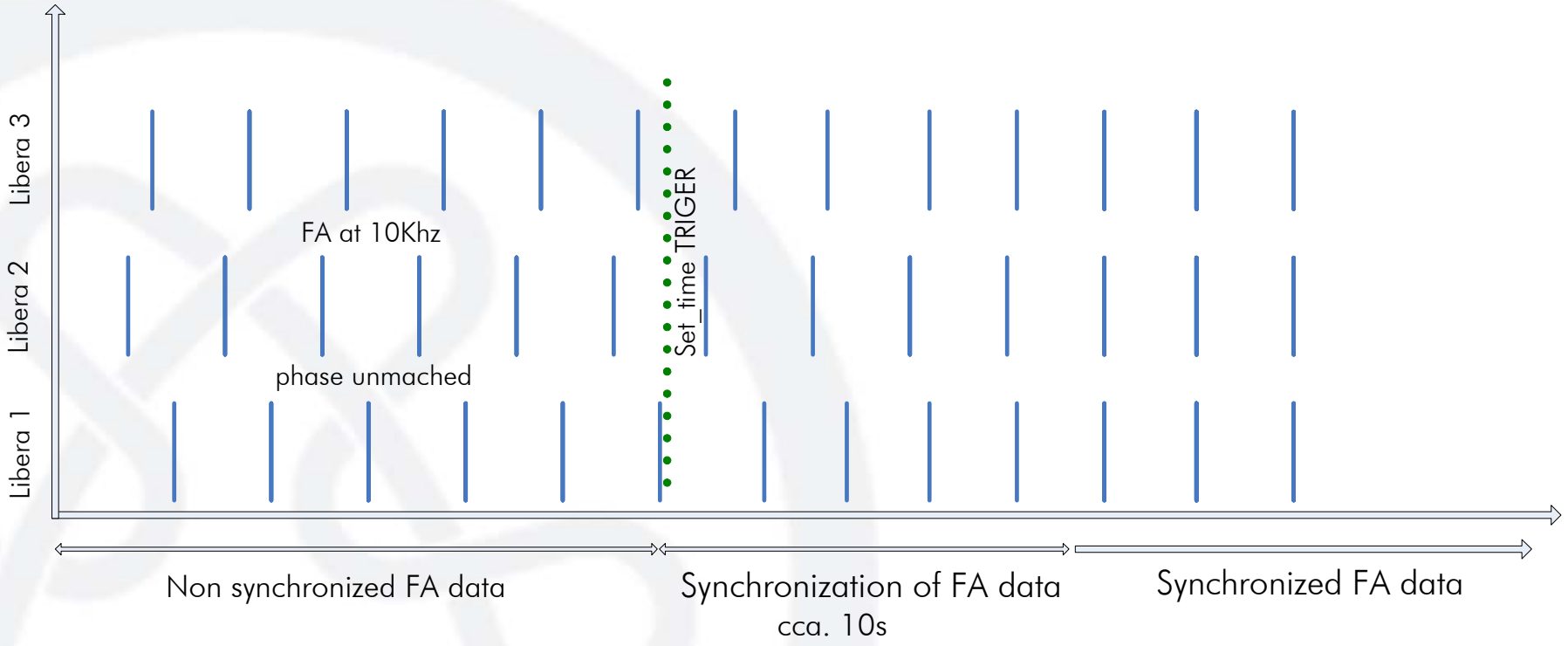
Possible Usage



Synchronization, 1

- Synchronization of the FA data (@10kHz) on set_time trigger.
- 16bit counter is enclosed in the GB Ethernet packet. On synchronization it is resetted.
- Synchronization performed by PLL, clocking the VCXO. More on next slide.
- Synchronization is completed in less than 10seconds after set_time trigger.

Synchronization, 2



Electrical and Physical Interface

Property	Value	Remarks
Communication speed	1000Mbps	10 and 100 Mbps not supported
Auto-negotiation	Required	Physical connection required at boot time
SFP module	SGMII compatible module required	Copper or optical
Copper communication media	Cat-5e cables or better	According to the IEEE802.3ab;
Number of GB Ethernet ports	1	

Communication Protocol Properties

Property	Value	Remarks
Communication direction	Unidirectional, out from Libera	10 and 100 Mbps not supported
Default Packet type	UDP over IP	
Frame	IEEE 802.3 Frame Format	According to the IEEE802.3ab;
Collision detection	None	Intended for use with "level 2" or "level 3" switches
Packet size (data)	Fixed size, maximum 100 bytes	
Source and destination MAC	2 x 6 bytes	Boot-time configurable
Source and destination IP numbers	2 x 4 bytes	Boot-time configurable
Source and destination port numbers	2 x 2 bytes	Boot-time configurable

Fast Application Data Delivery Properties

Property	Value	Remarks
Default and maximum FACQ packet content	4 x V, Sum, Q, X, Y	Data order same as order of appearance at the FA, all of them 32-bit
	Libera status bitmask (ADC overflow, interlock status)	Max 16-bits
	16-bit packet counter	Reset to 0 at set_time() trigger
Stop packet transmission	Through external HW trigger or SW command	Configurable through CSPI
Start packet transmission	Through external HW trigger or SW command	Configurable through CSPI
Latency between first data available at FA and the start of transmission	Less than 0.5 μs	

Deliverables

- FPGA firmware integrated transmit-only GB Ethernet core.
- FPGA firmware integrated wrapper that passes FA data to GB Ethernet core and implements GB Ethernet core configuration space.
- Driver and CSPI integrated support for GB Ethernet core.
- A sample program for GB Ethernet core configuration (binary and source).
- A demo program to receive the Libera transmitted data on a Linux or Windows PC fitted with GB Ethernet port.

Current Status

- Development Release has been released to Libera GB Ethernet launch customers (Elettra, NSRRC).
- GB Ethernet data flow from Libera is stable and well tested in house.
- It is being tested on Elettra.
- Demo version with time-limited (8 hours) GB Ethernet data flow will be enclosed in regular sw Release 1.40 in December 2006.