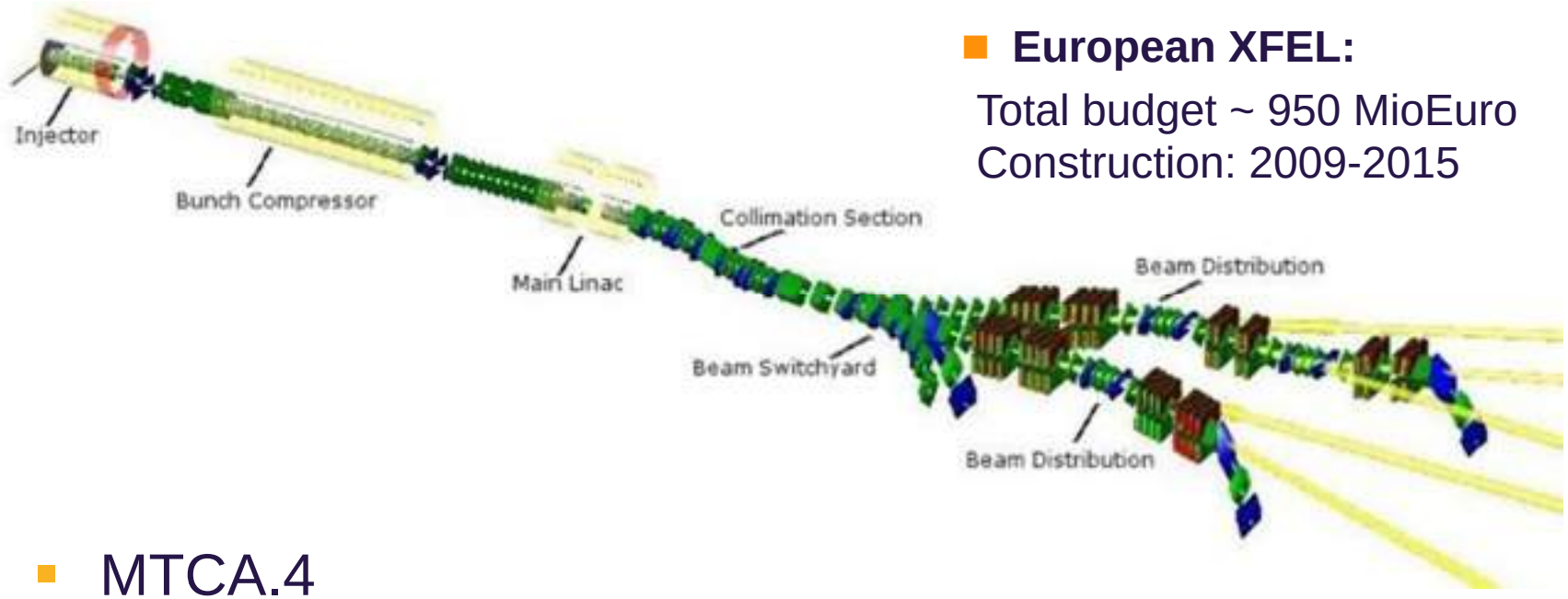
# Recent developments on MTCA.4

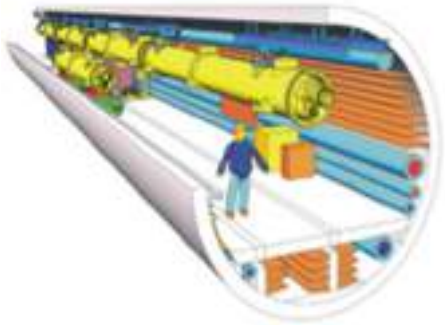
Dr. Frank Ludwig - DESY
for the LLRF Team

# Outline




- **European XFEL:**
  Total budget ~ 950 MioEuro
  Construction: 2009-2015

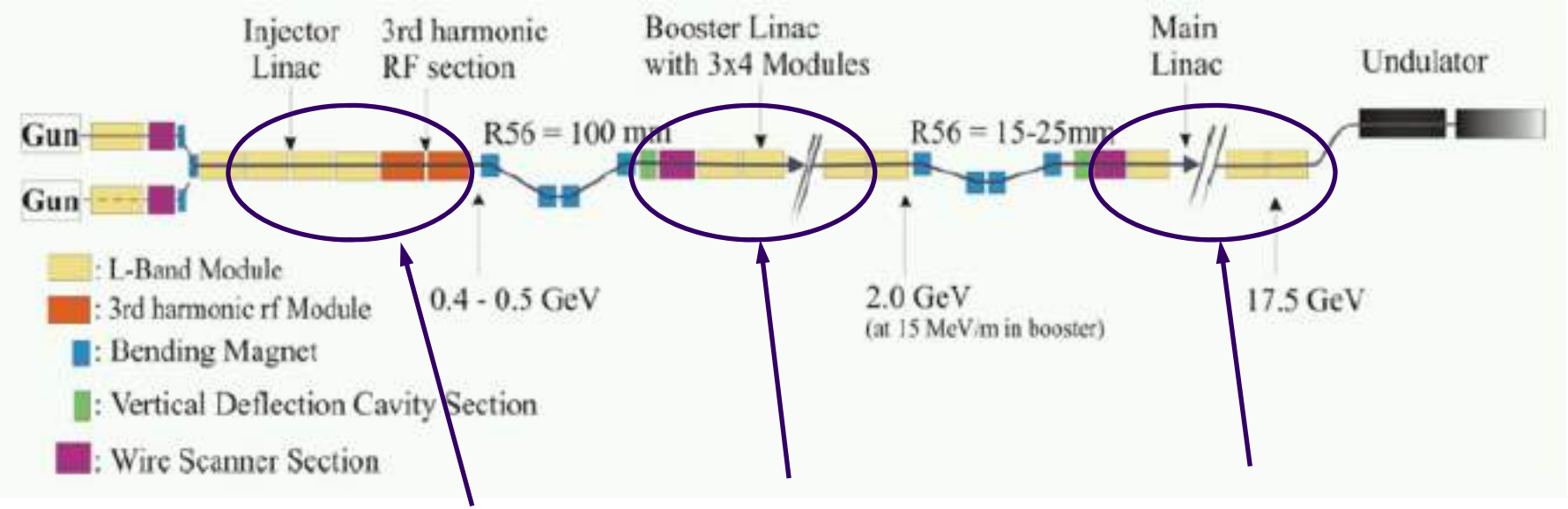
- MTCA.4
- LLRF System in MTCA.4
- Applications and Recent Developments
- MTCA.4 for Industry
- Outlook



# Motivation



- **Requirements for the cavity field stability (long- and short-term) :**




Amplitude and Phase stability :

$f_{CAV} = 1.3GHz$

$\Delta A / A_{rms} = 0.01\%, \quad \Delta\varphi_{rms} = 0.01\ deg$

$\Delta A / A_{rms} = 0.03\%, \quad \Delta\varphi_{rms} = 0.03\ deg$

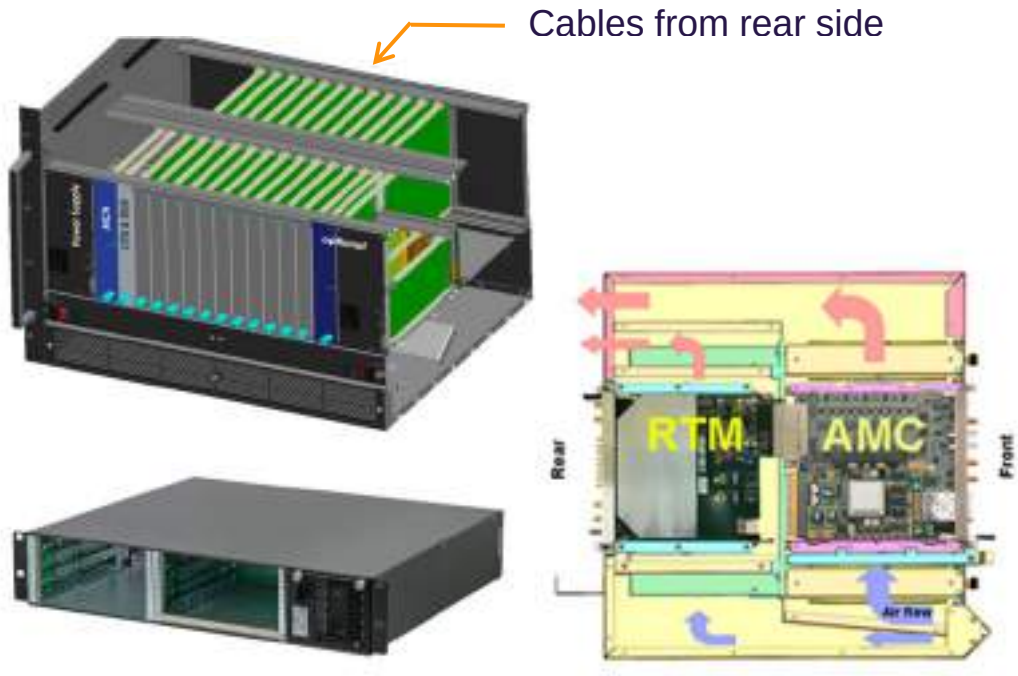
$\Delta A / A_{rms} = 0.1\%, \quad \Delta\varphi_{rms} = 0.1\ deg$

- Review meeting 12.2007: XFEL will be based on xTCA
- XFEL fast electronics will be based on **MTCA.4**: > 200 Crates

# MTCA.4 Crate Standard



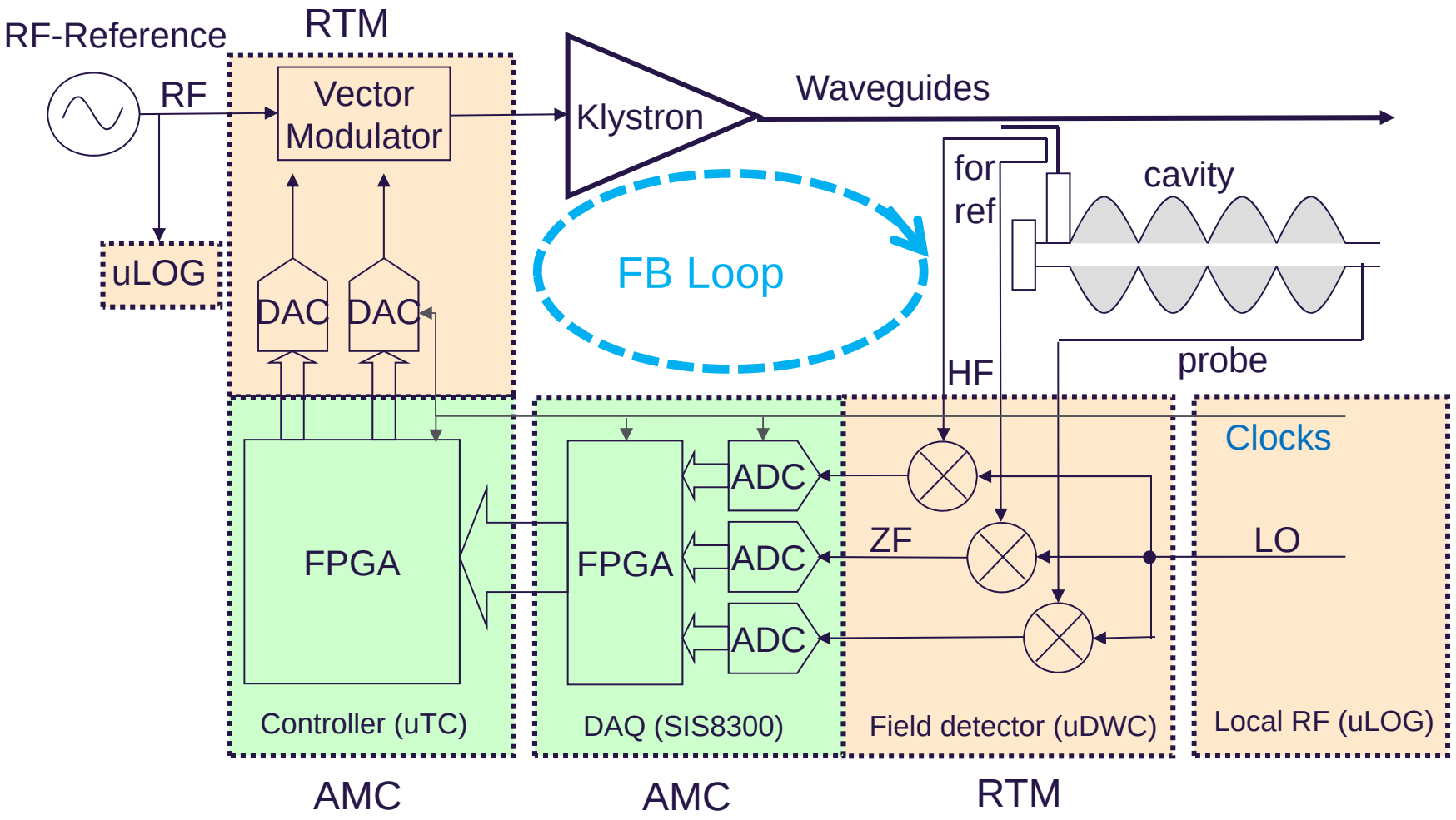
- Development partnership *„xTCA for Physics“* (38 partner): 03/2009
  - **Research Institute**: SLAC, FNAL, IHEP, IPFN, ITER, DESY
  - **Industry:** Connector-, Board-, Crate-, System Manufacturer
- Ratification PICMG 2011 (http://www.picmg.org)
  - **M**icro **T**elecommunications **C**omputing **A**rchitecture .4 (MTCA.4)




- **Modular + modern architecture**
  - Reusability + PCIe + Ethernet
- **High availability**
  - Redundant power and fan optional
  - Well defined remote management
- **High digital performance**
  - Very low analog distortions
  - 4 lanes PCIe: 400 MB/s ... 3.2 GB/s

# Modular LLRF System in MTCA.4

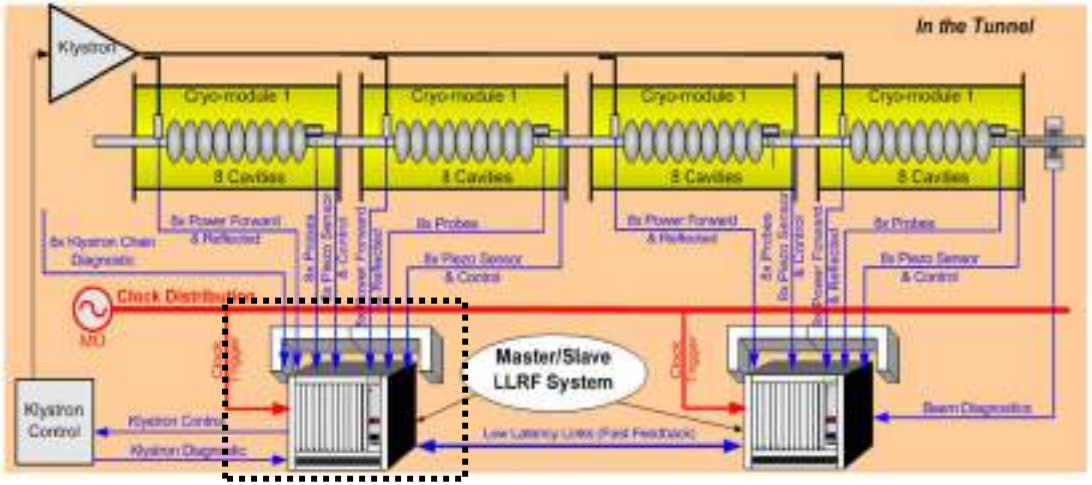
- **High frequency regulation (simplified) :**

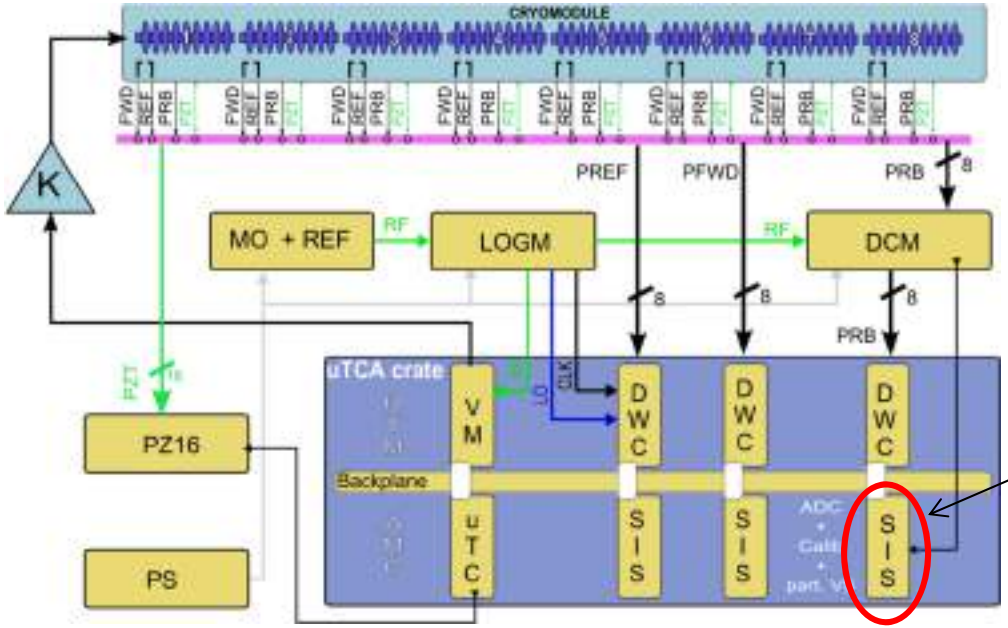


# LLRF System in MTCA.4

FIL

Subversions for:
- Injector linac
- Third harmonic
- NC structures
- Booster, main linac



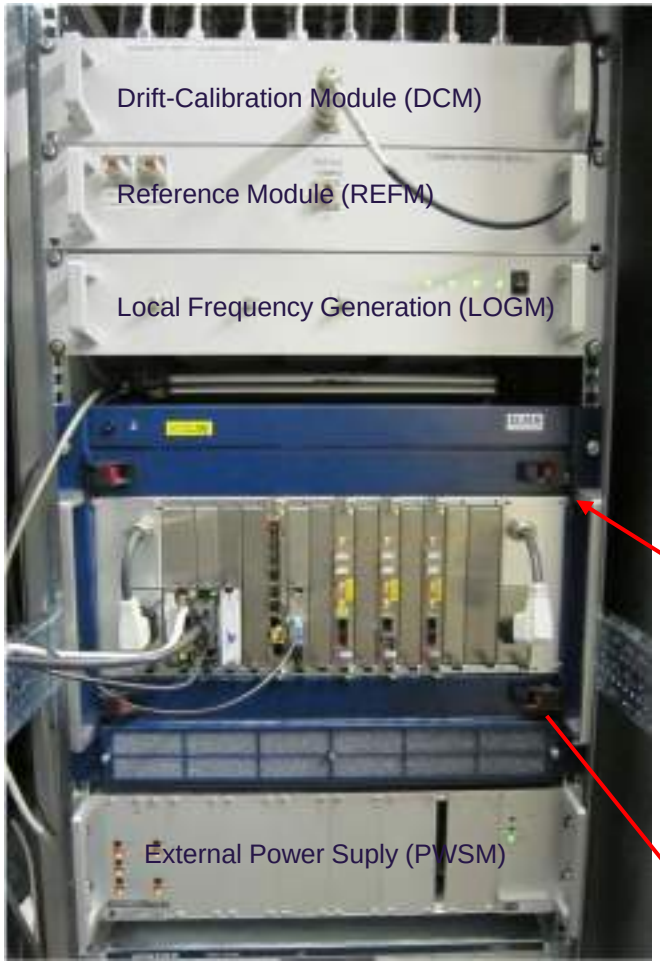




ADC board for readout of:
- Probe signals
- Forward signals
- Reflected signals
- ….
- Control DCM / DWC

Courtesy of J.Branlard

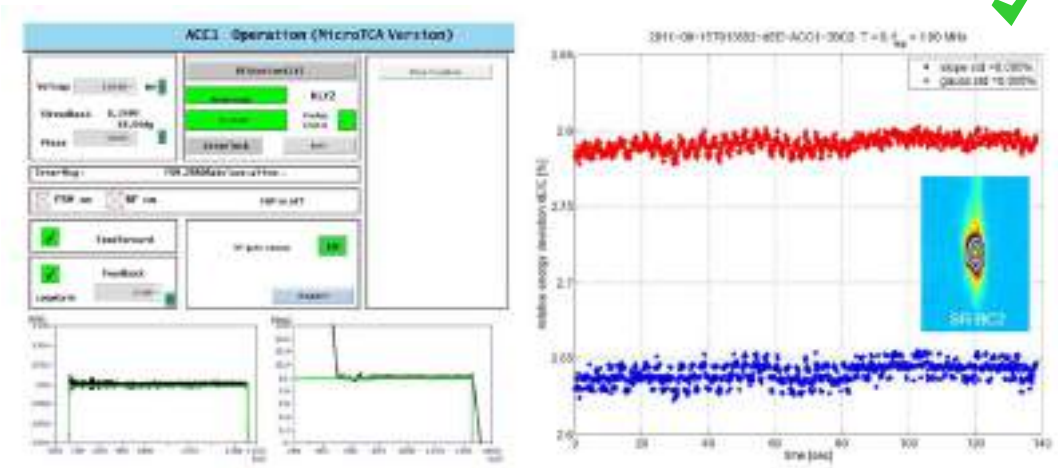
# FLASH injector prototype system

## MTCA.4 Prototype System




## LLRF Systemperformance Test

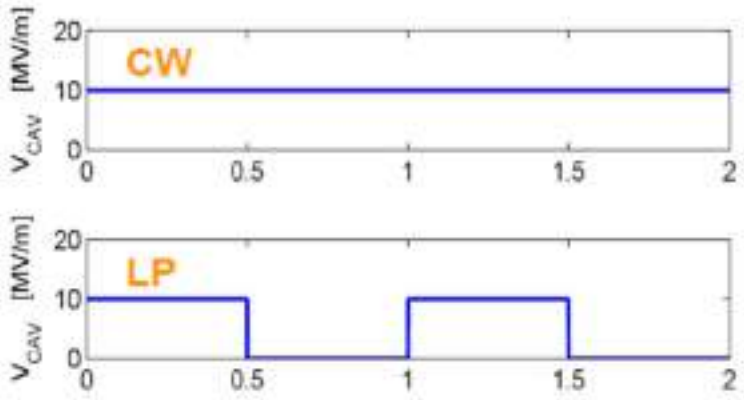
Measured shot-to-shot beam energy stability at SR-3BC2 of 0.005% (rms)




- LLRF AMC and
- RTM Modules

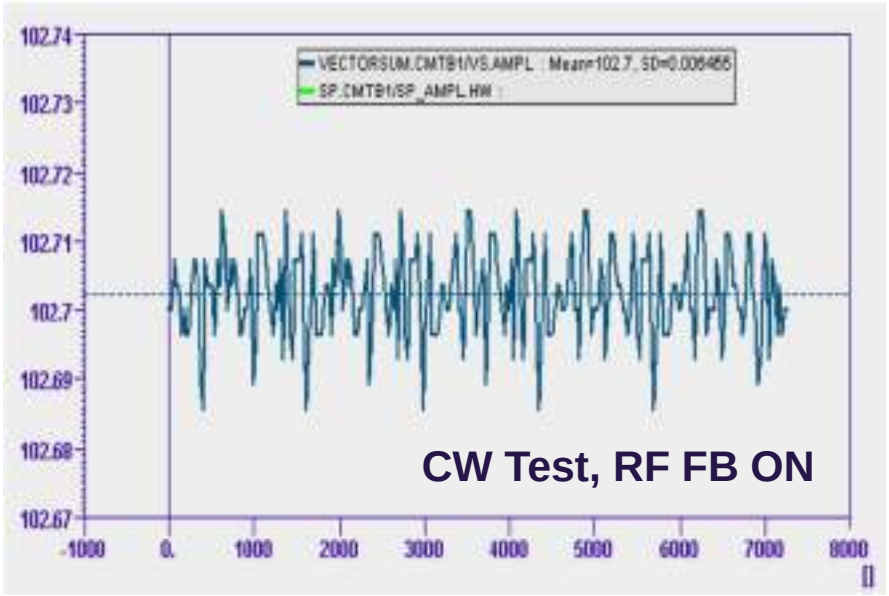
# Other Facilities operating MTCA.4 Systems

- **CMTB (Cyro Modul Test Bench) :** - CW and Long-Pulsed test
  - Full MTCA.4 crate occupation test




- Operations at 3MV/m

Standard deviations : (in-loop)
- dA/A = **6.2 x $10^{-5}$**
- dPhase = **0.0098°**

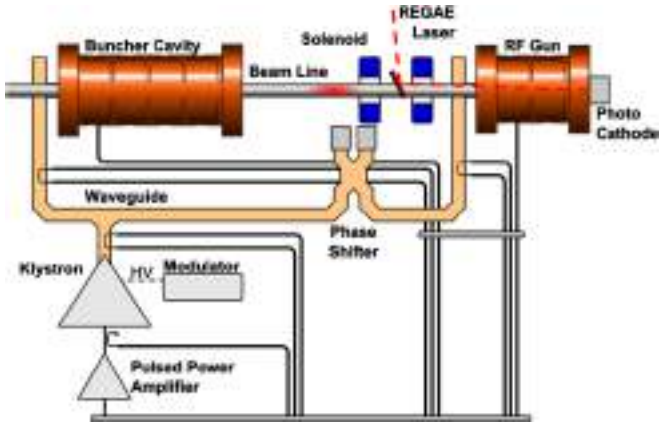


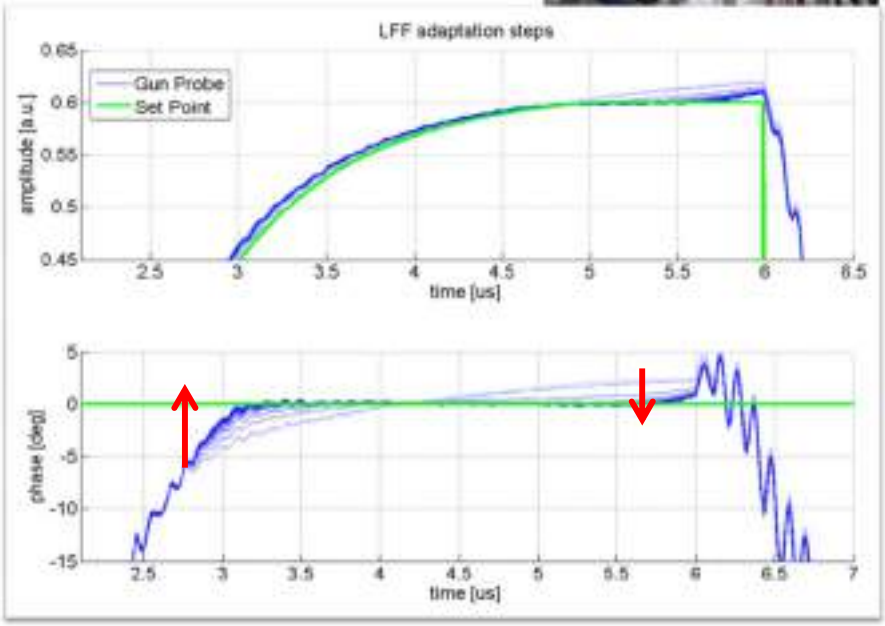

Courtesy of J.Branlard

# Other Facilities operating MTCA.4 Systems

- **REGAE (Relativistic Electron Gun for Atomic Exploration) :**
  - Electron source for time resolved diffraction experiments

- **3GHz LLRF system based on MTCA.4:**
  - Buncher Cavity and RF-Gun S-Band, NC
  - 10 channel process Kly/Gun/Buncher/Laser
  - Non IQ IF=25MHz, fs=125MHz, LFF
  - dA/A~0.007% (rms), ✓
  - dPhi ~0.004 deg at cavity bandwidth

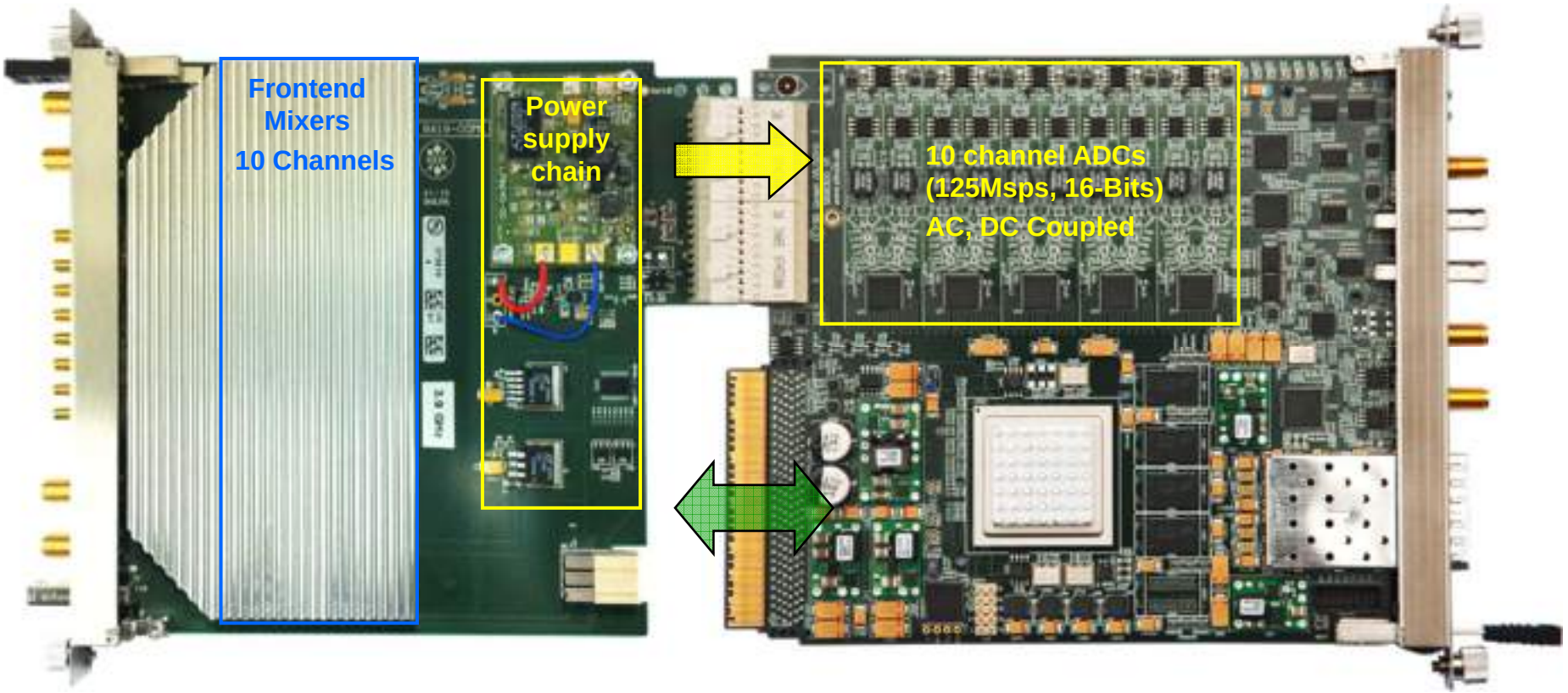



Courtesy of K. Flöttmann, M.Hoffmann

# Signal Conditioning and Digital Processing

- **High frequency Down-Converter (uDWC)**
  (License state -> Industry)
- **Multi-Channel fast ADC Digitizer (SIS)**
  (Industry redesign V5->V6 011/12)

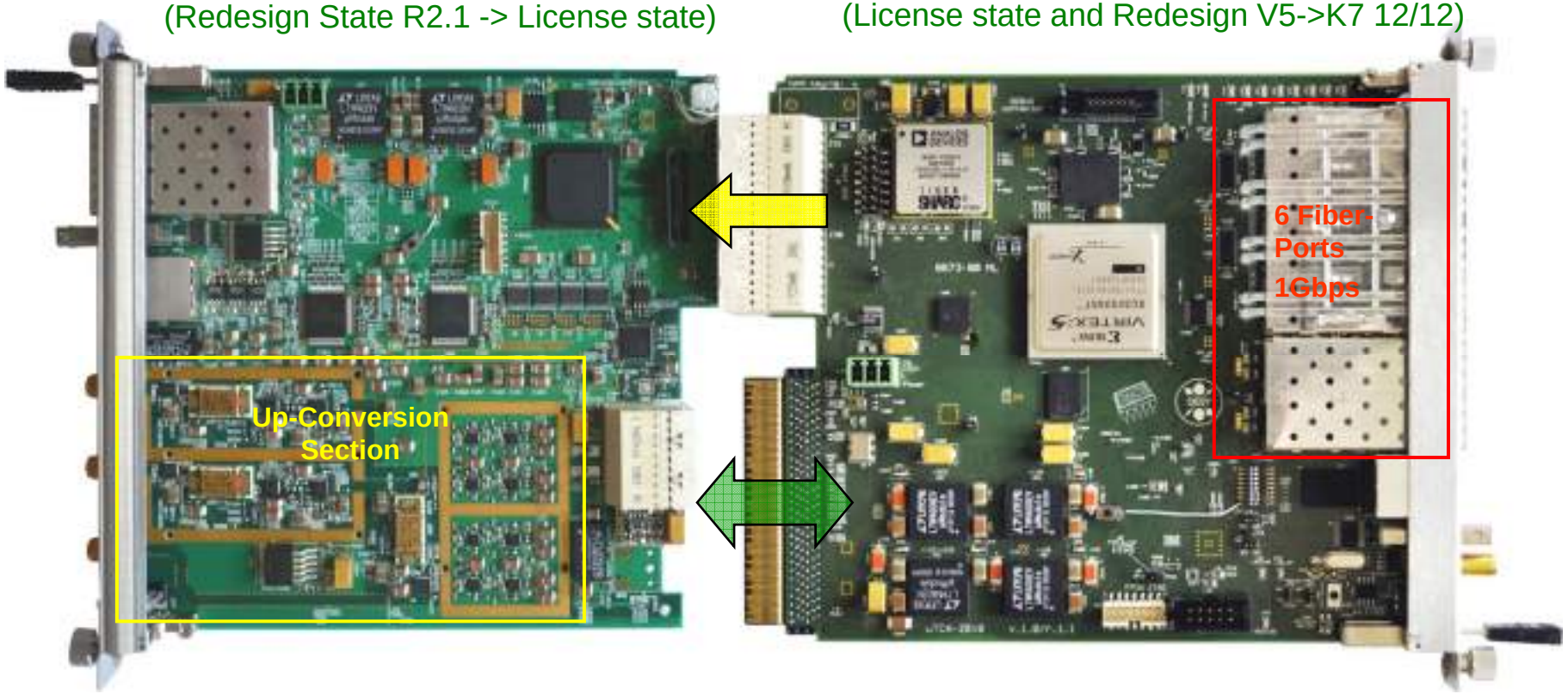



- 10 channel field detection
  (1.3GHz, …, 3.9GHz)
- Resolution, 0.003%, 0.003deg, < 10fs

- 10 channel ADCs (125Msps, 16-Bits)
- FPGA pre-processing partial cavity vector sum
- Low latency links via MTCA-backplane

# LLRF Controller and Klystron Driver

- **High frequency Klystron Driver (uVM)**
  (Redesign State R2.1 -> License state)
- **LLRF FPGA Controller (uTC)**
  (License state and Redesign V5->K7 12/12)




- 2 channel Vector Modulator (108MHz, 216MHz, 1.3GHz…3.9GHz)
- 16-bit DAC performance
- 2 Fiber-Ports, Standalone operation

- LLRF Controller, 6 Fiber-Ports, 8 GB-Links
- FPGA(Virtex5), DSP
- RJ45 communication port

# Controller V2.0 based on Xilinx K7

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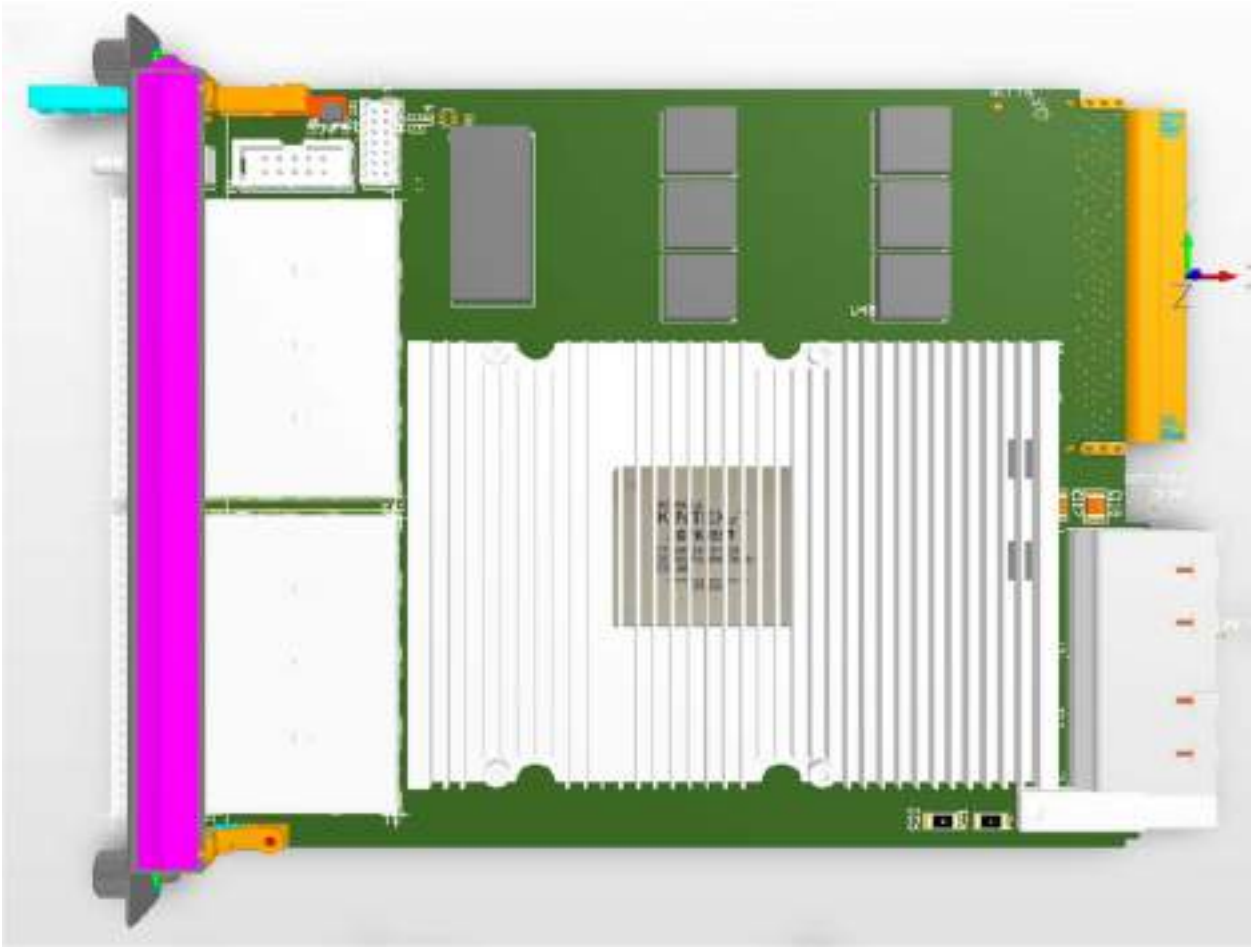
## Controller Performance (uTC)

- FPGA (Xilinx K7)
- DDR3 RAM, 4Gbit
- 8x SFP+ (Fiber Ports)
- 4 Low-Latency Links (AMC)
- 4 Low-Latency Links (Z3)
- 2 Low-Latency-Links / GbE
- 4 PCIe Links (AMC)
- IPMI, JTAG
- MTCA.4 compatible
- Z3 Class D1.2 compatible



(Expected in 02/13
-> License state)

# Modular LLRF SRF System in MTCA.4

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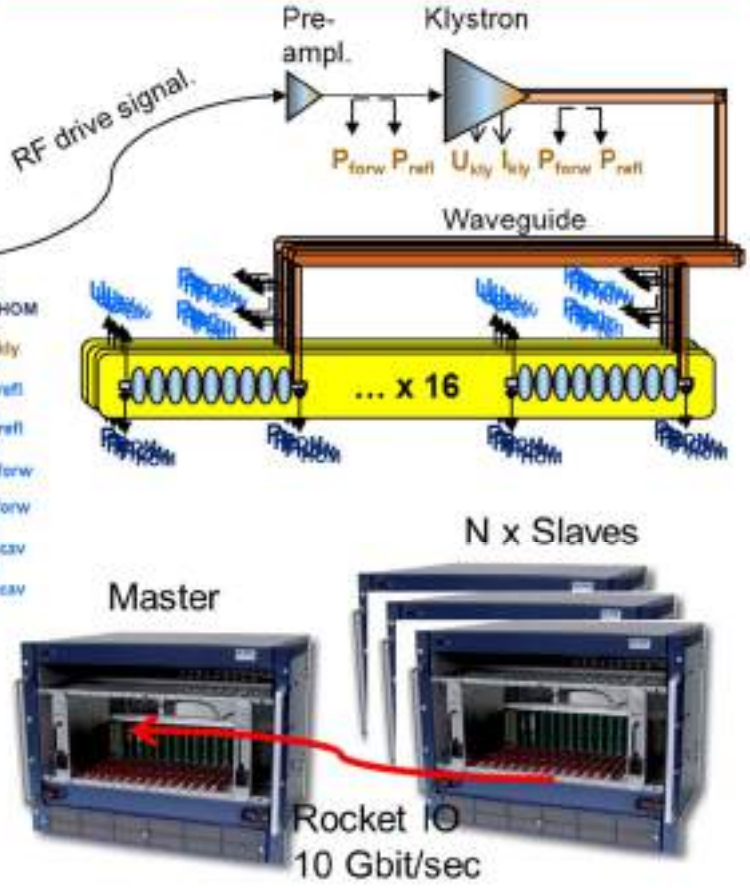
## MTCA.4 system configuration for:

**Pulsed N*16 cavity SRF system**
+ Ultra-fast klystron protection
+ HOM signal processing (2N-1)*8

| | AMC | RTM | |
|---|---|---|---|
| # -3 | PM 1 | Spare LNPM/HVPM | |
| # -2 | PM 2 | Spare LNPM/HVPM | |
| # -1 | MCH | MCH for RF backplane | |
| # 1 | CPU + HDD | Spare CPU/10GbE/GPU/... | |
| # 2 | FPGA V5 + Rad. Mon. | Machine Protection | |
| # 3 | Timing | Timing Distribution | |
| # 4 | Controller | Vector modulator | |
| # 5 | ADCs 8 x 800MSPS/12bit | 8 x Higher Order Modes | $P_{HOM}$ |
| # 6 | ADCs 8 x 800MSPS/12bit | Fast Klystron Protection | $P_{kly}$ |
| # 7 | ADCs 10 x 125MSPS/16bit | 10 x Down-converter | $P_{refl}$ |
| # 8 | ADCs 10 x 125MSPS/16bit | 10 x Down-converter | $P_{refl}$ |
| # 9 | ADCs 10 x 125MSPS/16bit | 10 x Down-converter | $P_{forw}$ |
| #10 | ADCs 10 x 125MSPS/16bit | 10 x Down-converter | $P_{forw}$ |
| #11 | ADCs 10 x 125MSPS/16bit | 10 x Down-converter | $U_{cav}$ |
| #12 | ADCs 10 x 125MSPS/16bit | 10 x Down-converter | $U_{cav}$ |
| #13 | MCH spare | Spare Ext. synchr.. / MO | |
| #14 | PM 3 | Local Oscillator Generator | |
| #15 | PM 4 | Local Oscillator Generator | |

AMC Backplane / RTM Backplane




Courtesy of H.Schlarb

# Available digital AMC's and RTM's

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RTM

- Machine Protection System (DESY)

- ADC and DAC (DESY)
  - 8 ch ADC 95 MSPS, 16bit
  - 4 ch DAC 16 MSPS, 16bit

- Test RTM

- Coupler Interlocks
- Beam Loss Monitors
- Toroid protection / readout
- Wire Scanner
- Clock & Trigger Contr. for Exp.

AMC

- AM90x (Concurrent)
  - Core i7, 16GB DDR3
  - x8 PCIe (Gen1,2,3)
  - SSD support

- DAMC2 (DESY)
  - Xilinx Virtex 5
  - FMC carrier
  - 4 SFPs

(100 pcs production)

- TAMC651 (TEWS)
  - Spartan 6
  - 1 SFP

- Module carrier

IP: - TAM100/200 (Tews)
- AMC703 (Hytec)

PMC: - PMC AMT (NAT)
- TAMC260 (Tews)

FMC: - TAMC631/640/641

IO: - ADIO24 A/D IO (ESD)

# Available analog AMC's and RTM's

FIL

- Down-Converter (DESY)
  1.3 - 4GHz
- 2 ch APD Pulse Stretcher (DESY)
- BPM (DESY)
- SIS8900 (Struck)
  LEMO Adapter Board

RTM

AMC

- SIS8300 (Struck)
  ADC Digitizer
  - 10 channel ADC
  - 16 bit, 125 MSPS
  - 2 channel DAC
  - Xilinx Virtex 5
  - 2 SFPs
- AMC520 (Vadatech)
  ADC Digitizer
  - 10 channel ADC
  - Xilinx Virtex 6
  - Dual core QorIQ

# AMC's and RTM's in the pipeline …

FIL

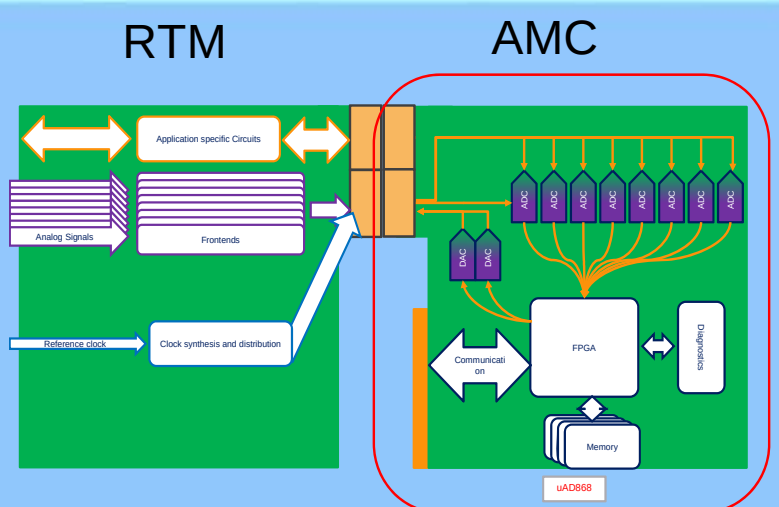
- Ultra-fast Klystron Protection, HOMs (DESY)

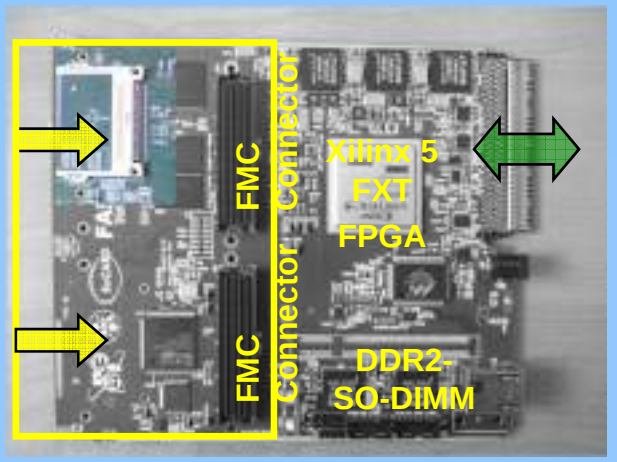
  High-Speed Sampling
  - 8 channel ADC (12-bits, 800Msps, 2.7GHz)
  - 2 channel DAC (16-bits, 160Msps, 400Msps)
  - Xilinx Virtex 6, DDR Memory
  - SFP support
  - Gigabit Ethernet, IPMI

- Universal 2 Slot FMC AMC Processing (DESY)
  - 2x1 or 2x2 FMC mezzanine support;
  - Virtex5 with PowerPC440
  - DDR2 SO-DIMM RAM support
  - IPMI unit, CF card memory
  - Gigabit Ethernet, Serial port, JTAG
- FMC Card for BAM monitors (DESY)
  Pulsed-signal conditioning

- AMC Timing Board (DESY)
  Timing, Clock, Interlock Distribution

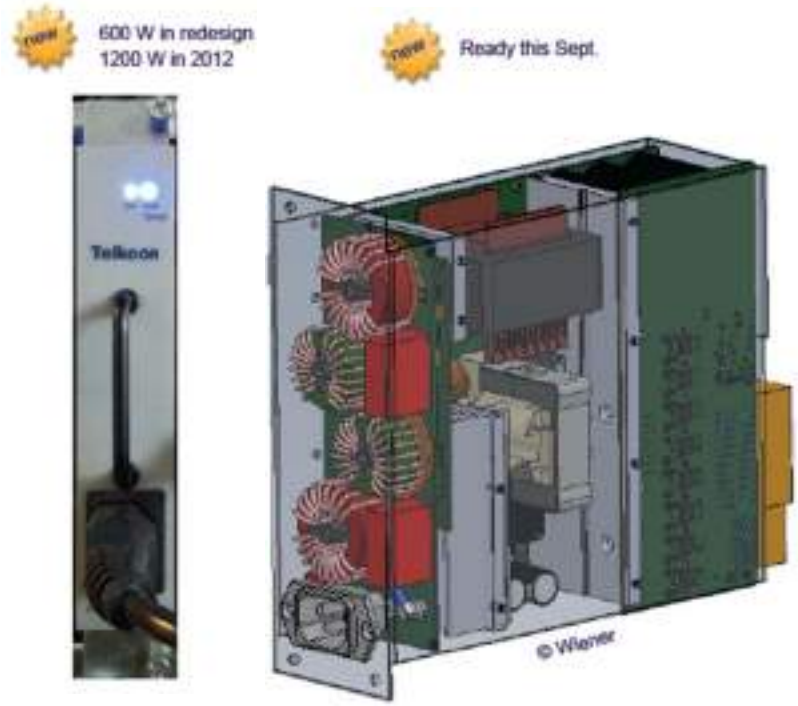
all ready to use expected in 02/13 for licensing …

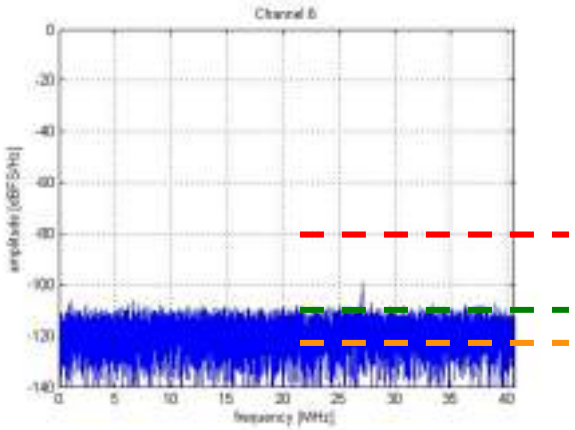


# Signal Integrity in MTCA.4 (below <-80dB)

- Low distortion MTCA.4 power supplies
- Guidelines for AMC and RTM designers




Poor Power Supplies : < 80dB SFDR

Power-Entry-Modules: < 110dB spurious free

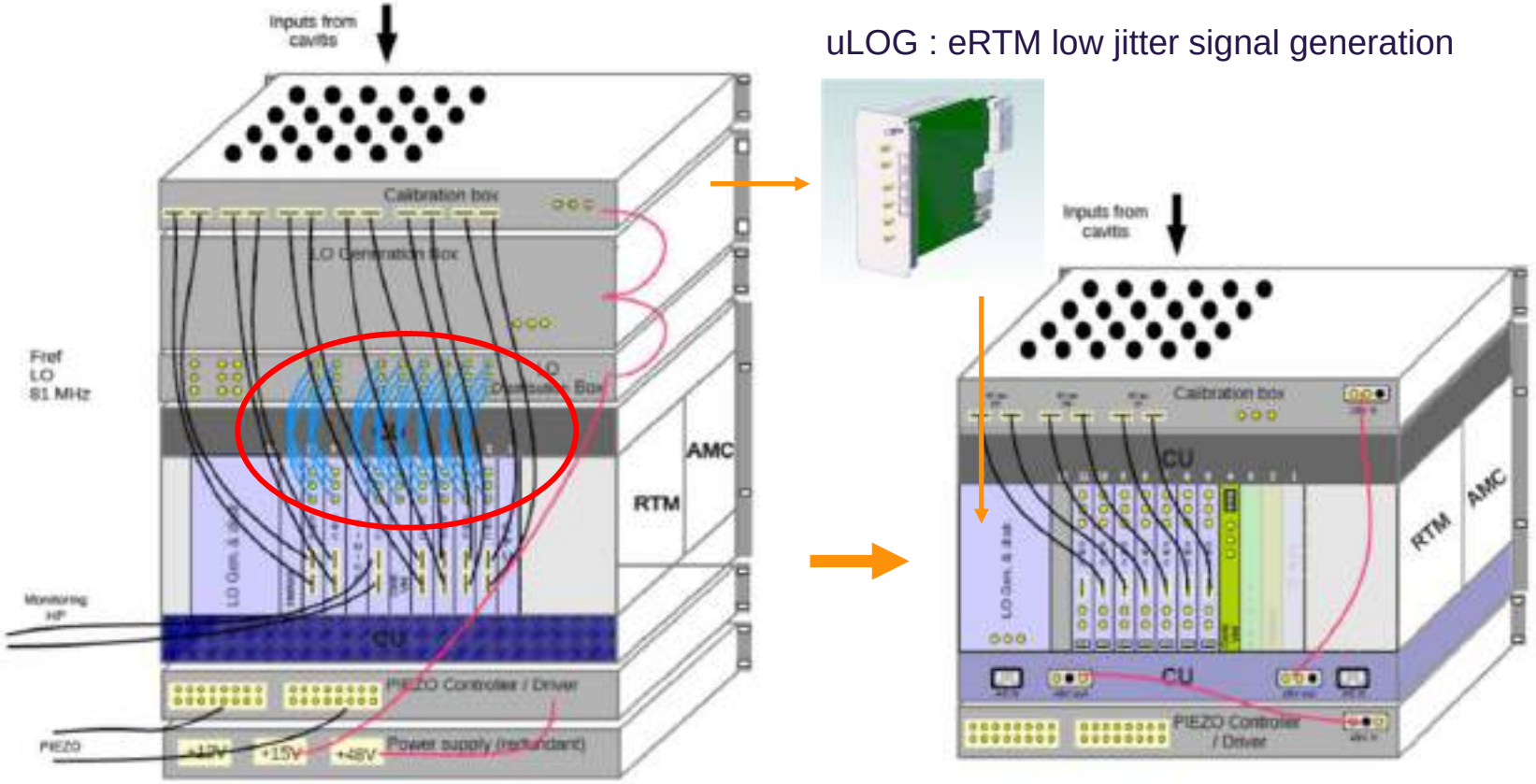
VS-Scaling : < 120dB SFDR

→ Single cavity resolution of dA/A=2.8E-5 achieved (1MHz BW).

→ Signal integrity in MTCA.4 crate achieved ADC eval board performance.

# Recent Developments : RF Backplane

- **Introduction of an optional RF-Backplane :**




Complicated cable management → LLRF eRTM backplane concept

# Recent Developments : RF Backplane

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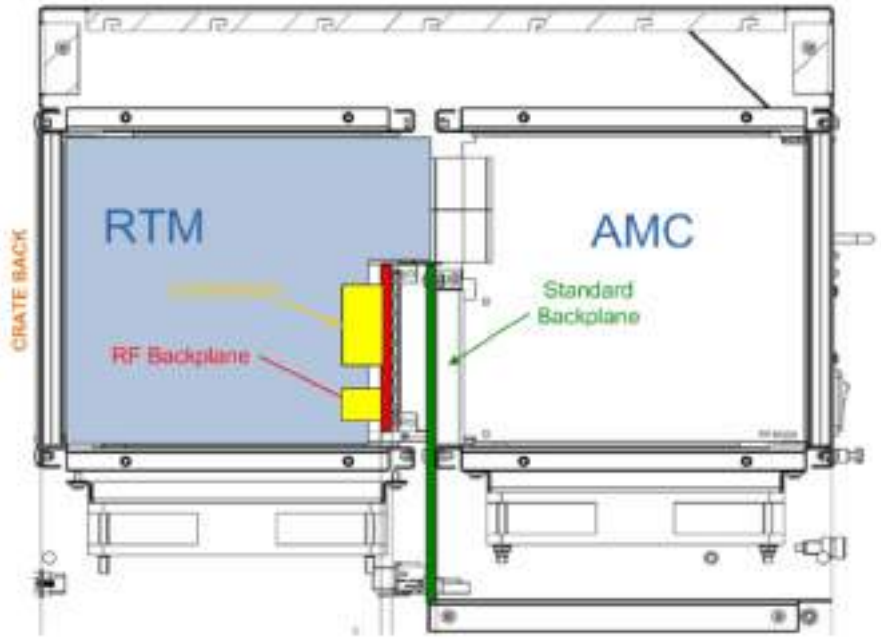
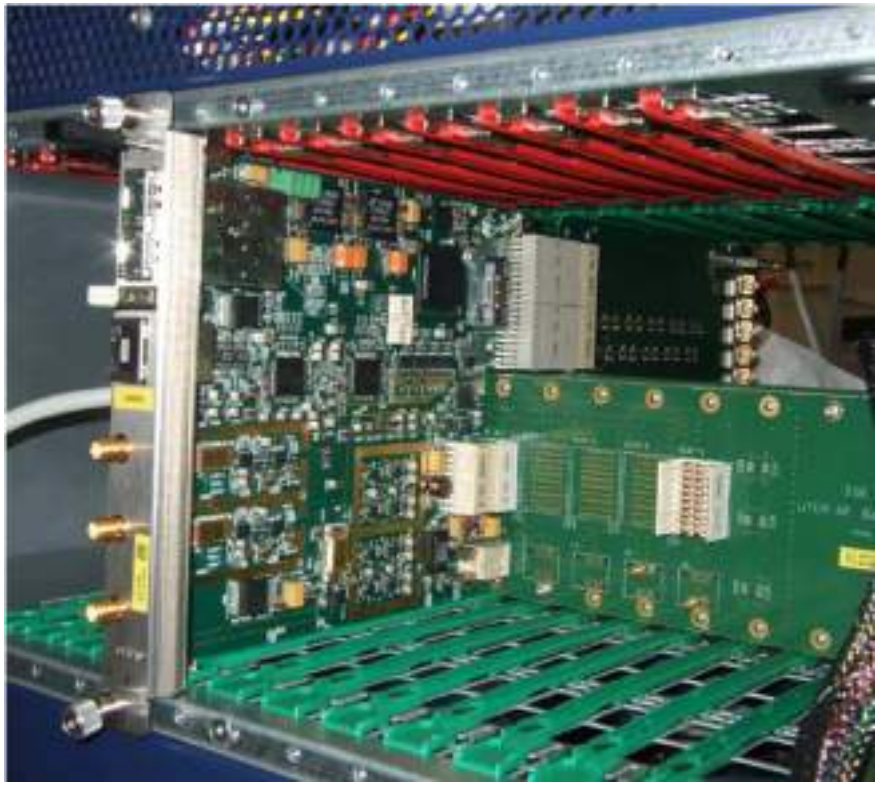
- **Successful test of an RF-Backplane in 02/2012**

- Low-jitter high-frequency signal distribution (<10fs)
- Low-jitter ADC-clock signal distribution (<200fs)

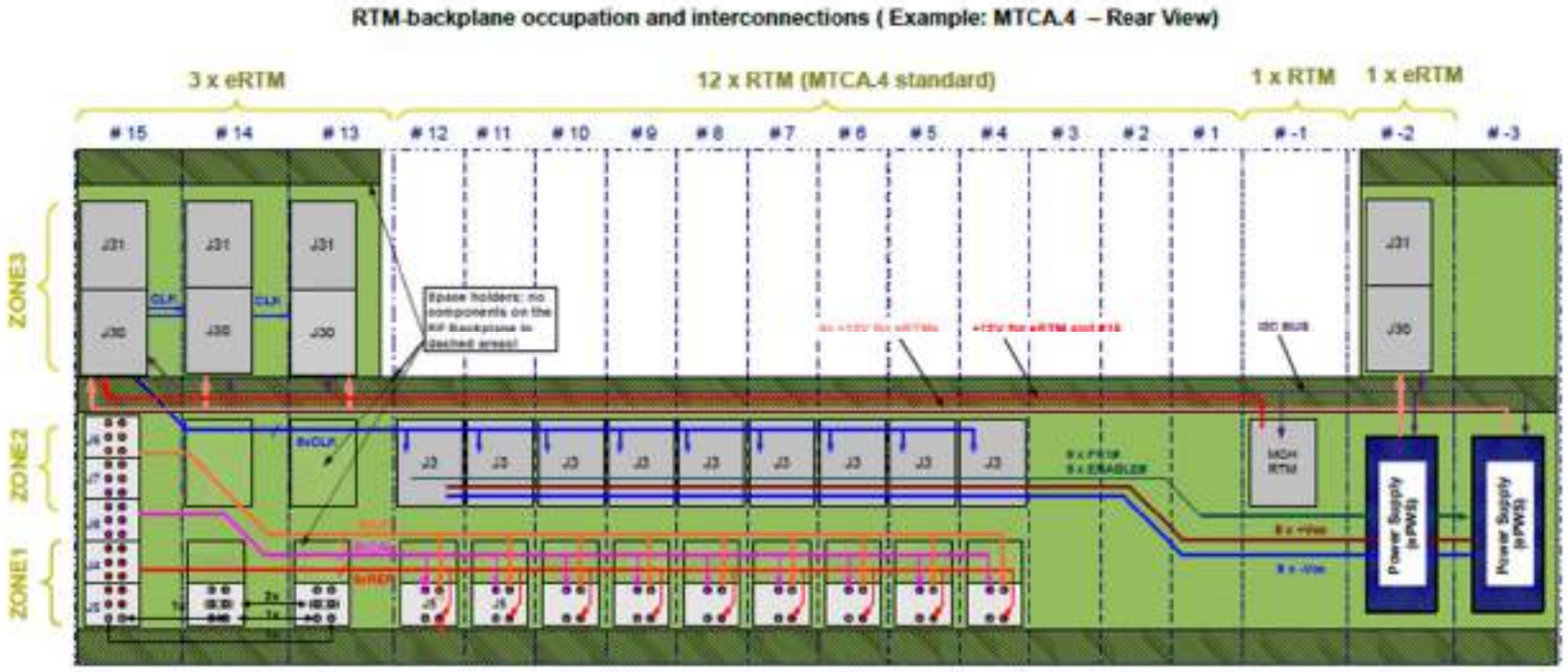


# Recent Developments : RF Backplane

FIL

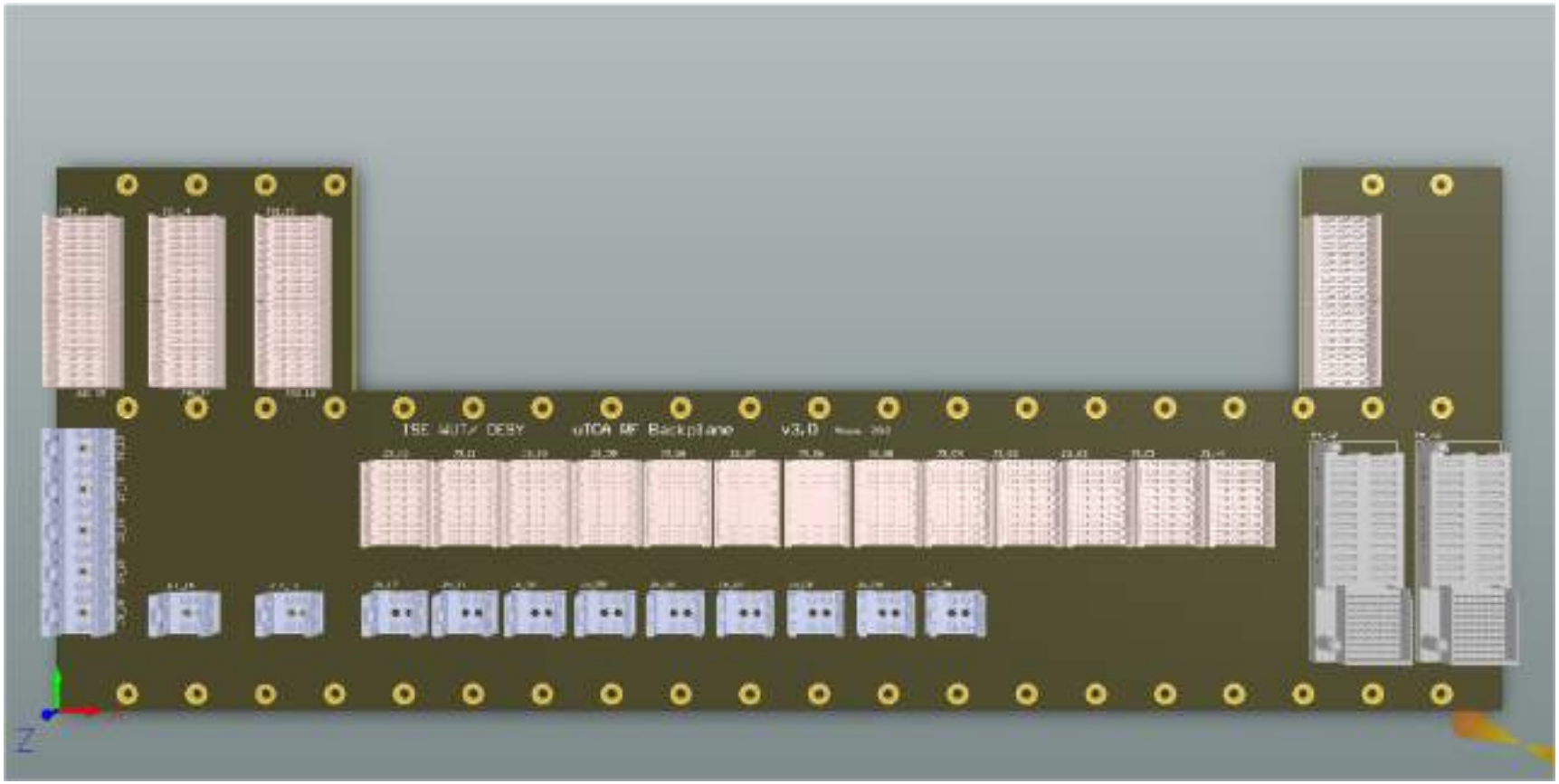
- **Introduction of an RF-Backplane**
  - Integration of eRTMs into the AMC Management
  - Fully compatible and optional extension to MTCA.4
  - Distribution of 9 RF, 9 LO, 9 CAL high frequency signals
  - Patented in 08/2012




Courtesy of K.Czuba

# Recent Developments : RF Backplane

- **RF-Backplane extension compatible to MTCA.4**




Courtesy of K.Czuba

# Zone3 Classification Recommendation

FIL

Deutsches Elektronen-Synchrotron
Ein Forschungszentrum der Helmholtz-Gemeinschaft
http://mtca.desy.de

- PRELIMINARY -

Class A1.1

Z3 Connector Pin Assignment Recommendation for Analog Applications for AMC/RTM Boards in the MTCA.4 standard

**FEATURES**

MTCA.4 management zone:
- Power, I²C, J-Tag support

Analog signal transmission zone:
- 10 channel AC-coupled differential input signals
- 10 channel DC-coupled differential input signals
- 5 differential output signals

Digital clock signal transmission zone:
- 6 LVDS inputs for low-jitter clock signals

User signal transmission zone:
- 12 LVDS inputs / outputs for user-configuration
- Optional dual high-speed links and user I²C bus

Zone shielding:
- Supports ground shielding between zones

**APPLICATIONS**

- AMC / RTM: board design in MTCA.4 standard
- High-precision multi-channel analog-to-digital converters
- High-speed multi-channel analog-to-digital converters
- Multi-channel high-frequency down/up-converters
- Multi-channel sensor readout and output
- Analog signal conditioning boards
- Low-clock jitter signal sampling and clock recovery

**GENERAL DESCRIPTION**

This Class A1.1 pin assignment definition of the Z3 connector in the MCA.4 standard is a recommendation mainly for AMC and RTM boards transferring analog signals over the Z3 connector. The main goal is to classify the undefined Z3 pin assignment for applications to achieve the highest compatibility between AMC and RTM boards for a broad MTCA.4 market.

**AMC Z3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION**

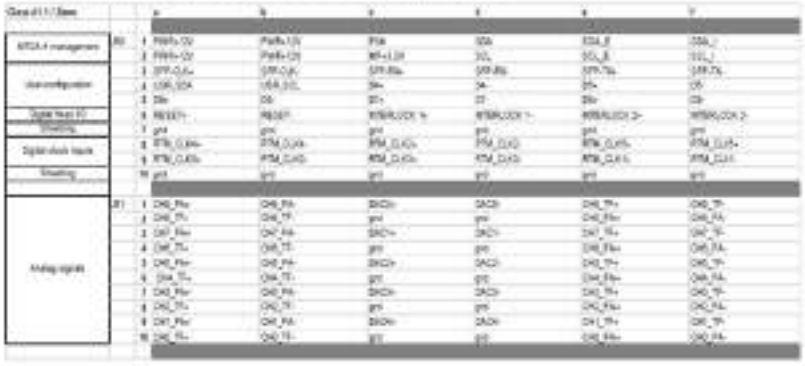


Table 1 : view from AMC side

Deutsches Elektronen-Synchrotron
Ein Forschungszentrum der Helmholtz-Gemeinschaft
http://mtca.desy.de

- PRELIMINARY -

Class D1.0, D1.1, D1.2, D1.3, D1.4

Z3 Connector Pin Assignment Recommendation for Digital Applications for AMC/RTM Boards in the MTCA.4 standard

**FEATURES**

MTCA.4 management zone:
- Power, I²C, J-Tag support

Digital signals with fixed direction:
- Standard dual high-speed link support
- 2 LVDS low phase noise clocks
- 4 LVDS outputs

Digital signals in the user zone:
- Class D1.0: 64 LVDS I/O signals
- Class D1.1: 42 LVDS I/O signals, 2 high-speed links
- Class D1.2: 36 LVDS I/O signals, 4 high-speed links
- Class D1.3: 26 LVDS I/O signals, 8 high-speed links
- Class D1.4: 6 LVDS I/O signals, 16 high-speed links

**APPLICATIONS**

- AMC / RTM: board design in MTCA.4 standard
- High-speed data processing
- Multi-channel data converters
- Multi-channel sensor readout and output
- Digital signal conditioning boards

**GENERAL DESCRIPTION**

This Class D1 pin assignment definition of the Z3 connector in the MCA.4 standard is a recommendation mainly for AMC and RTM boards transferring digital signals for high-speed or low-speed applications over the Z3 connector. The subclasses D1.0, D1.1, D1.2, D1.3, D1.4 offers different numbers of digital input / outputs and high-speed communications links. The main goal is to classify the undefined Z3 pin assignment for applications to achieve the highest compatibility between AMC and RTM boards for a broad MTCA.4 market.

**Z3**

- Z3 pin-assignment not standardized in MTCA.4 (AMC – RTM pairs)

-> Z3 Classification
-> Higher compatibility between AMC's and RTM's

# Helmholtz Validation-Fond

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## MTCA.4 for Industry and Research

**4 Mio. €**

# Helmholtz Validation-Fond

## MTCA.4 for Industry and Research

DESY

**7 Industry Partner**

**4 Mio. €**

# Helmholtz Validation-Fond

## MTCA.4 for Industry and Research

HELMHOLTZ ASSOCIATION

DESY

**7 Industry Partner**

**4 Mio. €**

# MTCA.4 for Industry

- **To foster industrialization of MTCA.4 (incl. LLRF)**

- **Support for institutes and industry**
  - Consulting: Help to start with MTCA
  - User guide and Web Site
  - Organization of workshops and exhibitions


- **DESY designs -> industry (licensing)**
  - Cost and quality improvements
  - New modules to complete portfolio

- **Supporting industry to**
  - Add missing modules
  - Improve EMI with test environments and shielding, EMI classification
  - Gain new MTCA.4 applications in more markets

**Dr. Ilka Mahns / DESY**
**Technology Transfer Division**

Project duration: mid 2012 … mid 2014




## Welcome to the MTCA Workshop for Research and Industry

The MTCA workshop for industry and research will take place from 11th December to 12th December in Hamburg, Germany. DESY invites you to participate in this workshop.

The workshop will bring together experts and beginners from industry and research to discuss present and future developments in the field of MTCA. The main task of the workshop is

- to spread the knowledge of MTCA;
- to show how to set up a MTCA.4 system;
- to show which modules are available today;
- to learn if there are incompatibilities between modules;
- to resolve ambiguities in the specifications;
- to discuss desired changes to the standard;
- to improve the backplane for analog applications.

**Thanks for your attention!**

At an exhibition from industry, the newest products involving MTCA.4 modules will be presented. You will have direct contact to the manufacturers.

We are looking forward to meeting you at the workshop in DESY, Hamburg!



This workshop is part of the Helmholtz Validation Fund HVF-0016 "MTCA.4 for Research and Industry"
http://mtcaws.desy.de