

Dejan Tinta

Libera Photon

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17 September 2009

Libera Photon

A new member in the Libera product family

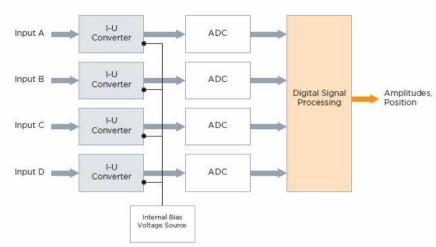


Basic Features

- All in one:
 - Current to voltage conversion
 - Digitalization
 - Digital signal processing
- Four current inputs
- Internal bias voltage source
- Internal calibration current source
- Same interfaces like Libera Brilliance:
 - Connection to control system
 - Timing (synchronization)
 - Integration in FOSS

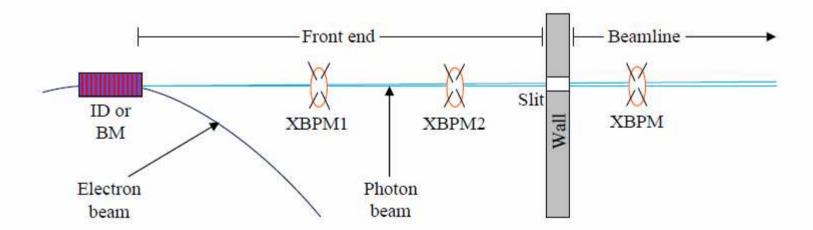


Instrumentation

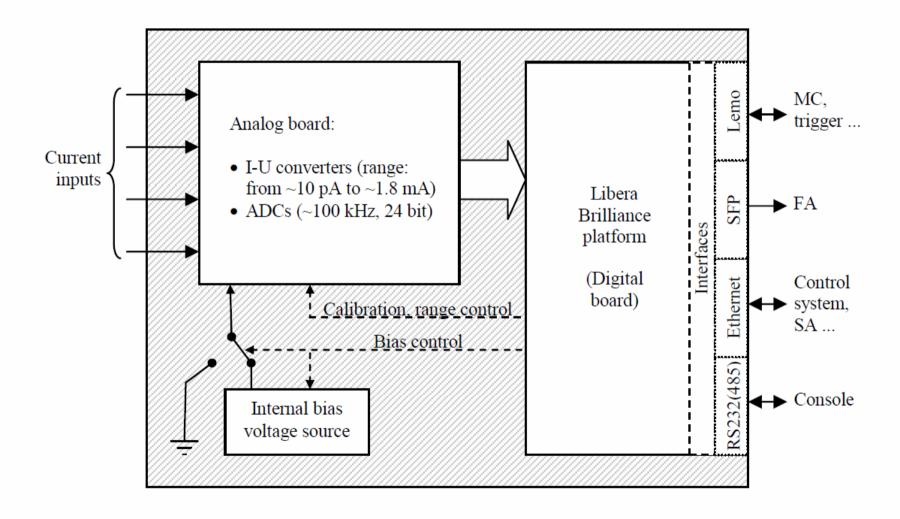


Applications

- XBPMs at front ends of storage rings (monitoring, integration in FOSS)
- On beamlines: XBPMs, ionization chambers (monitoring, feedback)



Libera Photon Layout



Front Panel

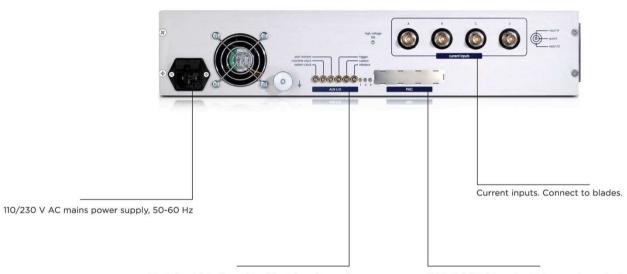
100 Base-T Ethernet ports used for communication and integration with accelerator control system. Control and measurement data are exchanged at lower rates. Port 3 is for standard use. Ports 1 and 2 are intended for future use.

SFP slots, used for fast serial communication. They provide reliable data exchange at the high rate needed to support fast feedback processing. Libera Gigabit Ethernet Interface is now availale. Several other standards are supported.

RS485 ports, used for control of horizontal and vertical corrector magnet power supply. Additional functionality possible. Up to 6 RS485 channels available.



Back Panel



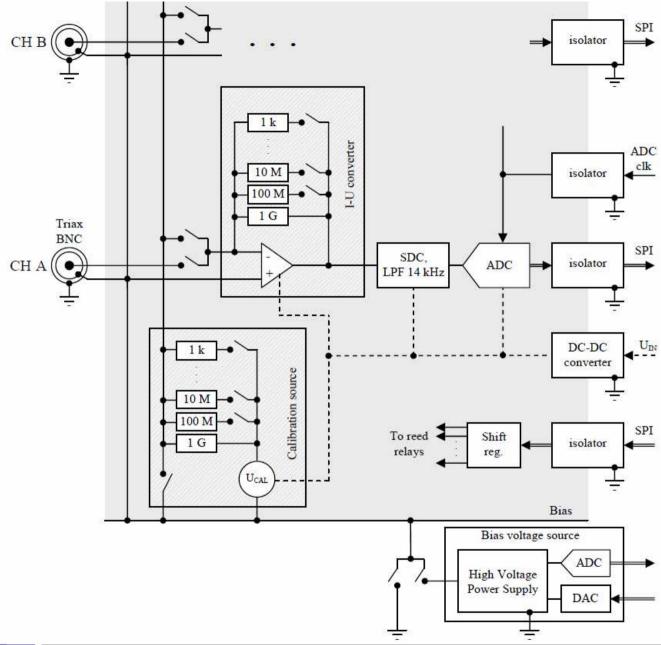
Fast signal interfaces. Used for triggering and synchronization purposes. They support time critical events and processes:

- System clock reference. Synchronizes Libera with accelerator timing system.
- Machine clock reference. Synchronizes Libera with accelerator revolution frequency.
- Post mortem trigger. Used for acquisition of data for post mortem analysis.
- Trigger. Used for sinchronization with asynchronous external events, i.e. injection or time setting. Functionality is software defined.
- Custom. Reserved for future purposes.
 Interlock. Optoisolated. Sends a warning signal if beam position is outside a predefined range

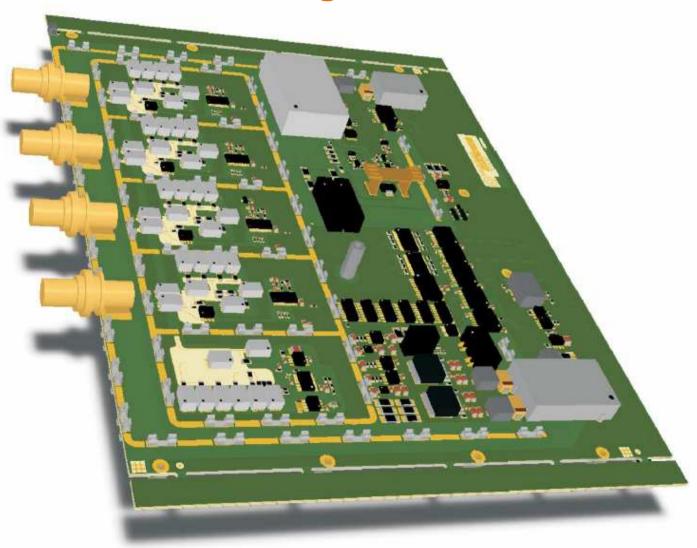
PMC slot. PMC board with two analog outputs can be attached in the slot. The DACs of the outputs are connected directly to the FPGA. The outputs can be used to e.g. drive the mirrors in the beamline feedback.



Analog Board Scheme



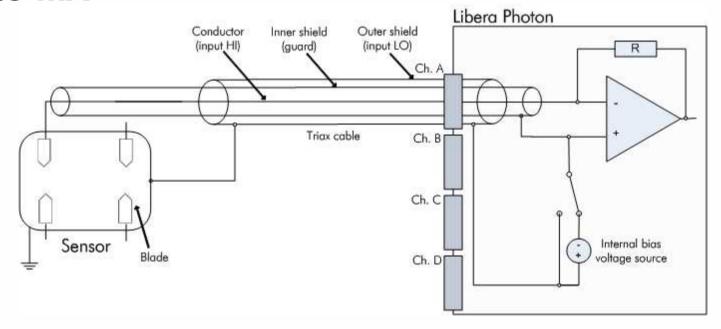
Analog Board



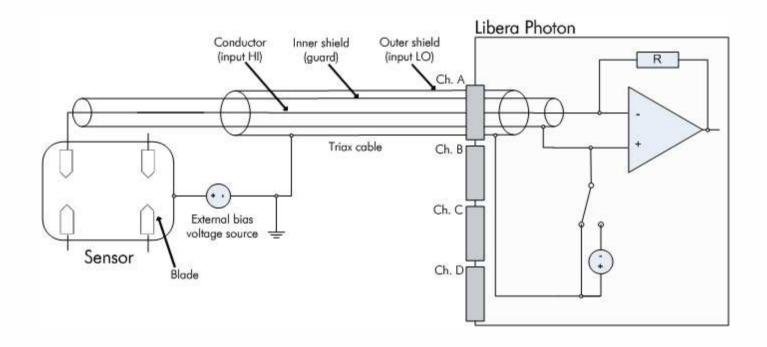
Measurement with Internal Bias Voltage Source

Internal bias voltage source:

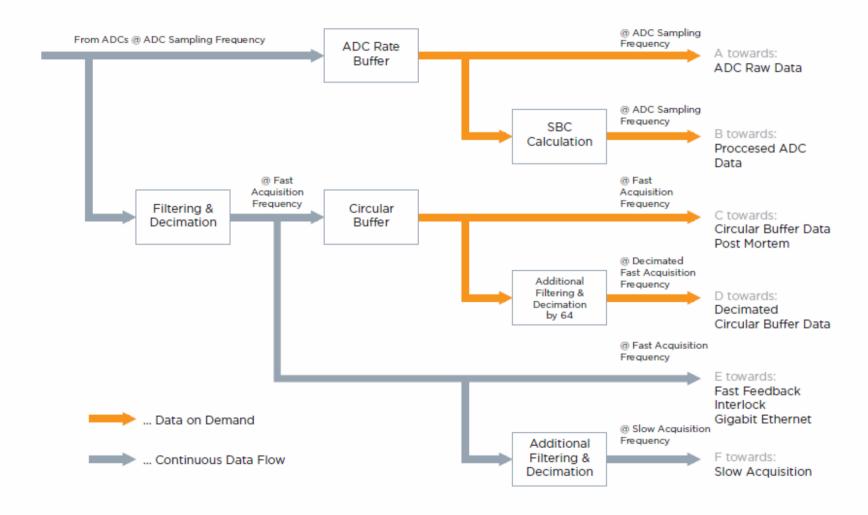
- 0 V -450 V
- 7.5 mA



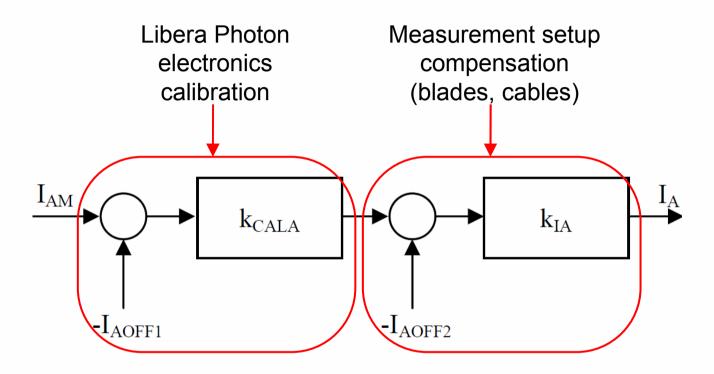
Using an External Bias Voltage Source



Data Paths



Offset & Gain Compensation



$$\begin{split} I_A &= \left[\left(I_{AM} \text{-} I_{AOFF1} \right) \text{*} k_{CALA} \text{-} I_{AOFF2} \right] \text{*} k_{IA} \\ I_B &= \dots \\ I_C &= \dots \\ I_D &= \dots \end{split}$$

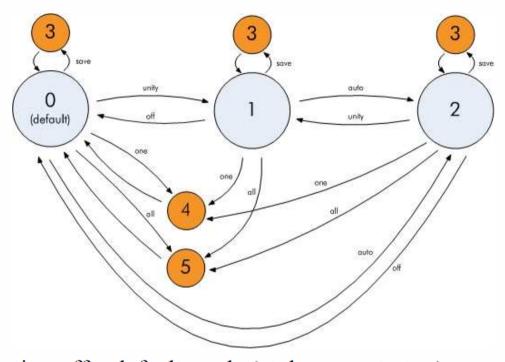
Libera Photon Electronics Calibration

- Connect internal calibration source
- Acquire data
- Calculate correction coefficients:

$$I_{AV} = \left[(I_{AAV} - I_{AOFF1}) + (I_{BAV} - I_{BOFF1}) + (I_{CAV} - I_{COFF1}) + (I_{DAV} - I_{DOFF1}) \right] / 4$$

$$k_{CALX} = I_{AV} / (I_{XAV} - I_{XOFF1}); \quad (X = A, B, C, D)$$

Calibration Modes



mode 0: calibration off – default mode (at daemon startup)

mode 1: apply unity coefficients

mode 2: auto calibration

mode 3: save last good coefficients

mode 4: manual calibration (on demand) – only one (current) range

mode 5: manual calibration (on demand) – all ranges



Measurement Setup Compensation

- Cable leakage
- Differences between blades...

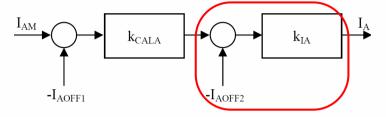


Table of coefficients defined by user:

| | k _{IA} | I _{AOFF2} | $k_{\rm IB}$ | I_{BOFF2} | k_{IC} | I_{COFF2} | $k_{\mathbb{D}}$ | $I_{\text{DOFF}2}$ | \mathbf{k}_1 | OFF ₁ | \mathbf{k}_2 | OFF ₂ | |
|-------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|-----------------------|-------|
| Range | 1 1 1 1 1 1 | 0 0 0 0 0 0 | 1 1 1 1 1 1 | 0 0 0 0 0 0 | 1 1 1 1 1 1 | 0 0 0 0 0 0 | 1 1 1 1 1 1 | 0 0 0 0 0 0 | ? ? ? ? ? ? | 0 0 0 0 0 0 | ? ? ? ? ? ? | 0 0 0 0 0 | · ID1 |
| | | | | | | | | | | | | | → ID2 |
| | | | | | | | | | | | | · | • |

All coefficients can be set also as runtime parameters



Position Calculation

1st option: measurement in horizontal and vertical direction (after insertion device):

$$X = k_1 * [(I_A + I_D) - (I_B + I_C)]/[I_A + I_D + I_B + I_C] + OFF_1$$

 $Y = k_2 * [(I_A + I_B) - (I_C + I_D)]/[I_A + I_D + I_B + I_C] + OFF_2$

2nd option: two measurements in vertical direction (after bending magnet):

$$Y_1 = k_1 * (I_A - I_D)/(I_A + I_D) + OFF_1$$

 $Y_2 = k_2 * (I_B - I_C)/(I_B + I_C) + OFF_2$

3rd option: two measurements in vertical direction (after bending magnet, log equation):

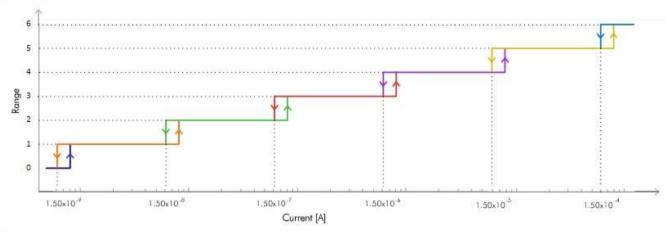
$$Y_1 = k_1 * log(I_A/I_D) + OFF_1$$

 $Y_2 = k_2 * log(I_B/I_C) + OFF_2$

Input Current Ranges

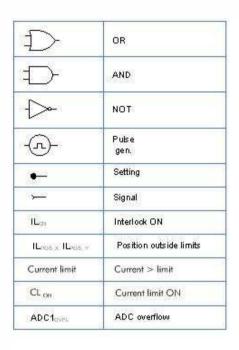
The ranges can be set manually or automatically. Automatic range control is based on observation of 2nd max. ADC sample. A hysteresis is introduced to avoid constant switching beetwen adjacent ranges:

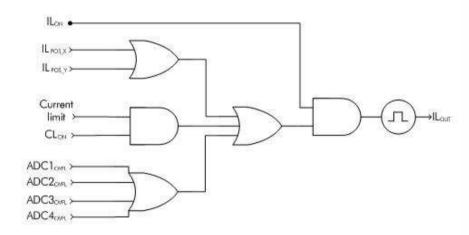
| Range | Input current |
|-------|-----------------|
| 0 | <2 nA |
| 1 | 2 nA – 20 nA |
| 2 | 20 nA- 200 nA |
| 3 | 200 nA − 2 uA |
| 4 | 2 uA – 20 uA |
| 5 | 20 uA – 200 uA |
| 6 | 200 uA – 1.8 mA |
| • | • |



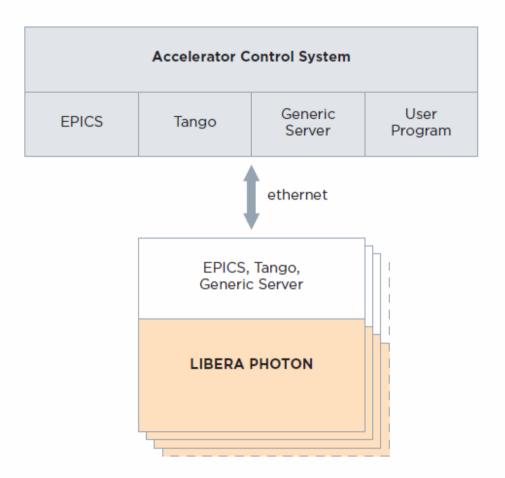


Interlock





Integration into Control System



Integration in FOSS

Libera Photon can be easily integrated in FOSS together with Libera Brilliance. Key features:

- •Fully synchronized data to accelerator revolution frequency (same synchronization mechanism is used like in Libera Brilliance: PLL, trigger, offsettune)
- •Fast data at ~10 kHz data rate and 2 kHz bandwidth
- Positions X and Y are provided
- •Three principles for FOSS are supported: GbE interface, Grouping, Communication Controller

Bandwidth



Future Upgrade

PMC board with 2 analog outputs:

- It is intended to close the beamline feedback (e.g. to drive the mirrors).
- The DACs will be driven by FA data (@ 10 kHz rate).
- Development kit in FPGA will allow the user to implement different control algorithms.

Thank you for your attention