



Instrumentation
Technologies

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Libera LLRF Software

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Libera **WORKSHOP**
2009

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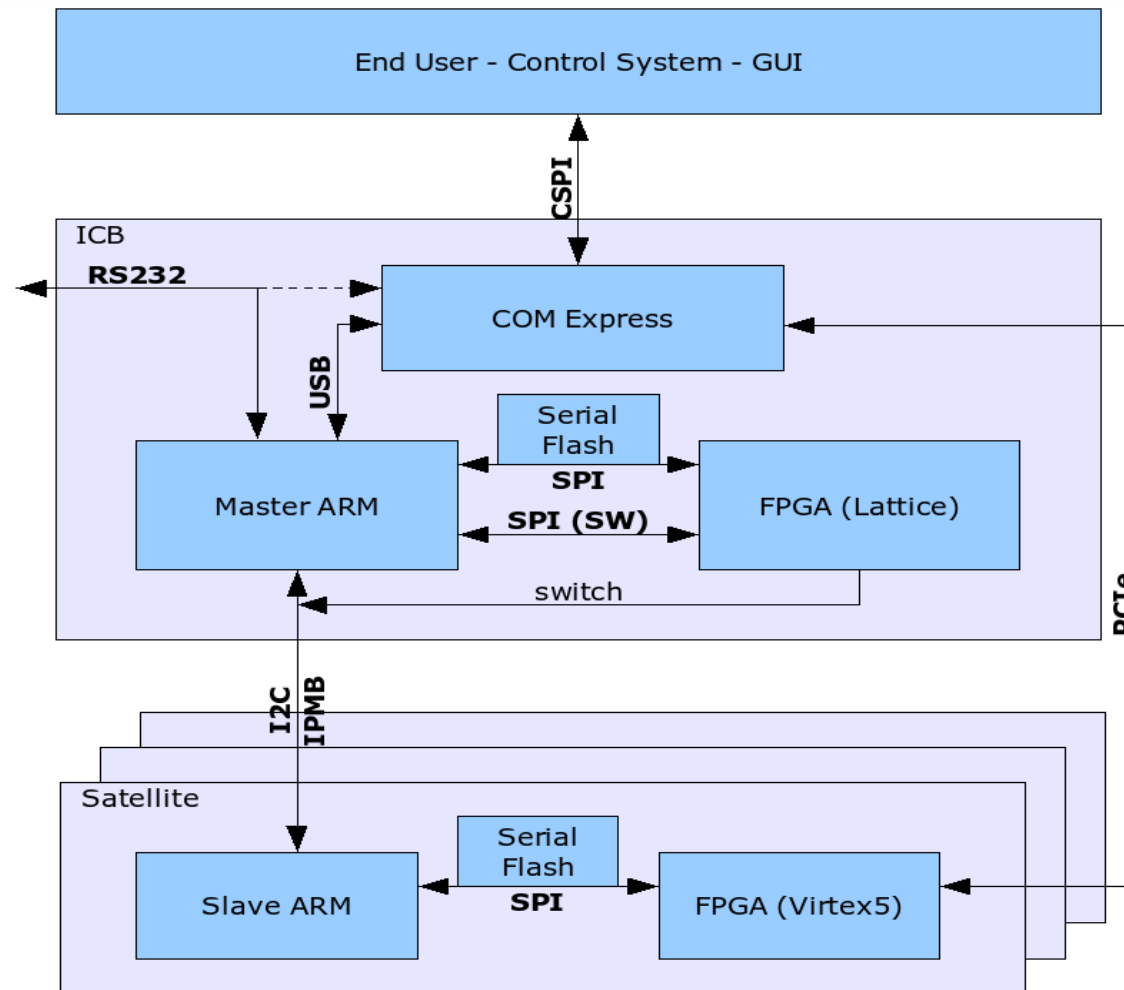
Libera LLRF SW Concept

- **Generic as much as possible**
- **@ Low level:**
 - 1-1 relation to HW satellite boards
 - Modular, but with minimal or no impact on performance
- **@ Mid & High level:**
 - Generic data paths
 - High level mapping for “instrument specifics”

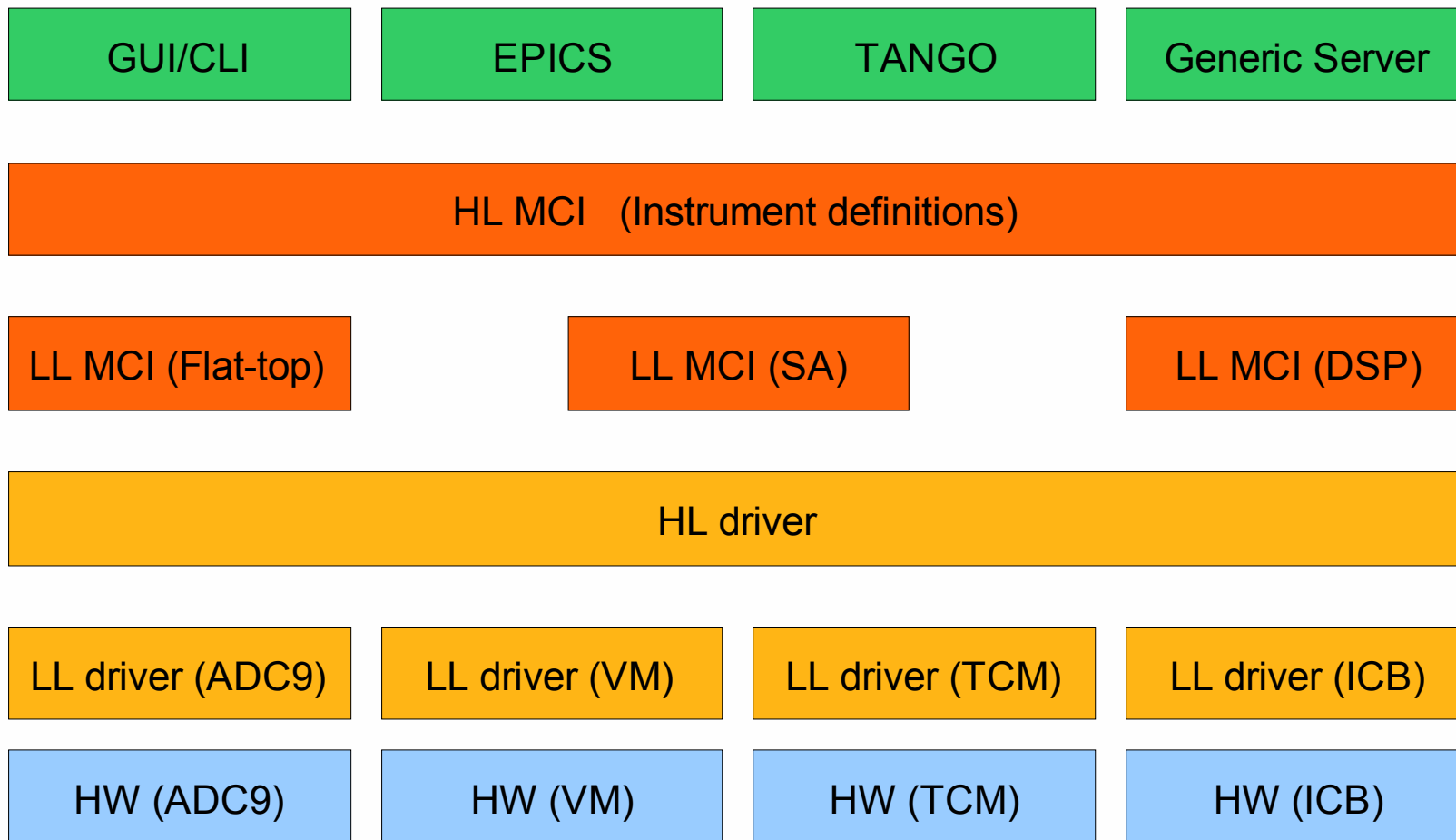
Low level (Chasis) Software

- As close to **IPMI standard** as possible (**Intelligent Platform Management Interface**)
- **Firmware upgrades**
- **JTAG access (FPGA debugging)**
- **Environmental monitoring**
 - Temperature
 - Voltages
 - Fan speed

Low Level SW



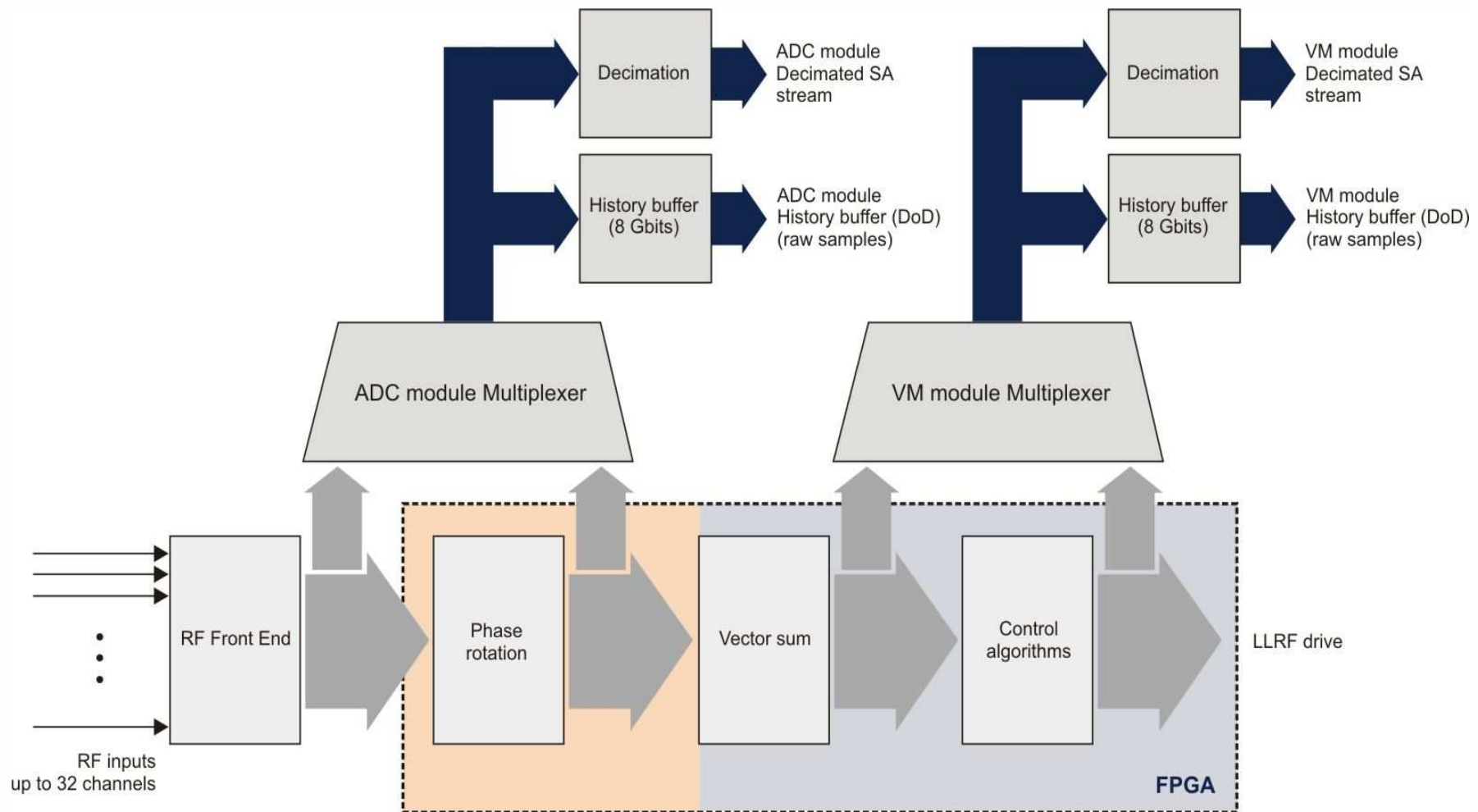
Mid & High Level Software

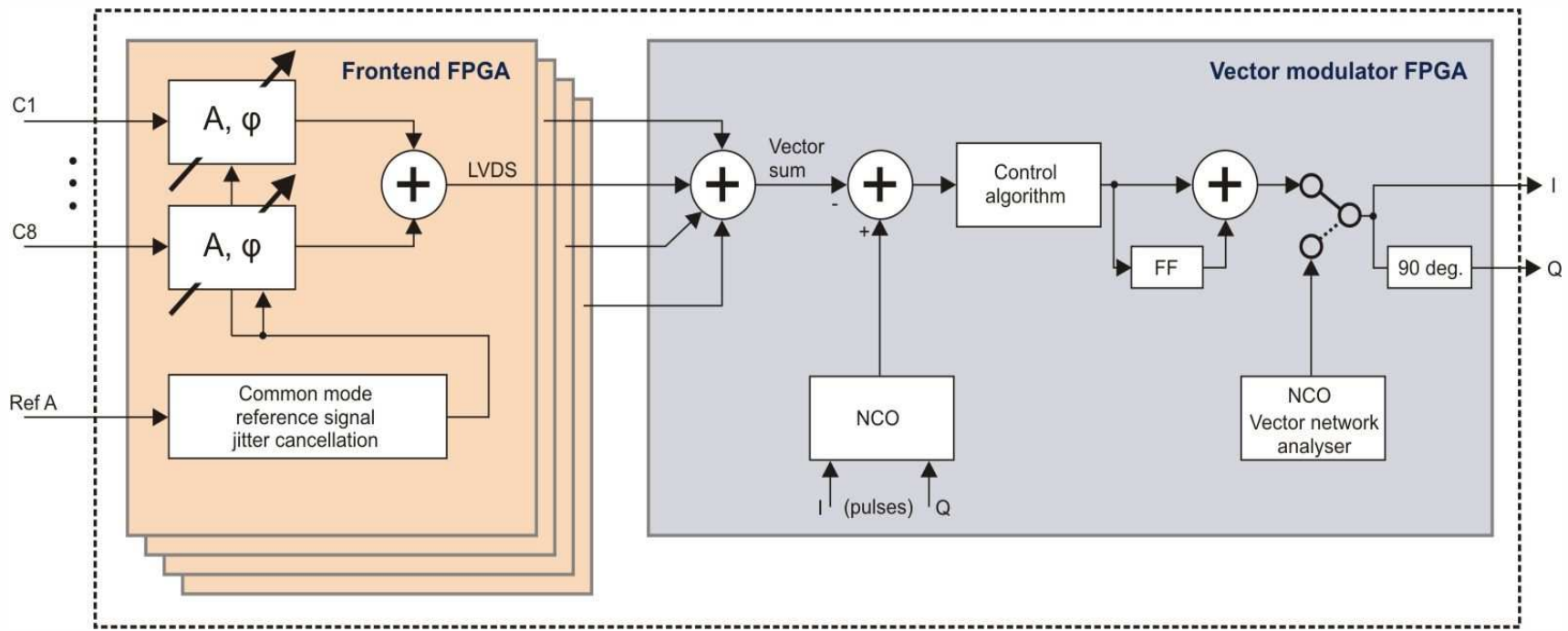


Mid Level Software

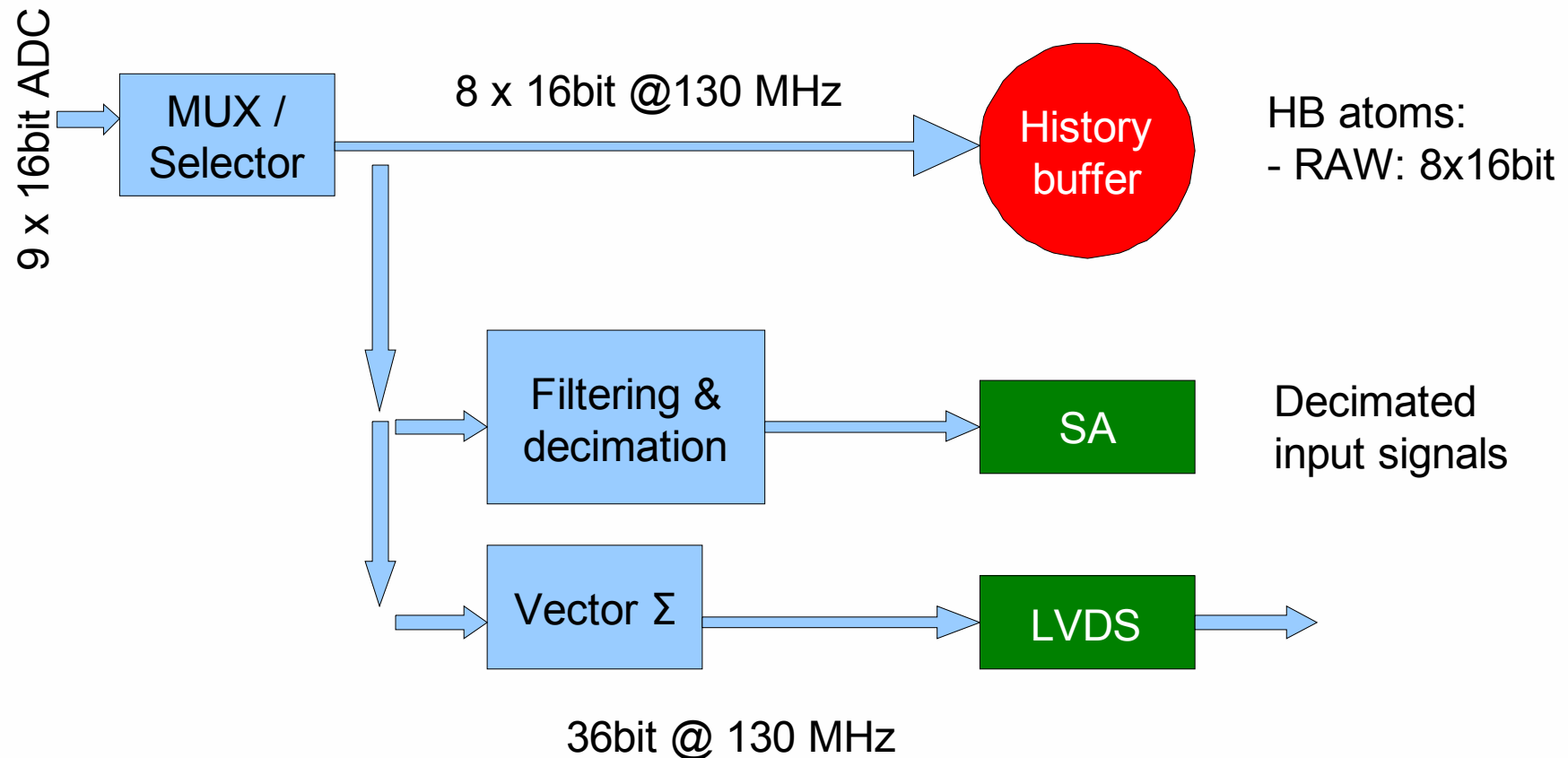
- **FPGA modules on internal bus:**
 - ADC, DAC, I/O, DDR2, PCIe
 - Timing & synchronization
 - DSP & Application
- **GNU/Linux driver modules:**
 - Flat-top, SA, DSP channels
 - DMA
 - Built-in debugging

LLRF Application & Monitoring

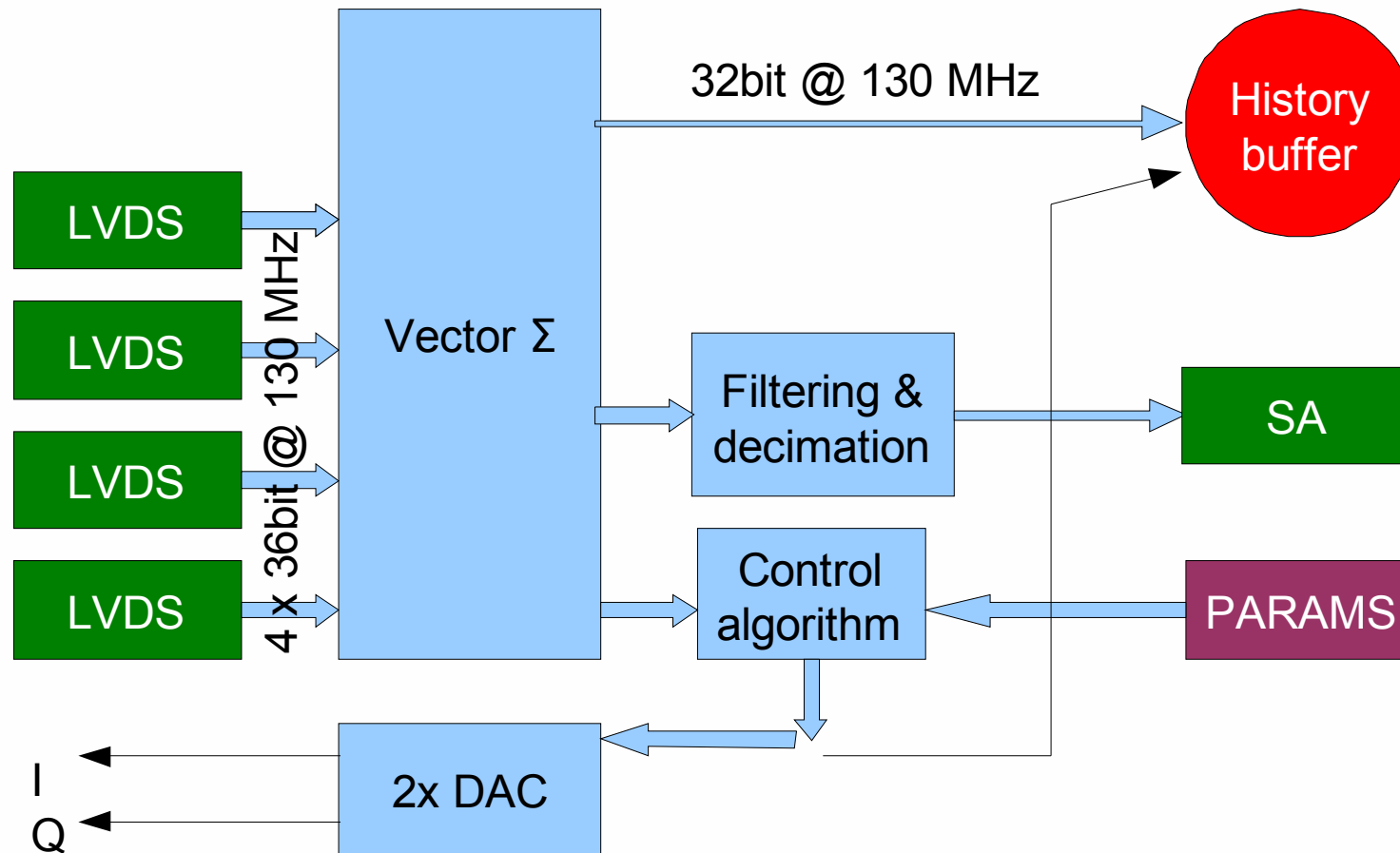




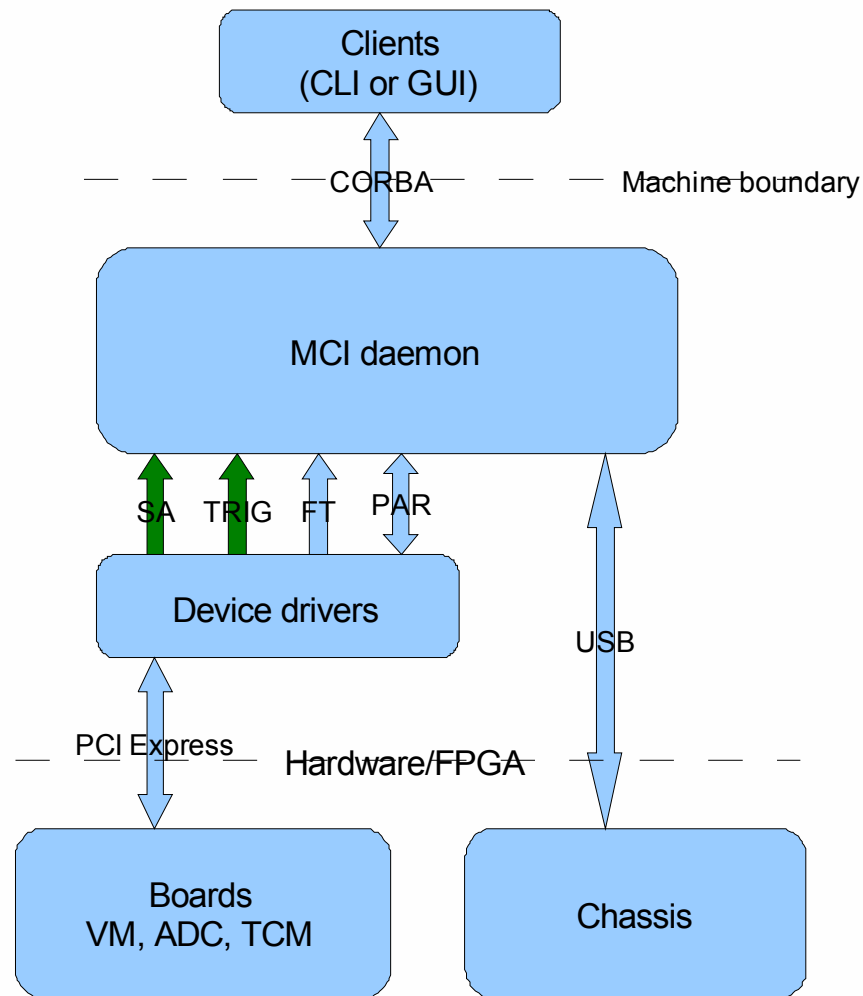
LLRF – Data Paths (ADC9)



LLRF – Data Paths (VM)



Software Interfaces



- **Measurement Control Instrument (MCI) is implemented in MCI daemon:**
- **Enumeration: List of boards, signals, sensors.**
- **Information (attributes, state,...) about board, signal, sensor, application.**
- **Provide signal data via callback receiver: bounded to BoardID, SigID, stream type (SA, Flat-top) and stream processing (eRaw/eAmpPhase/eIQ).**
- **Provide sensors attributes and data via USB IPMI protocol.**
- **LLRF application specific control (Sweep, Decay, Stability, Loop control, Trigger, ...).**
- **Chassis control (status, temperature control, FPGA load, Power control, ...).**

