Tomaž Karčnik, Borut Baričevič,
Vladimir Poučki, Sebastjan Zorzut

Libera Family Development Potential

tomaz@i-tech.si

24-25 September 2007

Current activities

- **Libera capabilities**
  - **Light source BPP**
  - **Hadron BPP**
  - **Bunch-by-Bunch feedback**
  - **Playground for R&D work**
- **Ongoing activities, applications**
  - **Pulsed mode BPP (FELs, ERLs)**
  - **LLRF**
    - **Embedding user FPGA core applications**

Single pass BPM

- **Developed for the 4th generation of light sources**
  - **Pulsed mode vs. (gated) CW**
  - **1.3 – 8 GHz vs. 500(350) MHz**
  - ***fs* vs. *ns* time scale/syncing**
  - **Feedforward vs. feedback**
  - **Direct sampling not possible yet**
- **Modifications ranging from RF electronics all the way up to CS interface**
- **Presentation by Borut Baricevic**

FPGA

- **Not many/all users have the ability/possibility to dive into the FPGA programming world:**
  - **Linus Torvalds when asked what he'd start doing if he moved out of kernel programming: *I'd really love to do FPGA's, but I've always been too busy to really sit down and start learning*.**
- **Obviously an interesting field**
- **Unfortunately, requires daily activities to keep the cutting edge**

FPGA devel. kit

- **Development kits**
  - **Simplify and speed-up the development cycle at the expense of lesser optimization**
  - **Getting new people on board**
- **Hardware and application specific environment for integrating user code**
  - **Verilog, VHDL (EBPP: Diamond, Soleil)**
  - **System Generator for Simulink (BBB: ESRF)**
  - **Other sources: Matlab & toolboxes, ….**

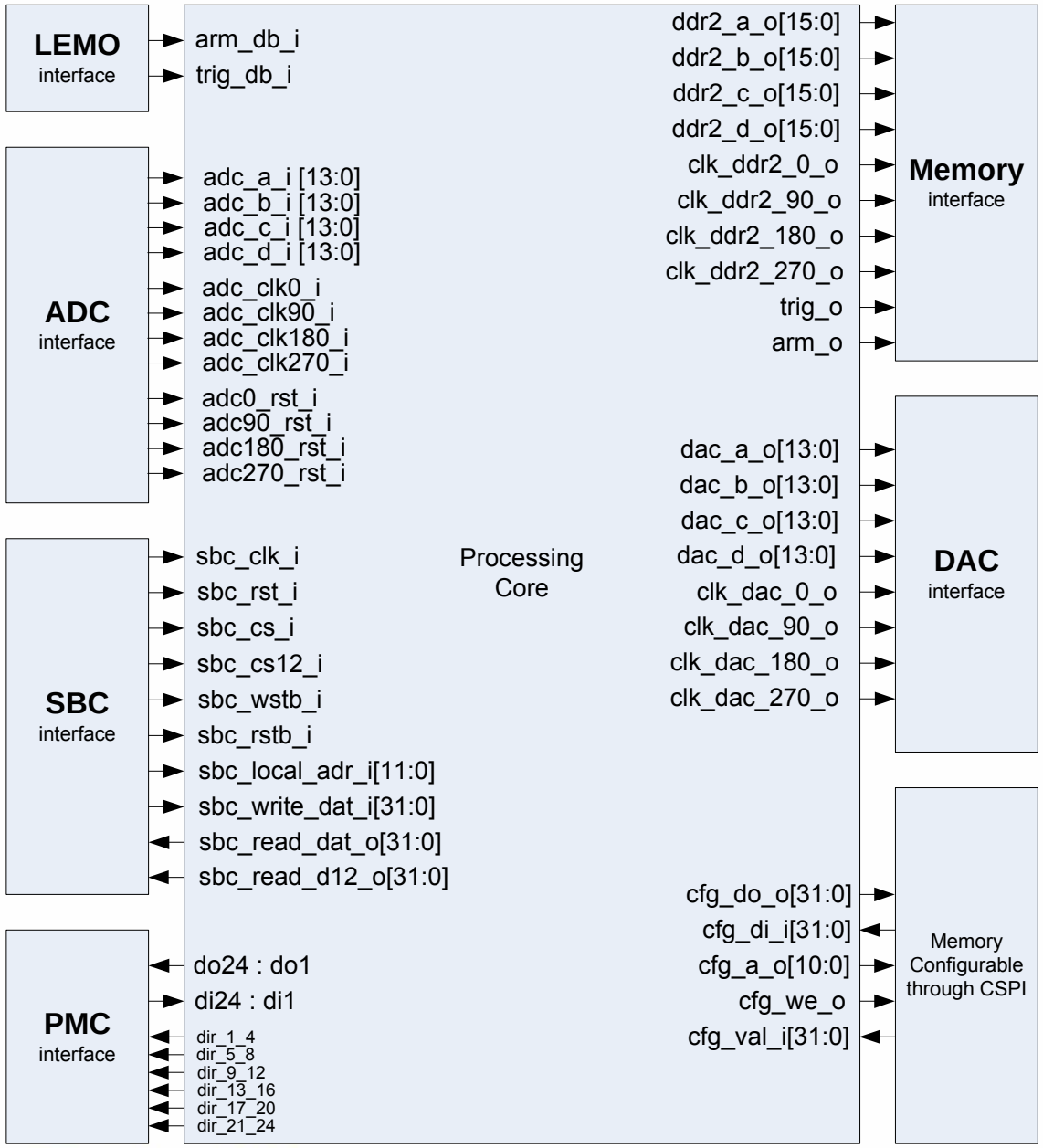
FPGA devel. kit

- The kit does not relive users from understanding the FPGA concepts and the process of FPGA design building: clock management, constrains, ...
- Ideally: Matlab/Simulink user can do FPGA development
- Verified interfaces to HW are included
  - High level programming not suitable for interfacing to hardware

FPGA devel. kit, contents

- **Contents:**
  - **Top module source code**
  - **Constraints**
  - **IP cores**
  - **Placeholders for user cores: Verilog and System Generator**
  - **System Generator demo application and configuration**
  - **Build scripts including configuration**
- **Live demo of FPGA development kit for BBB/LLRF in later session**

FPGA core connections



FPGA devel. kit demo

- **Live demo:**
  - **Full BBB application**
    - **Demonstrated earlier today**
  - **Integration of System Generator**
  - **Full development cycle**
    - **Minus FPGA build process, typ. 45 min**
- **Presentation by Vladimir Poucki**

LLRF

- LLRF is gaining importance in 4th generation light sources
- LLRF is not yet "clean, well defined" application from the implementation point of view
  - I/Os vary in number and function
  - Various configurations: 1:1, 1:n
  - Feedback device: playground for control algorithms
    - Similar to robotics

LLRF and FPGA

- **LLRF core digital control algorithm typically implemented in the FPGA**
  - **optionally a combination of (AS)ICs, DSPs**
- **FPGA**
  - **Parallel, hard real-time, reliable operation of "arbitrary" complexity**
  - **High learning threshold, slow development cycle, lot of work required to get the whole system operational**
    - **Fast interfaces (ADC, DAC, DDR2/3 RAM), programmable delays**
  - **Merging 3rd party code: user code, comm. cores**

FPGA devel. kit demo

- **Live demo:**
  - **Simplified LLRF application**
  - **Painless integration of System Generator and Instrumentation Technologies code, cores, tools, scripts, …., a.k.a. FPGA development kit**
  - **Full development cycle**
- **Presentation by Sebastjan Zorzut**