Libera Bunch-by-Bunch

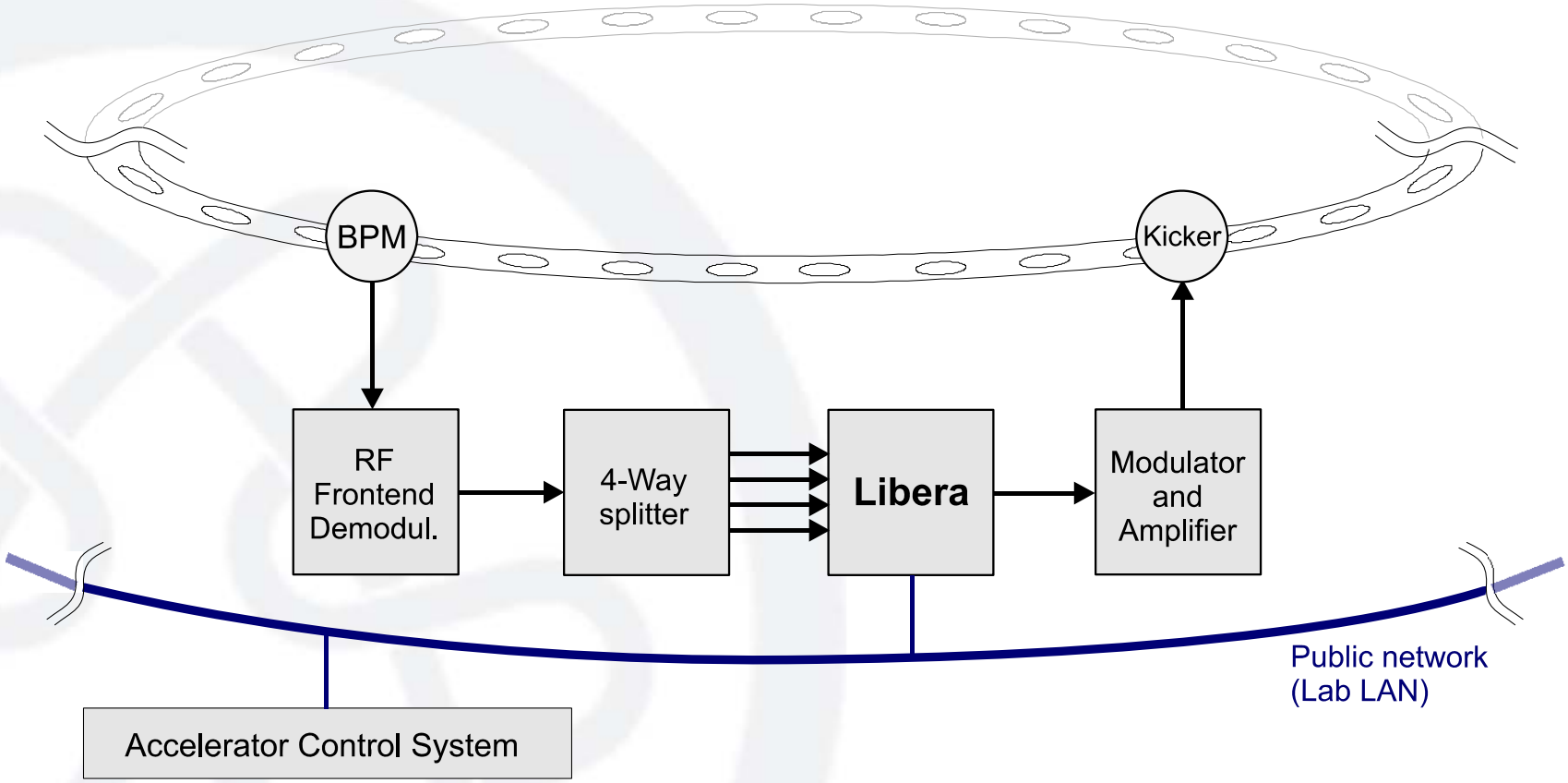
Borut Repič

Instrumentation Technologies
Slovenia

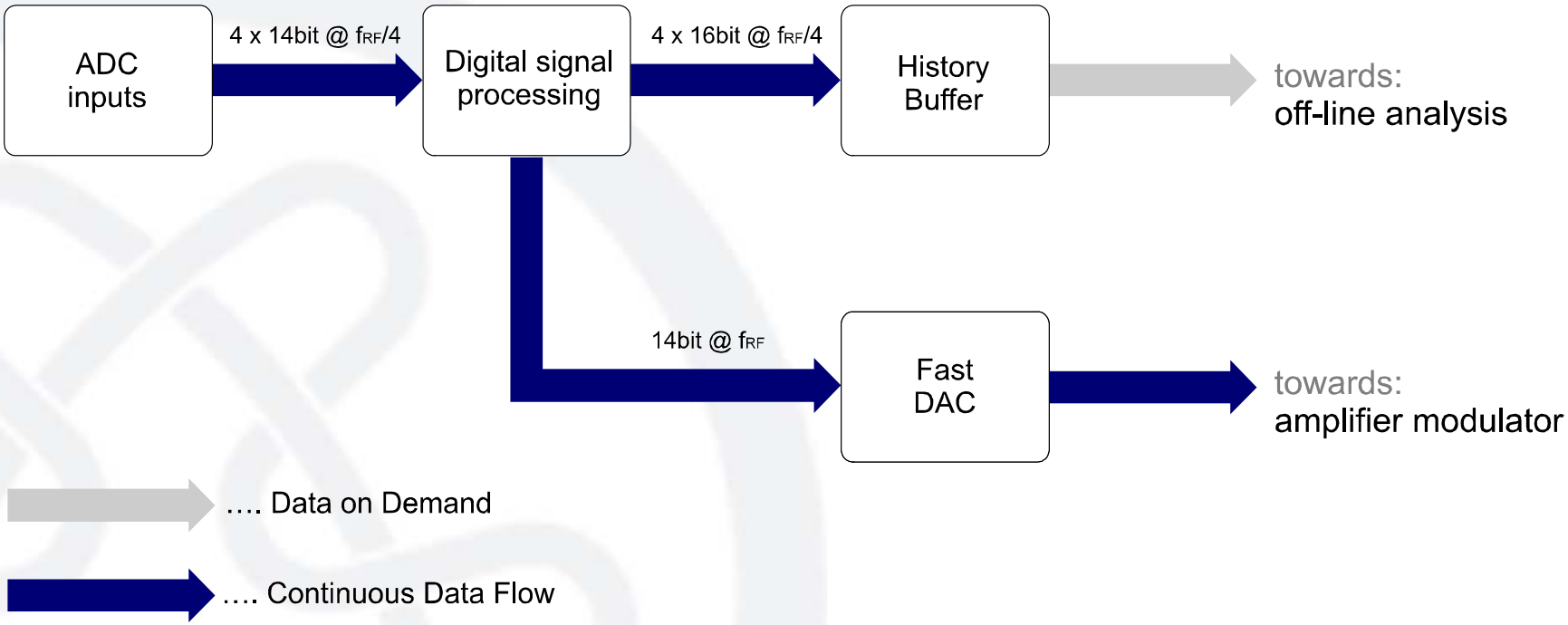
Introduction

- **Libera Bunch-by-Bunch is a platform, which provides necessary interfaces and DSP power to build bunch by bunch feedback system.**

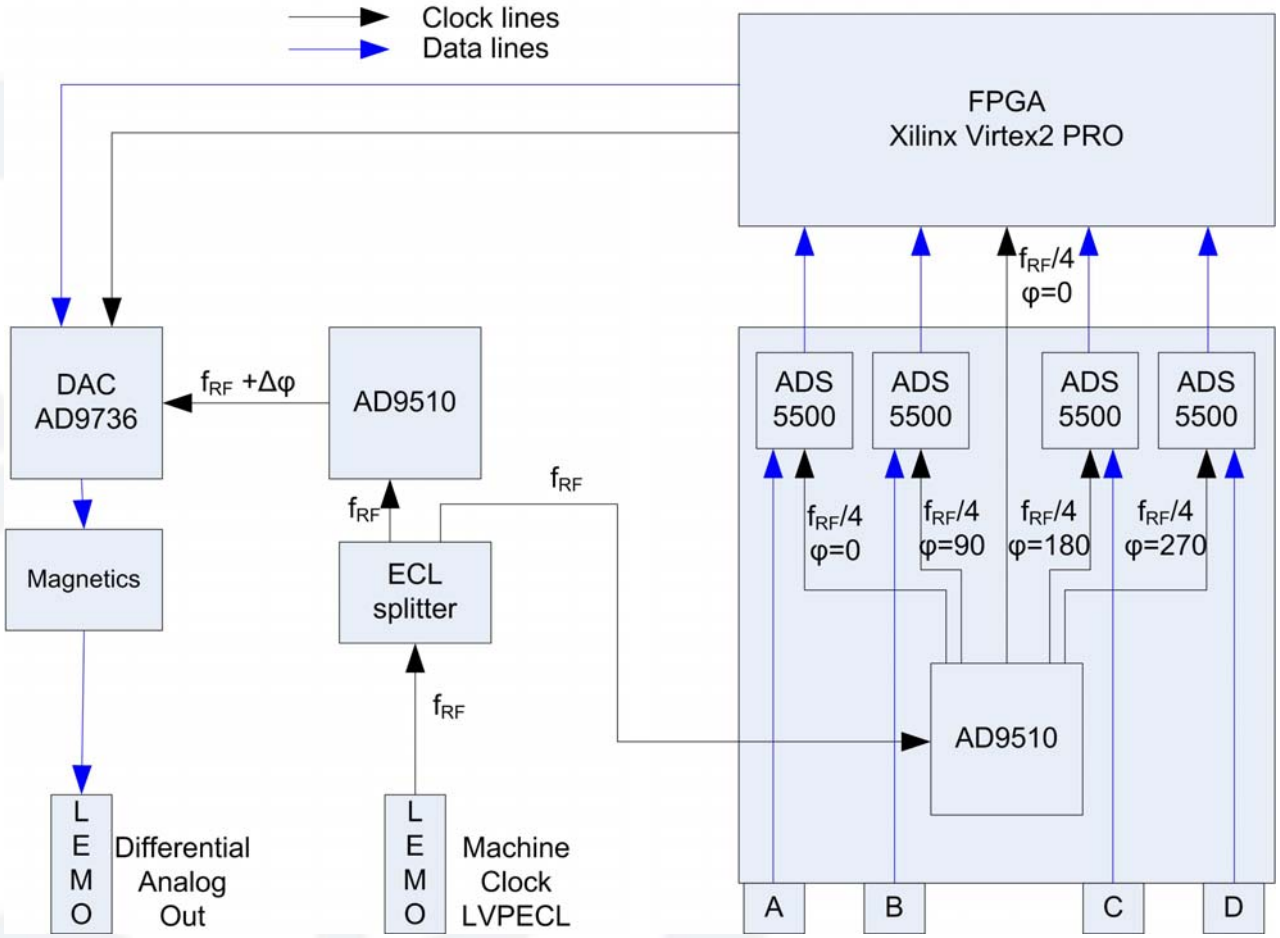
Libera in the System



Data Flow


ADC inputs
4 x 14bit @ fRF/4
Digital signal processing
4 x 16bit @ fRF/4
History Buffer
towards:
off-line analysis
14bit @ fRF
Fast DAC
towards:
amplifier modulator
…. Data on Demand
…. Continuous Data Flow

HW Interconnection

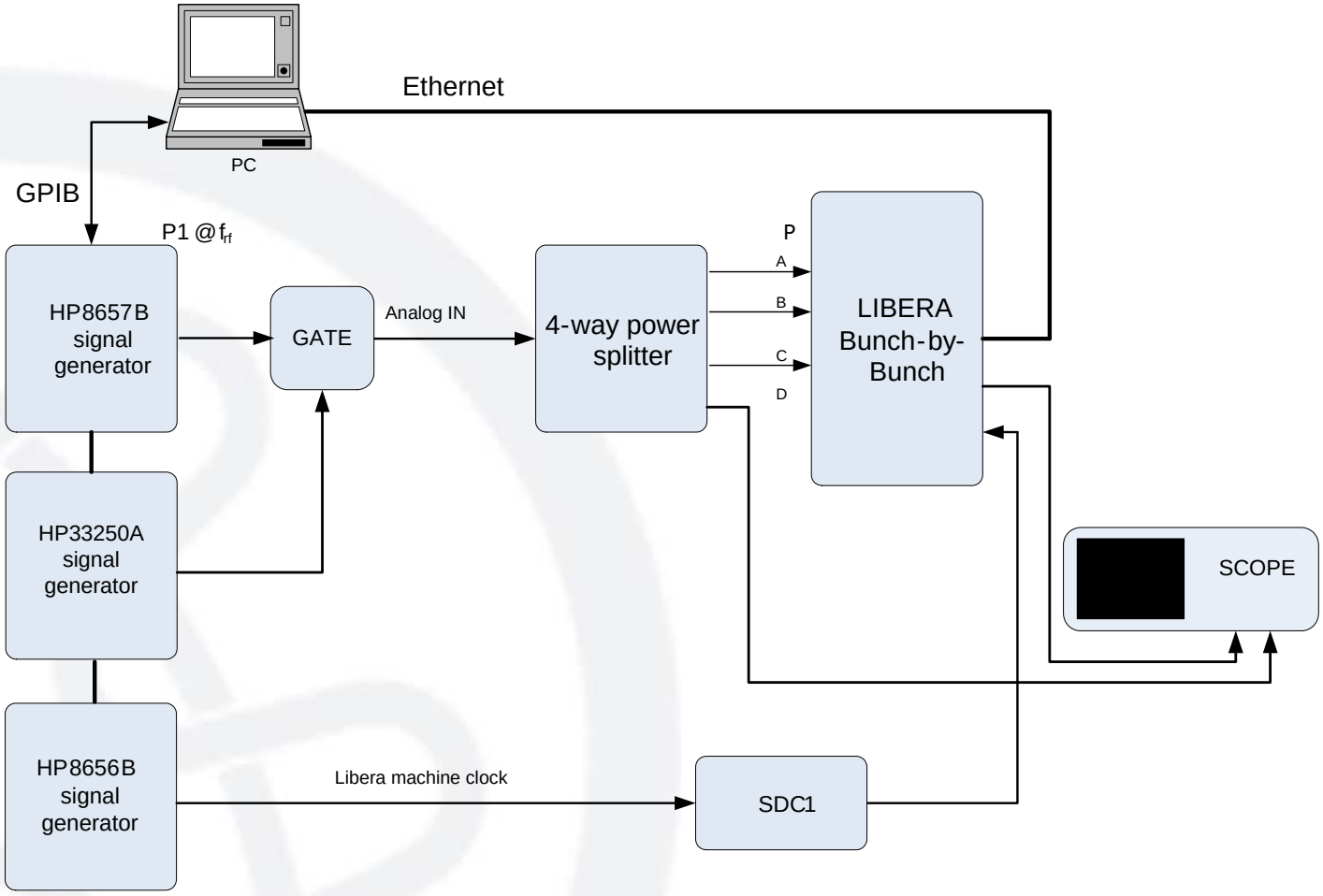


Data Path Latency

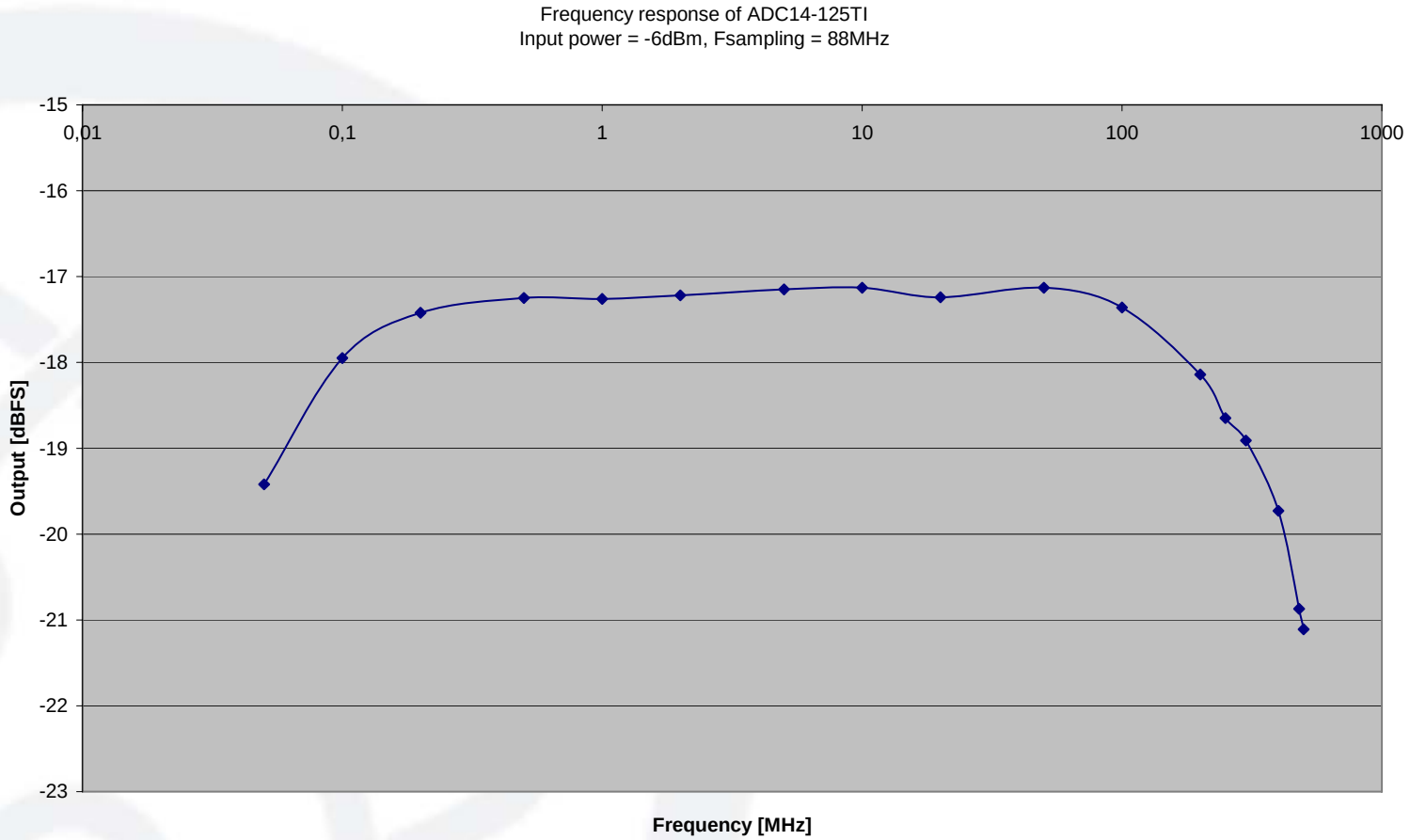
- ADC: 17CLK cycles @$f_{RF}/4$
- FPGA: 4CLK cycles @$f_{RF}/4$
- DAC: 35CLK cycles @f_{RF}

- Total: 119CLK cycles f_{RF}
  119/352MHz = 338ns
  119/500MHz = 238ns

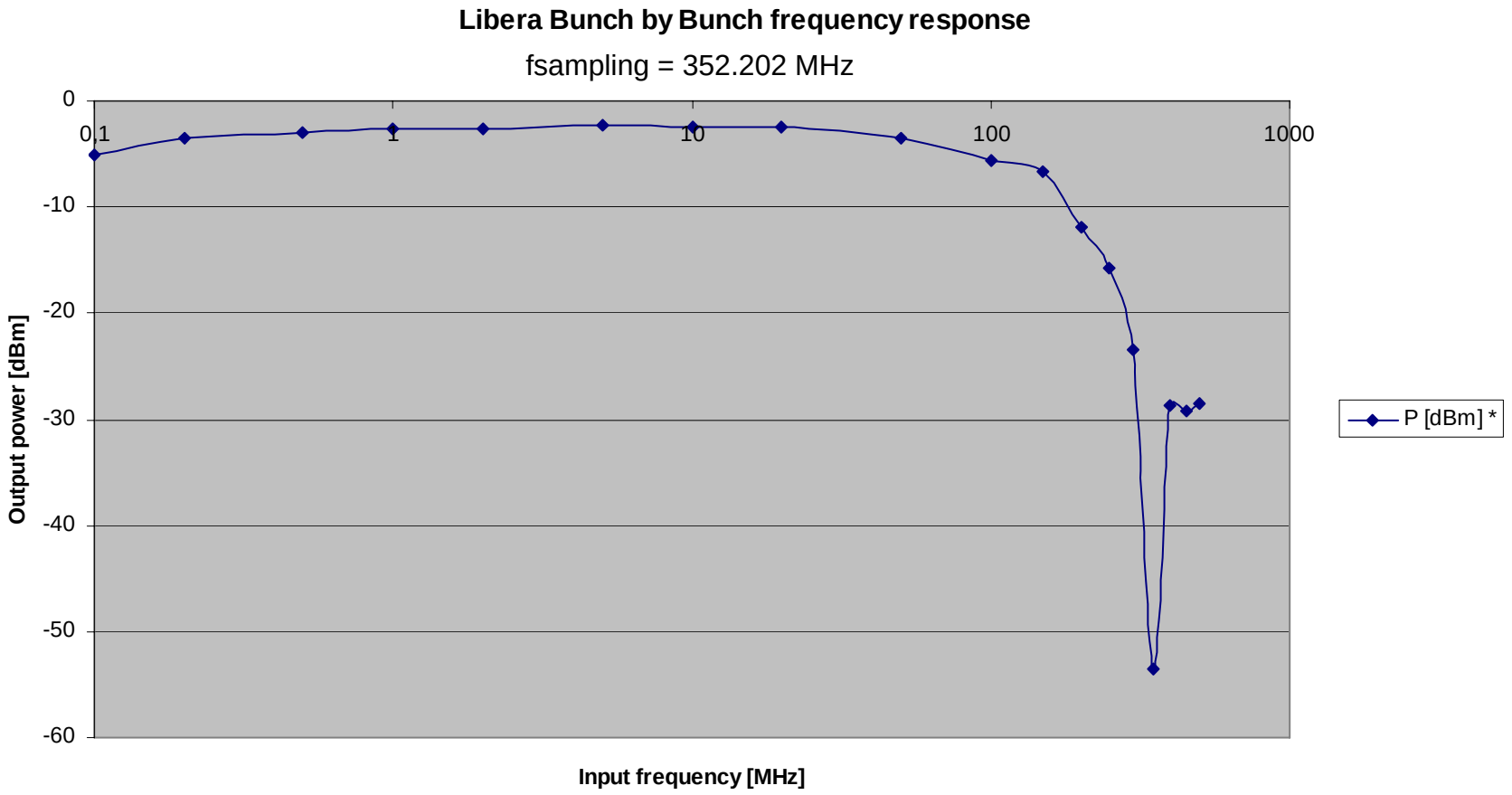
Latency Measurement



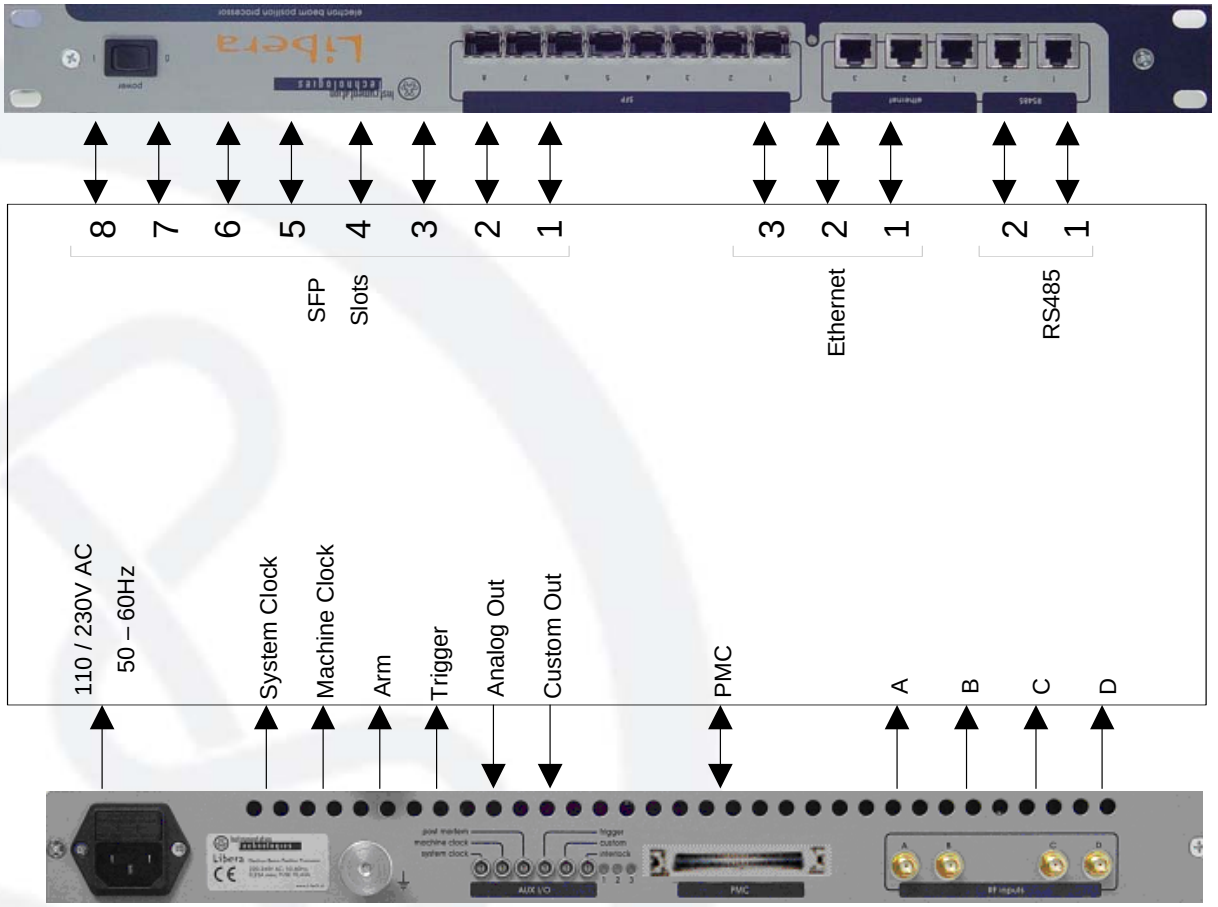
Frequency Response of Analog Front-End



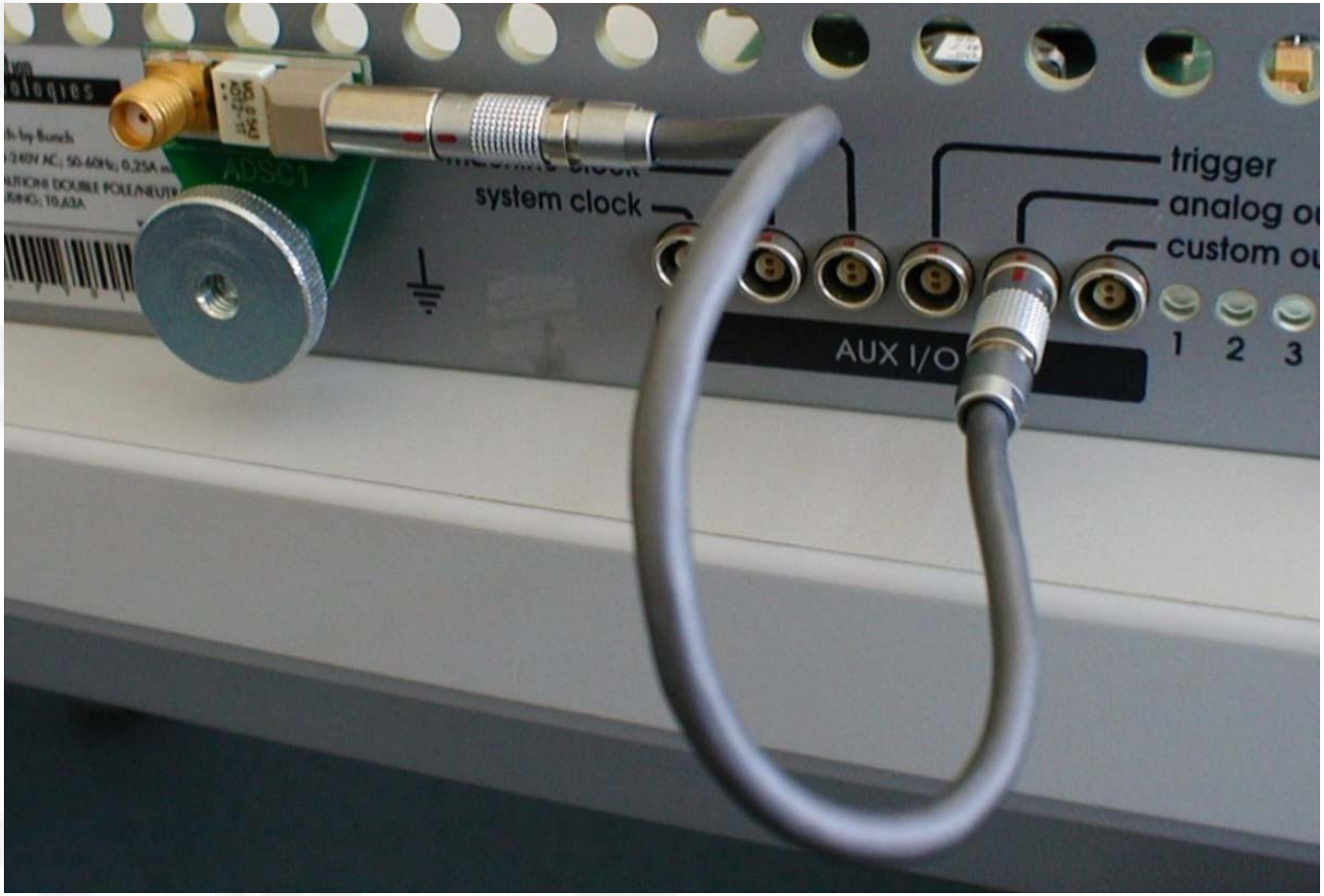
Frequency Response of the Libera Bunch-by-Bunch Unit



Interfaces

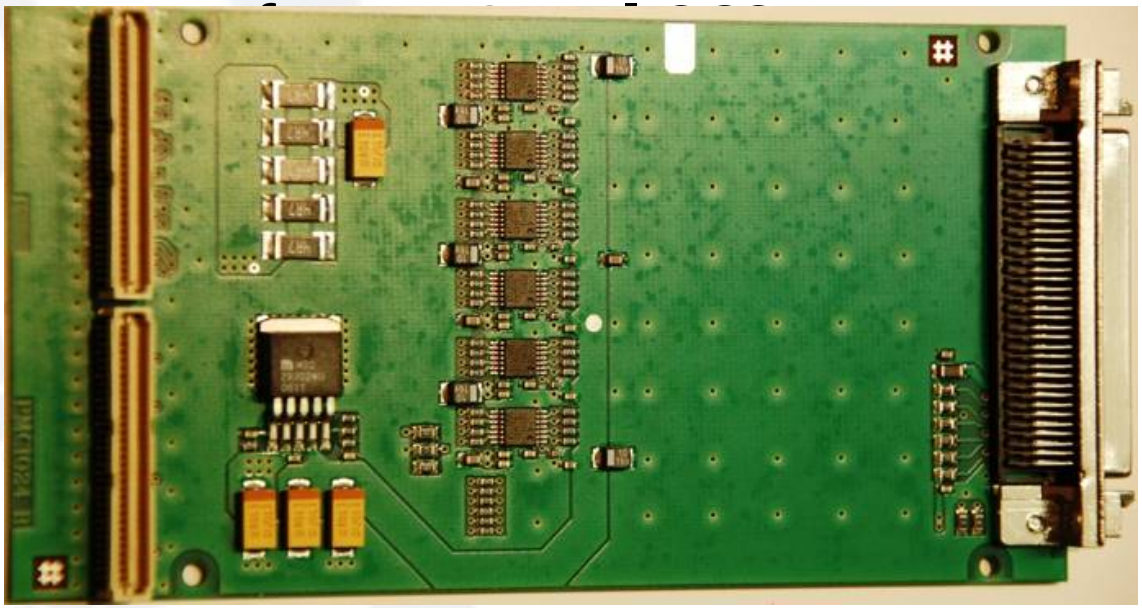

8
7
6
5
4
3
2
1
SFP Slots
3
2
1
Ethernet
2
1
RS485
110 / 230V AC
50 – 60Hz
System Clock
Machine Clock
Arm
Trigger
Analog Out
Custom Out
PMC
A
B
C
D

Single Ended Analog Output



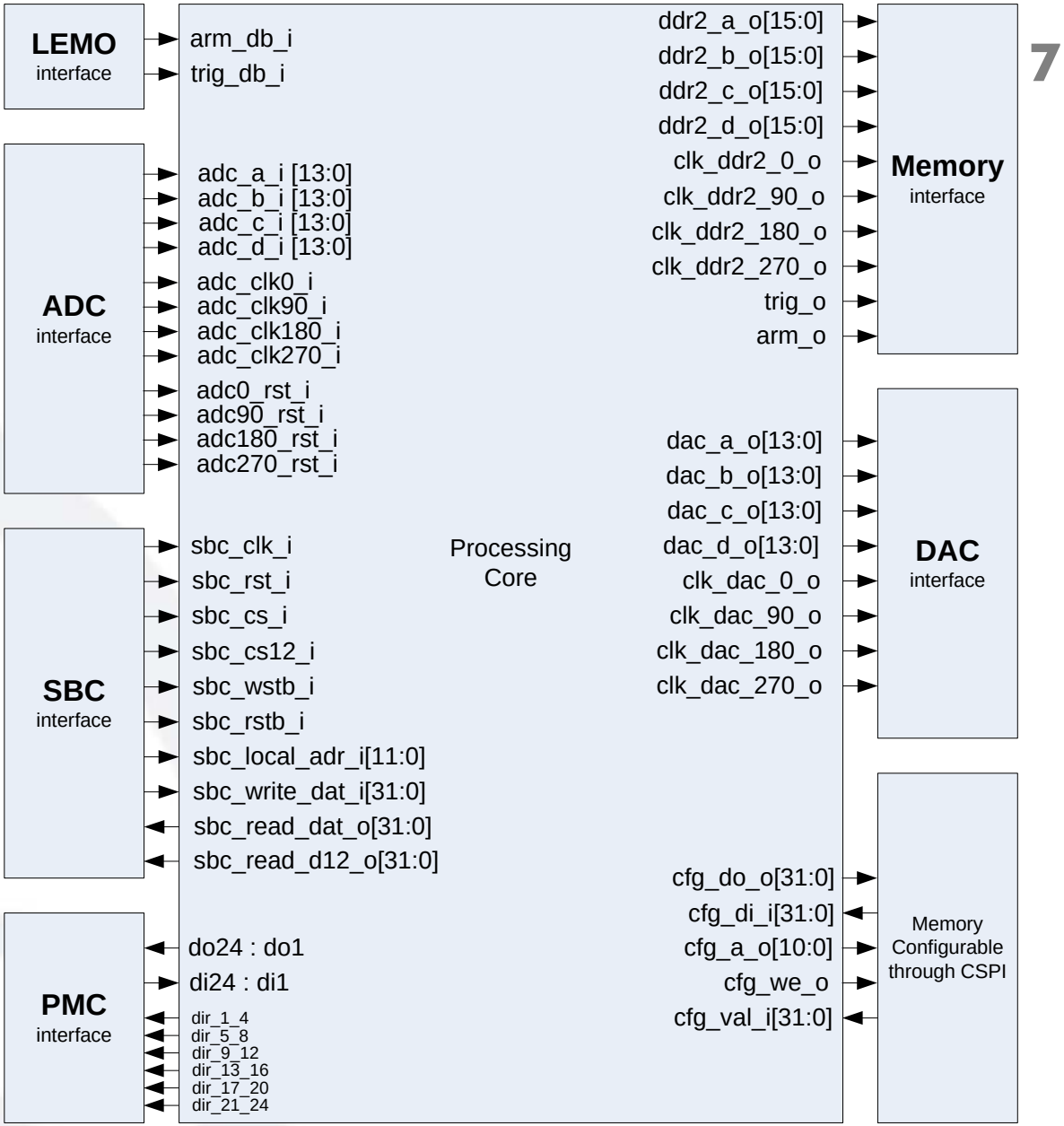
PMC I/O Module

- 24 I/O signals
- Direction control in groups of 4 signals
- GTL I/O levels



FPGA Architecture

Compatible with the System Generator, which provides system modeling and automatic code generation from Simulink and MATLAB



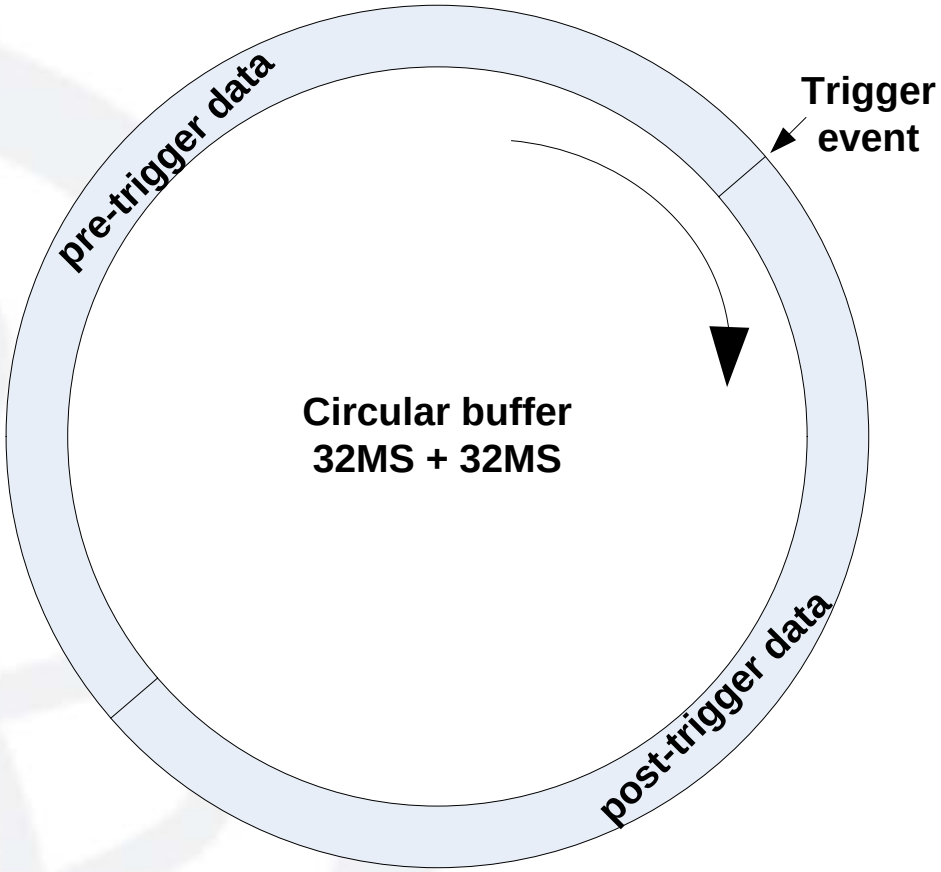
borut@i-tech.si ; www.i-tech.si Borut Repič

FPGA Features

Xilinx Virtex 2PRO XC2VP30 speedgrade -6

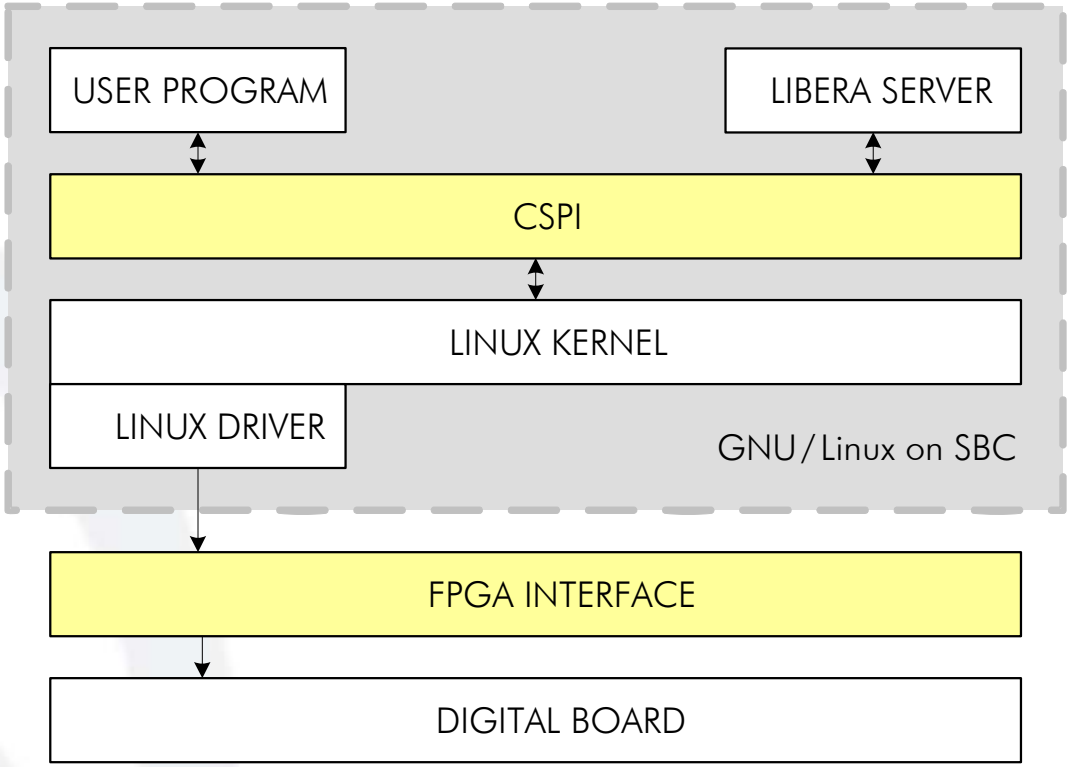
- Logic cells: 30,816
- BRAM (kbits): 2,448
- 18x18 multipliers: 136
- PowerPC processors: 2
- RocketIO transceivers: 8

Circular Buffer



Software Architecture

- **CORE:**
  - **GNU/Linux**
  - **Linux driver**
  - **CSPI**
- **EXTENSIONS:**
  - **Libera Server**
  - **Tango device**
  - **<Your Application>**



Conclusion

- Libera Bunch-by-Bunch is network attached device
- The control system interface is common to all the Libera family members
- Entire FPGA source code is supplied
- FPGA code is compatible with Xilinx System Generator
- Entire SBC software is available under GPL license including source code