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Libera Brilliance

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General about Libera Brilliance

- How does it work?
- Hardware interfaces
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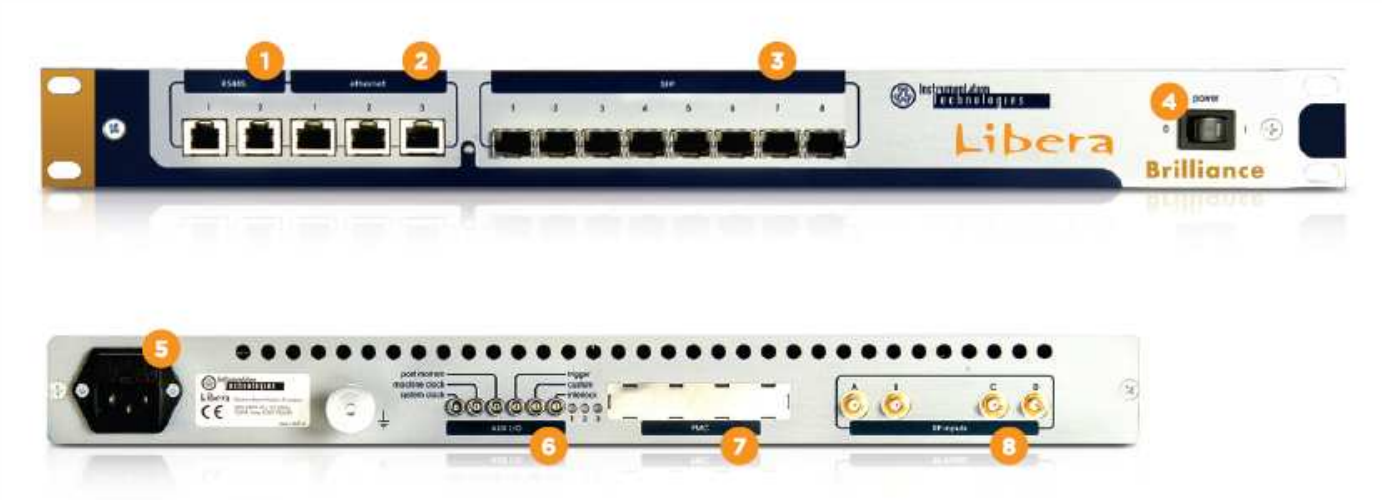
- High-level Software Architecture
- Integration into Control System
- Performance Specifications

How Does It Work?

- **Input signals come from button BPMs**
- **Four equal analog chains for analog signal processing**
- **Digitalization @ ~ 117 MHz**
- **Digital signal processing**
- **Position calculation**

Hardware Interfaces



1 … RS485 ports

2 … Ethernet ports for communication and integration into accelerator control system

3 … SFP slots are used for fast serial communication

4 … ON/OFF switch

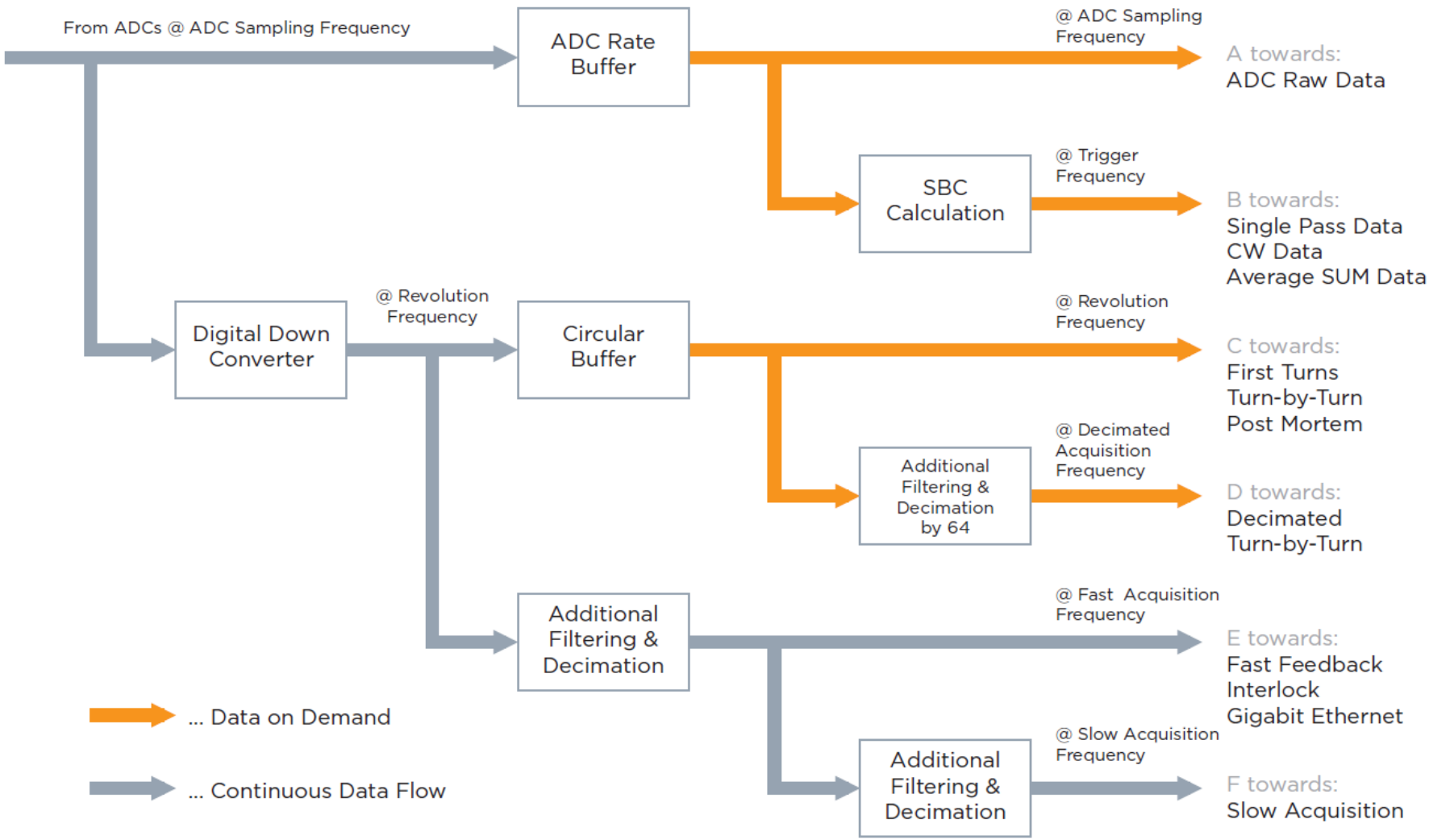
5 … Power supply

6 … Timing interfaces (synchronization, trigger, Interlock, Postmortem)

7 … PMC slot supports standard PMC boards

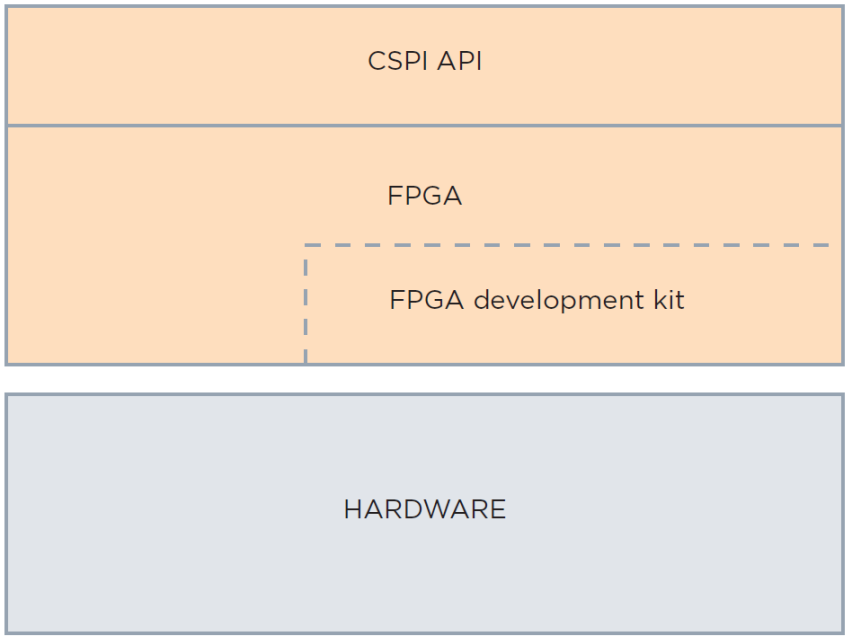
8 … RF inputs (connect to pickups)

Data Paths


From ADCs @ ADC Sampling Frequency
ADC Rate Buffer
@ ADC Sampling Frequency
A towards:
ADC Raw Data
SBC Calculation
@ Trigger Frequency
B towards:
Single Pass Data
CW Data
Average SUM Data
Digital Down Converter
@ Revolution Frequency
Circular Buffer
@ Revolution Frequency
C towards:
First Turns
Turn-by-Turn
Post Mortem
Additional Filtering & Decimation by 64
@ Decimated Acquisition Frequency
D towards:
Decimated
Turn-by-Turn
Additional Filtering & Decimation
@ Fast Acquisition Frequency
E towards:
Fast Feedback
Interlock
Gigabit Ethernet
Additional Filtering & Decimation
@ Slow Acquisition Frequency
F towards:
Slow Acquisition
... Data on Demand
... Continuous Data Flow

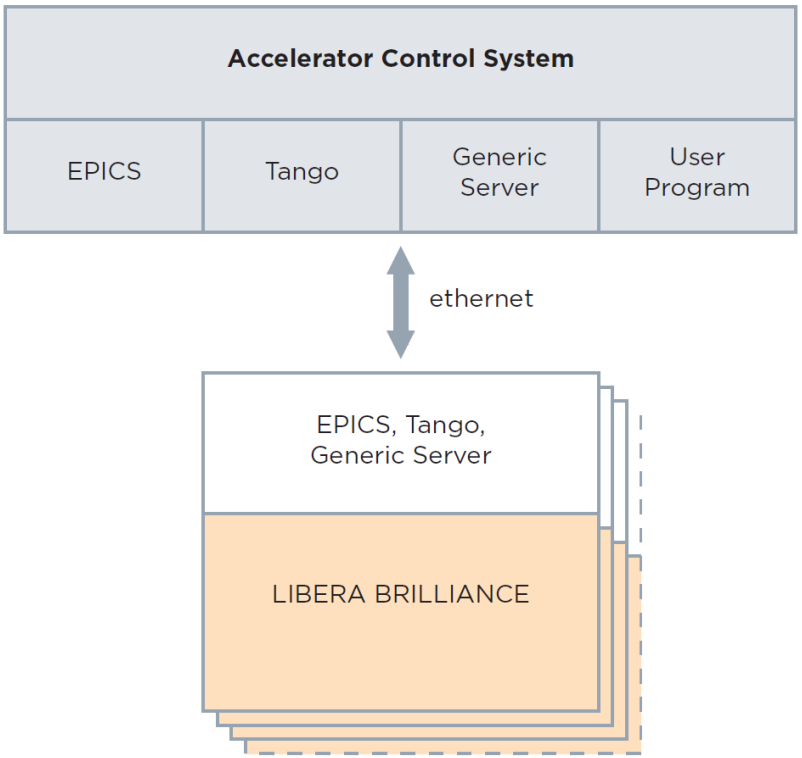
High-Level Software Architecture

- Linux, running on the SBC
- High-level C interface (CSPI API)
  - configuration
  - data streams
  - health monitoring
  - event monitoring
- Provided to users with GNU GPL license and source code
- FPGA Virtex II
- Software can be further developed by users
- FPGA development kit available



Integration into Control System

- **Data flow through Ethernet connection (data acquisitions, event delivery, health monitoring)**
- **EPICS driver for Libera Brilliance:**
  - **lightweight version, based on CSPI API**
  - **Diamond version (extra functionalities, not CSPI API based)**
- **Tango / Generic server:**
  - **source code available from Instrumentation Technologies**
  - **easy implementation based on the "libera utility" example**



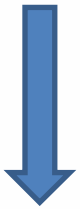
Performance Specification

Parameter	Range	Guaranteed performance, k=10mm	
		TBT=1.15 MHz	TBT=131 MHz
Resolution (turn-by-turn)	→-28 dBm	3 µm	1 µm
	→-44 dBm	15 µm	5 µm
Beam Current Dependence	0→-24 dBm	1 µm	
	0→-32 dBm	1,5 µm	
	0→-50 dBm	2 µm	
Fill Pattern Dependence	100%-20% duty cycle	1 µm	
FA Resolution	0→-20 dBm	0,25 µm	
Crosstalk		-45 dB to -70 dB	

How to Test It?

Minimum test setup must consist of:

- **Machine revolution frequency, Trigger, RF signal, …**



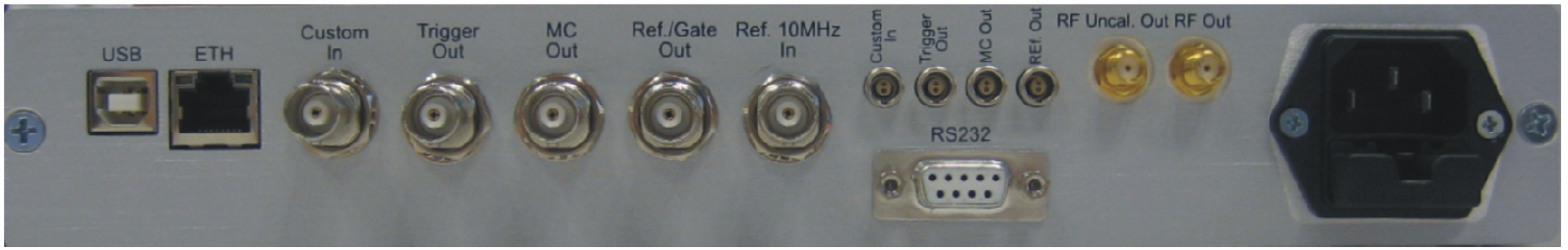
Beam-in-the-box

RF & Clock generator is new unit from Instrumentation Technologies that generates all signals.

RF & Clock Generator

- **The unit is portable**
- **It can replace 3 conventional generators (1 x RF, 2 x function).**
- **All the signals are synchronous as they are generated from the same source**
- **Synchronization to an external 10 MHz source is possible.**

front panel



back panel

History of Development

- **Software releases**
- **Basic functionalities**
- **Added features through cooperation with users**
- **Becoming the sophisticated multiple-use instrument**

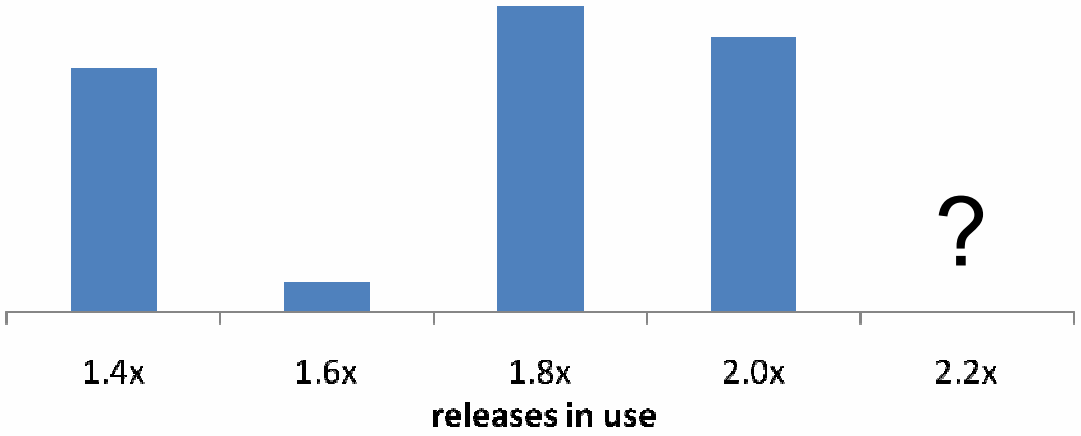
Software Releases

- **Running on Linux, armel platform**
- **Constantly upgraded**
- **Many features added from first SW releases**
- **Cooperation with users**

< 1.46 release	1.6x release	1.8x release	2.0x release
- Widely used	-Upgrade of kernel platform - New functionalities	- new PLL daemon - new parameters (switching source, delay, PM offset) - MAF design - additional Interlock features	- Major platform improvements (armel, NPTL,…) - Position calculation from ADC buffer (single pass, CW) - Spike removal on TbT, FA and SA data - Software PM triggering - Integration of Diamond CC

Future of Software Releases

- **Common users' opinion: "Too much effort to upgrade"**
- **New ideas were gathered from users**
- **Presentation on Users' meeting end of June 09**
- **Future release 2.20?**



What's New in the Last Year

- ESRF commissioning
- DESY Petra-III commissioning
- Evaluation of the latest software release at users
- We solved the problem with fans
- Users community expanded to USA
- New ideas gathered, also from users from USA
- First ideas for migrating Libera Brilliance to platform B

Proposed Features

- ADC offset compensation
- Timestamp on SA data
- Statistics calculation
- Access to DSC coefficients
- Disable notch filters when switching is off
- Improved MAF design
- ADC overflow filter
- ADC underflow detection
- Softer application of DSC coefficients
- Beam life-time measurement

Proposed Features (1)

- **ADC offset compensation**

The goal is to achieve better accuracy for single pass position measurement from ADC rate buffer, especially at lower ADC counts.

- **Timestamp on SA data**

Timestamp to be included in SA data as an additional column. This should be a counter which is reset with set-time trigger.

- **Statistics calculation**

Calculation of RMS and mean values on DD and SA data (position and amplitudes). Reduces the amount of data transfer through internal network and further calculation in the servers.

Proposed Features (2)

- **Access to DSC coefficients**

If a component in the analog chain fails (behind analog switch), the measurement is still valid if the DSC is on. This is because the input signals are all rotated through all channels.

- **Disable notch filters when switching is off**

The Notch filter in FA data chain is inserted to suppress the lower switching harmonic. If DSC is off, the Notch is not needed. Could be usable for testing purposes since during normal operation DSC should be on.

- **Improved MAF design**

MAF design to be improved. Users can set the exact ADC samples that have to be used for TbT position calculation.

Proposed Features (3)

- **Additional ADC overflow filter**

Set the number of turns with allowed ADC overflow before triggering the Interlock. Feature was developed and currently used by Diamond.

- **ADC underflow detection**

The goal is to prevent unnecessary Interlock triggering when the beam is lost. If the level is below predefined limits on all channels, the Interlock is not triggered.

- **Softer application of DSC coefficients**

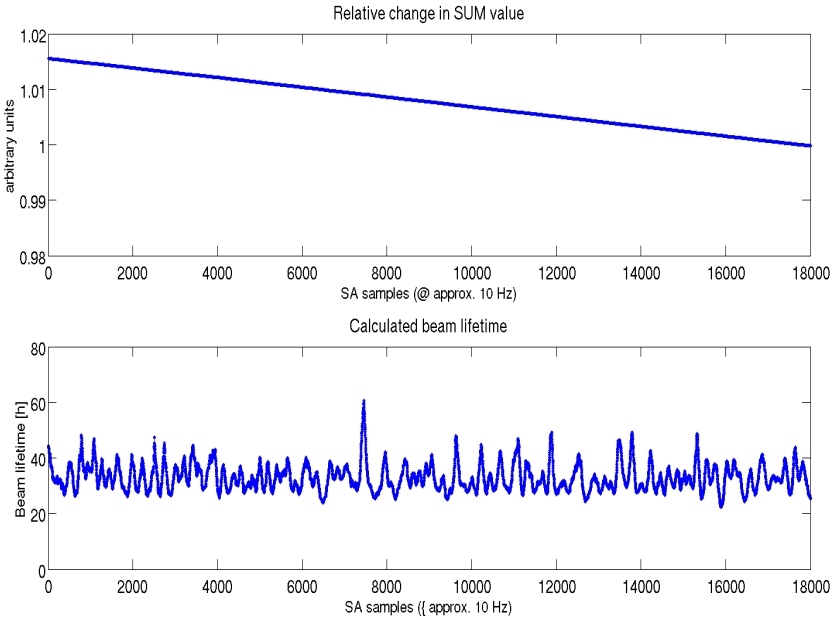
When new DSC coefficients are applied, some disturbances are seen in the amplitudes. This effect disturbs the calculation of beam life-time (for example). Application of a fraction of new coefficients will be seen as a smoother transition in the SUM value.

Proposed Features (4)

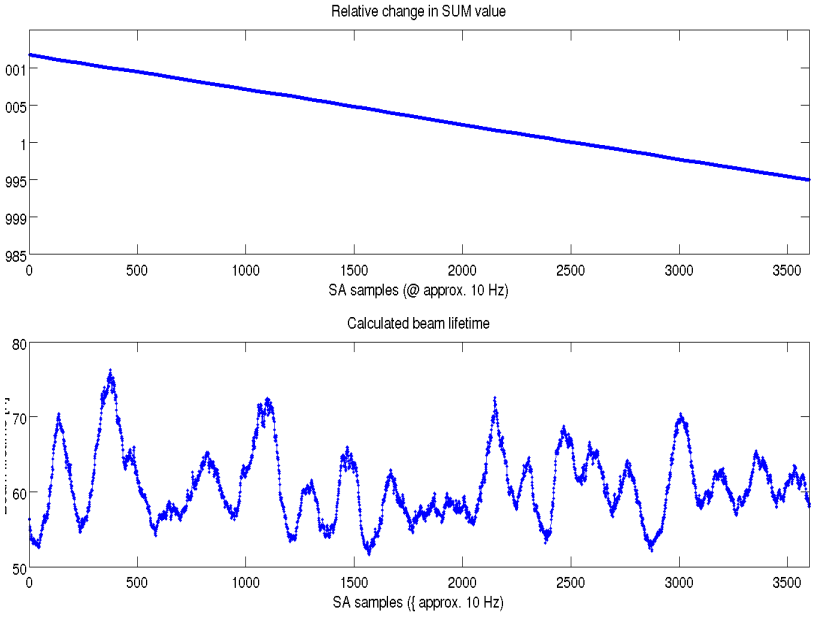
- **Beam life-time measurement**

Life-time measurement is based on the decay of the averaged SA-Sum signal (over certain period of time). Test script provided by ESRF.

case 1



case 2



What's Next?

- **Libera Brilliance is a state-of-the-art instrument**
- **Unification of software interface**
- **Retain compatibility of platforms A and B**
- **Software release 3.0 with MCI instead of CSPI API**
- **Continuous support for all users**

Thank you for your attention.