

Libera

Libera Spectra

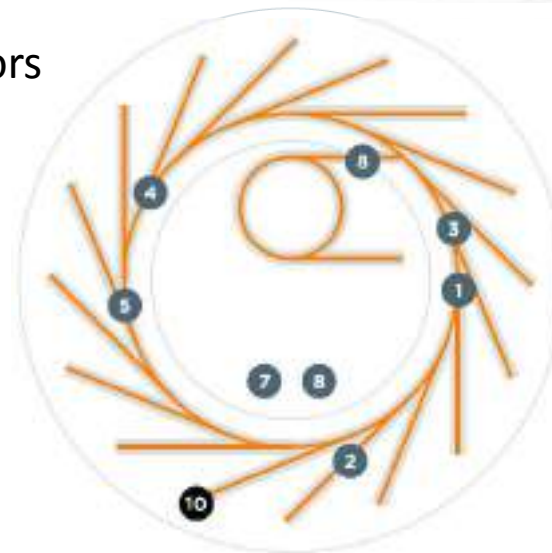
Elvis Janežič, Libera Workshop, October 2012, Solkan

What is Libera Spectra?

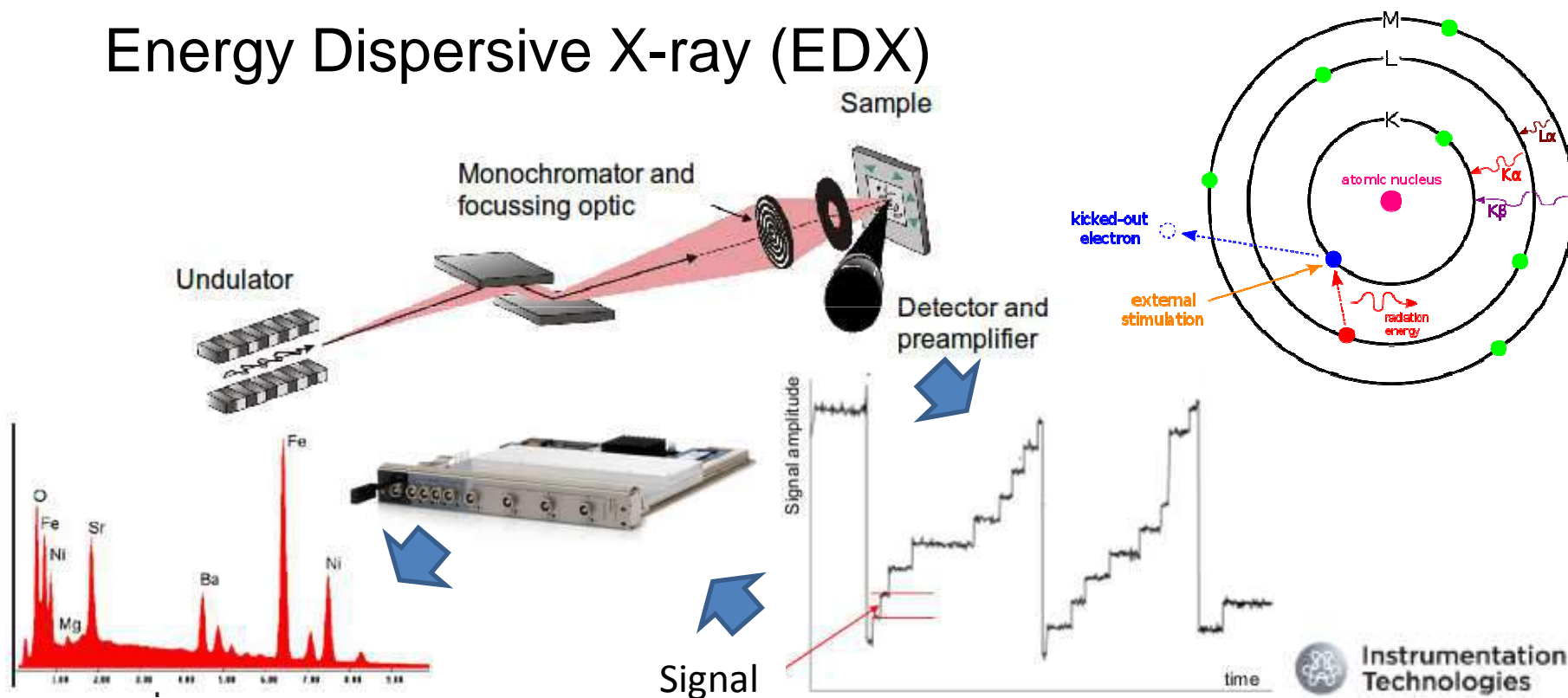
Libera Spectra is a high-performance digital pulse processor intended for spectroscopy studies.

It is designed for semiconductor detectors in energy dispersive x-ray experiments.

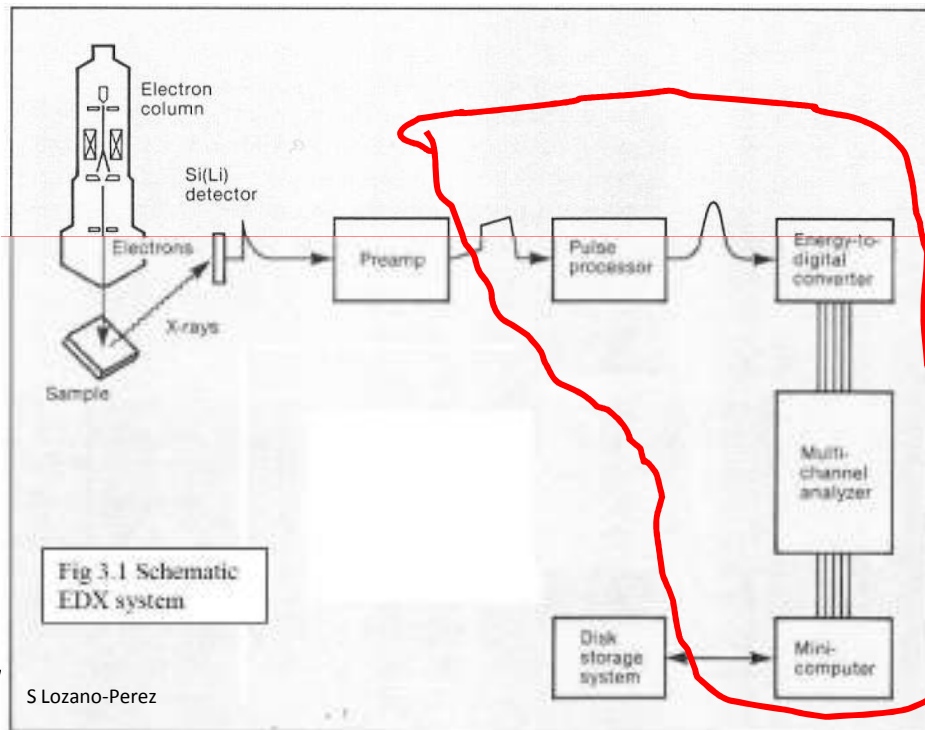
On synchrotrons it is located in the experimental hutch on the end of the beamline.



Energy Dispersive X-ray (EDX)



DPP, Detector readout, MCA, DSP...?



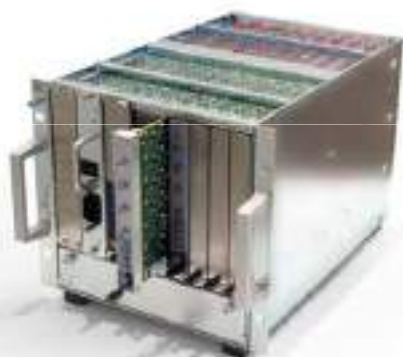
Analog system

- Pulse processor
- Energy to digital converter
- Multichannel analyzer
- Mini computer

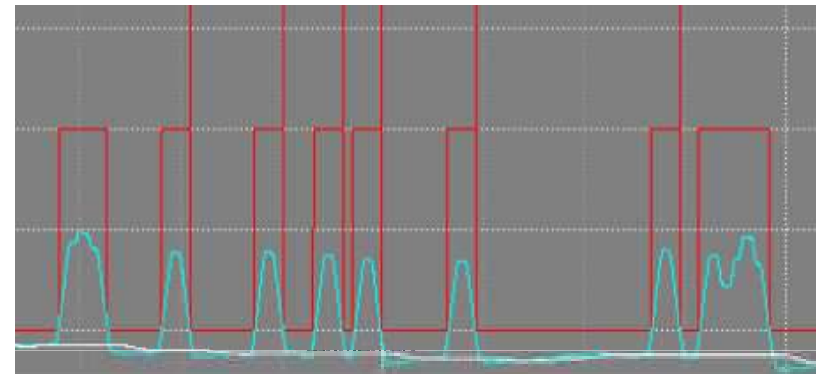
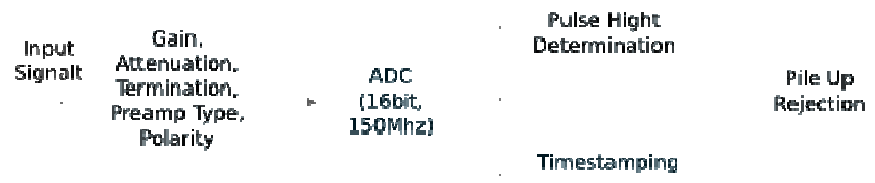
Digital system

- Libera Spectra
- SBC

Measurement system

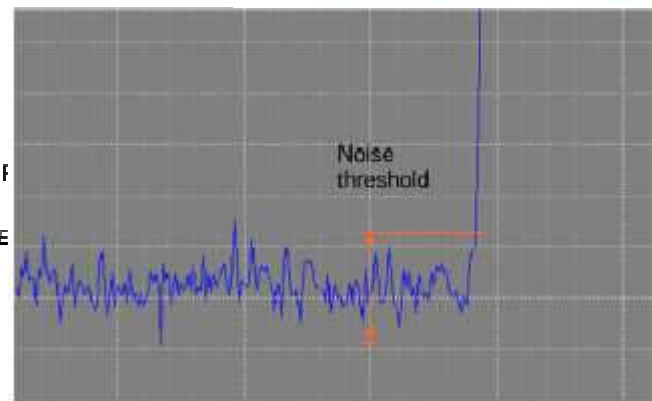


How does it work?



ANALOGUE CHAIN

LIBERA SPE



User Setting

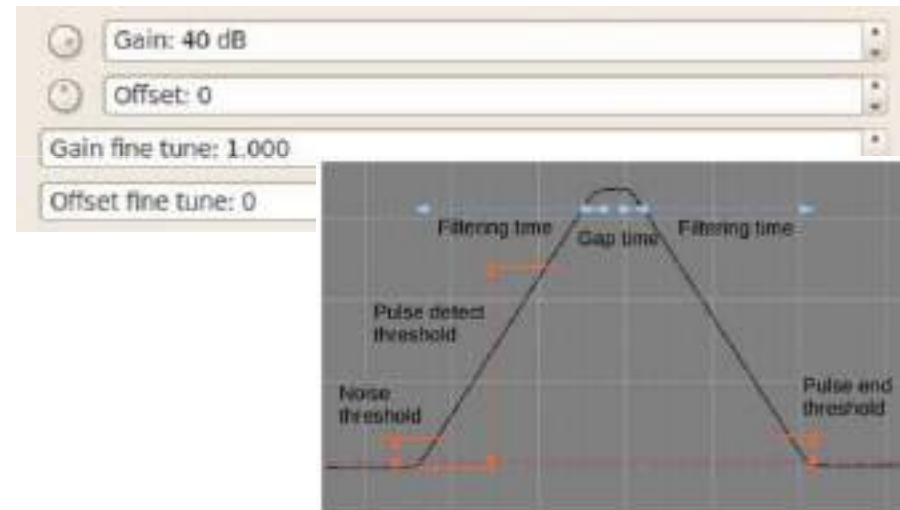
```
<node> boards.s5cX.channels.Y.hw.preamp.polarity
```

Basic:

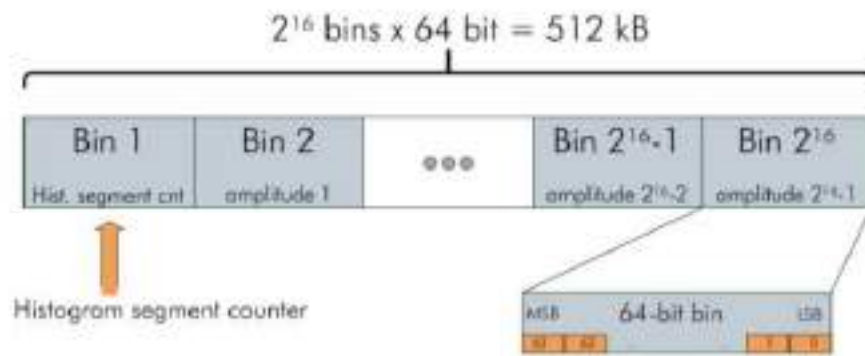
- Polarity: Positive or Negative
- Gain: 40dB
- Filtering time: 100ns to 10us
- Tresholds: Noise, Pulse Detection

Fine tuning:

- Gap time, Pulse Reset, Bias....

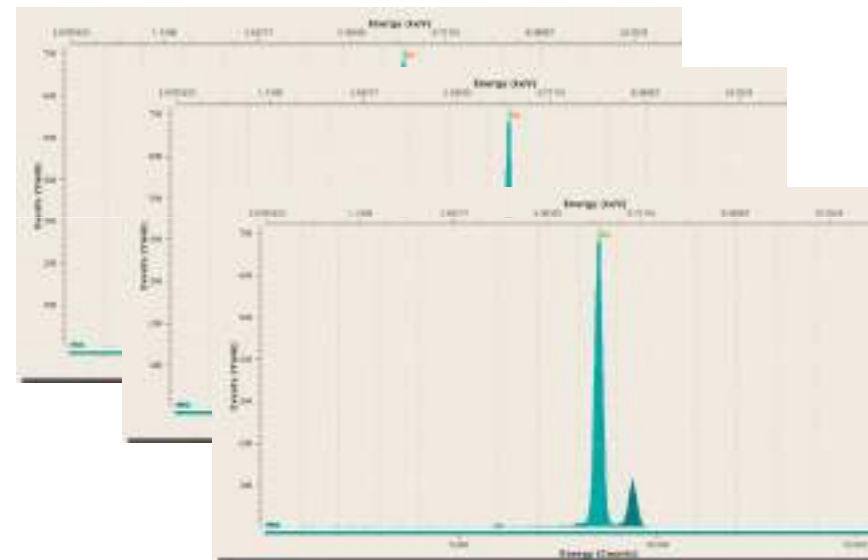


Histogram and Time Segmented Histogram



Time Segmented Histogram:

- On trigger records a histogram
- X- mapping



List Mode and Coincidence List Mode

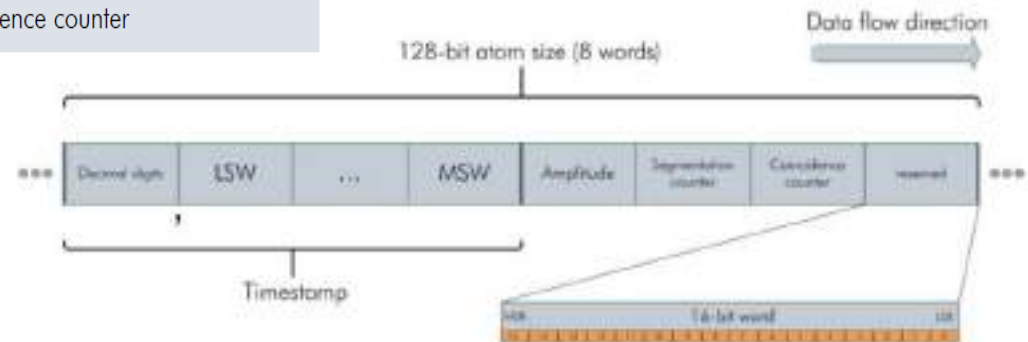
List mode:

- Huge amount of data

Coincidence List Mode:

- Records pulses before and after the coincidence trigger
- Less data

| |
|------------------------------------|
| Event in list mode |
| Pulse timestamp [ADC clock cycles] |
| Pulse amplitude [ADC counts] |
| Segmentation counter [counts] |
| Coincidence counter |



Statistics

- Basic statistics
- ROI
- FWHM
- Graph Calibration: ADC counts to eV
- Binning: 256 to 2^{16}

Statistics

Real time [ms]
Live time [ms]
Pile-up dead time [ms]
Reset dead time [ms]
Dead time [%]
Input events
Output events
ICR
OCR
OCR/ICR[%]

Specifications 1/2

Analog input channels: 4 @ 50 Ω or 500 Ω

Signal swing: -5V to 5V

Digital input/output channels: 4

ADC frequency (for sampling analog input signals): 100 – 160 MHz

ADC granularity (or sampling analog input signals): 16 bit



Specifications 2/2

Data processing:

- Xilinx Virtex 6 FPGA
- SBC (Intel i5) with 4GB RAM

Data throughput (Gigabit Ethernet): 1Gb/s



Benefits 1/2

Good resolution (FWHM):

- Low electronic added noise
- 16bit ADC

Scalable:

- 4 input channels per instrument
- Grouping up to 10 instruments in a single MTCA.4 system

Fast:

- Up to 1MCPS for all channels
- Filtering time from 100ns



Benefits 2/2

Applications:

- Histogram,
- Time Segmented Histogram
- List Mode
- Coincidence List mode

Libera BASE framework :

- possibility to add additional applications
- Custom made algorithms

Control system integration:

- Custom GUI
- EPICS
- MCI

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