Libera

# The Libera LLRF
# (Introduction, applications and recent development.)

*Robert Černe, Libera Workshop, October 2012, Solkan*

# Outline

- **Product philosophy**
- **Key characteristics**
- **Overview of the hardware**
- **Overview of the software architecture**
- **Implemented DSP algorithms with field application examples**
- **Recent development**
- **Conclusions**

# Philosophy behind the product offering

- **Facts about LLRF systems**
  - *LLRF is a vast area*
  - *Each application is unique*
- **Product offering approach**
  - *Building blocks (hardware, digital signal processing, software)*
  - *Collaboration with the customer to determine the exact requirements*
  - *Design and development of missing functionality*
  - *Delivery of the solution with training and commissioning*

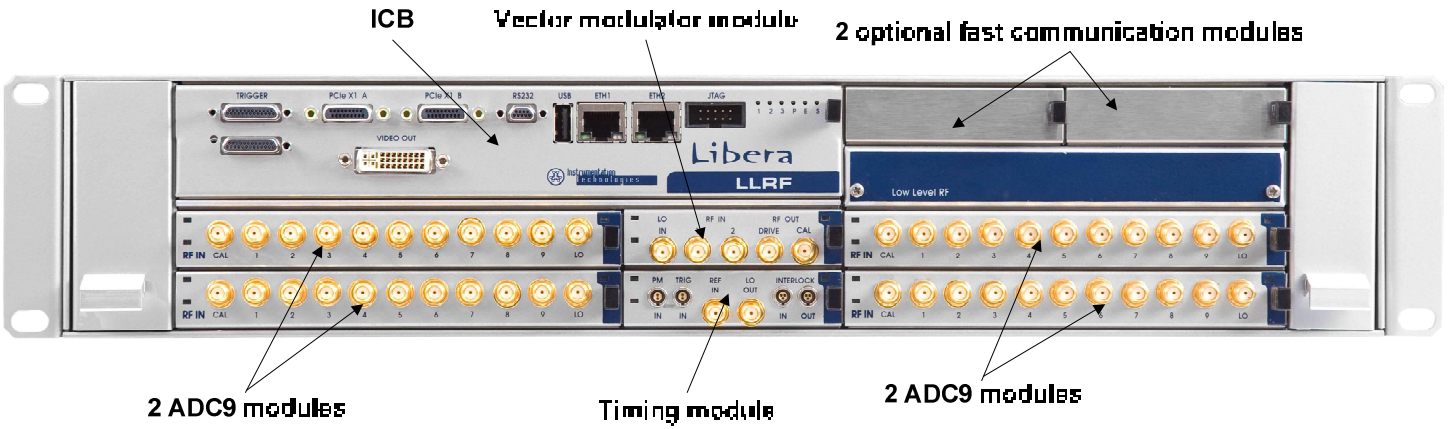
# Key characteristics 1/2

- **Robustness:**
  - *Reliable hardware operation (chassis health monitoring)*
- **RF system safety**
  - *Reliable interlock system*
  - *Operational procedures*
- **High performance**
  - *Added amplitude and phase noise*
  - *Compensation of the temperature drifts of the LLRF receiver*
  - *Signal monitoring*
  - *Application algorithm execution*

# Key characteristics 2/2

- **Flexible operation:**
  - *Local and remote operation using a GUI*
  - *Support for integration in the accelerator's control system*
- **Support for customization**
  - *Hardware (support for different frequencies)*
  - *Signal processing (FPGA development kit)*
  - *Application software (software development kit)*
- **Based on standards**
  - *µTCA*
  - *AMC*

# Hardware architecture



# Interconnection Board (ICB)

- **Implements MCH functions and acts as a COM Express carrier board.**
- **Power distribution.**
- **High throughput PCIe switch fabric.**
- **Distribution of switch fabric clock.**
- **IPMI management of AMC modules.**
- **Integrated COM Express module with powerful CPU.**
- **FPGA for configuration and control of ICB hardware.**
- **Interfaces: JTAG, RS232, host USB, management Ethernet, 2x PCIe, 2x LXI, DVI, USB and 2x GbE.**

# LLRF receiver AMC module (ADC9)

- **Consists of digital and RF PCBs.**
- **9 RF input channels, LO (Local Oscilator) input and calibration input.**
- **Down conversion technique used.**
- **9 x 16 bit ADCs (up to 130 MS/s), raw acquisitions (DDR RAM up to 8 Gbits)**
- **Virtex 5 FPGA .**
- **ARM processor with IPMI support.**
- **PCIe endpoint implemented in FPGA.**
- **8x PCIe link to the card edge connector.**
- **Dedicated low latency LVDS links to the card edge connector.**

# LLRF transmitter AMC module (VM)

- **Consists of digital and RF PCBs.**
- **2 RF output channels, 2 RF input channels and LO input.**
- **Up/Down conversion technique used.**
- **2 x 14 bit double DACs (up to 260 MS/s), 2x 16 bit ADCs raw acquisitions (DDR RAM up to 8 Gbits)**
- **Virtex 5 FPGA .**
- **ARM processor with IPMI support.**
- **PCIe endpoint implemented in FPGA.**
- **4x PCIe link to the card edge connector.**
- **Dedicated low latency LVDS links to the card edge connector.**



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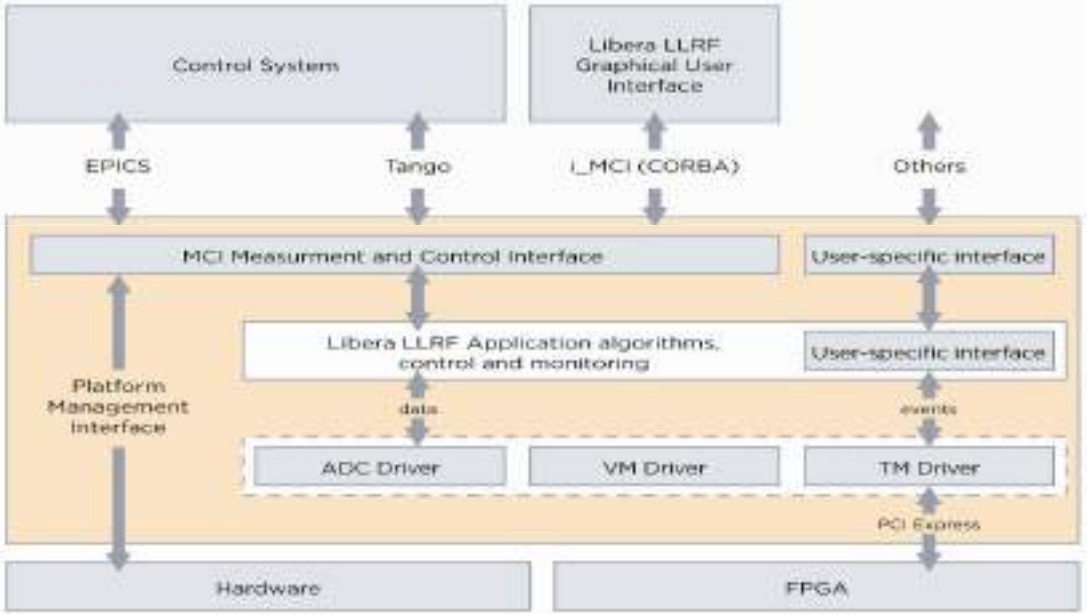
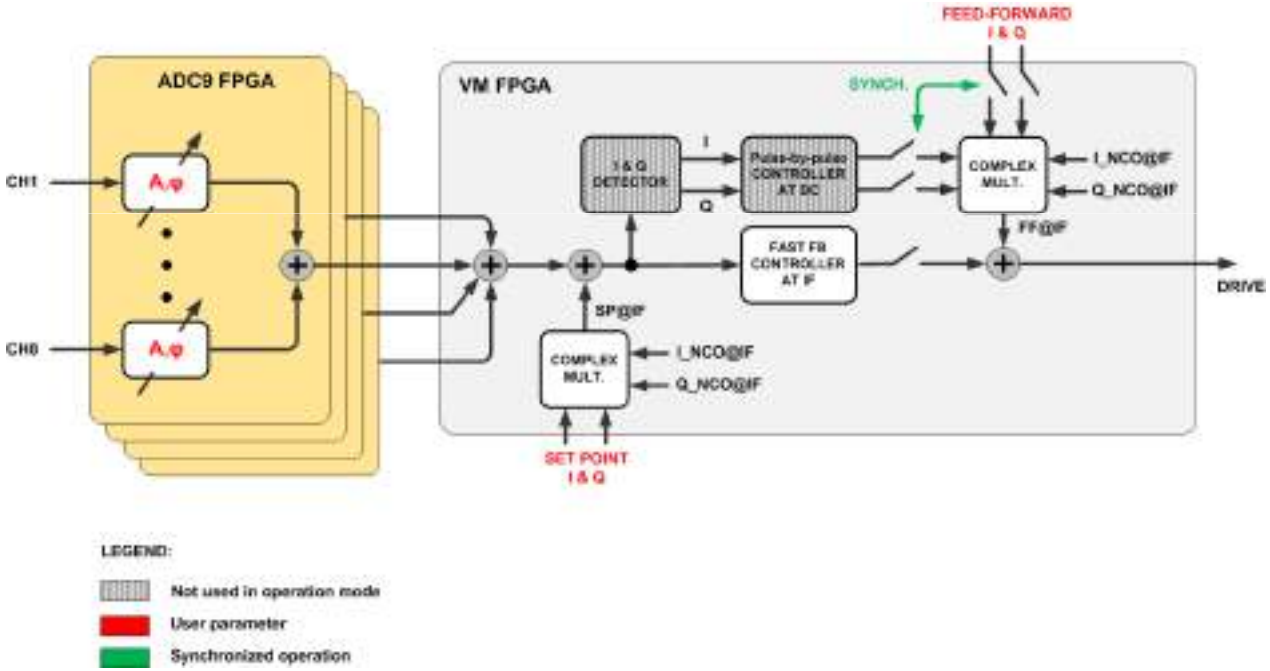
# Timing AMC module (TCM)

- **Consists of digital and RF PCBs.**
- **MO (Master Oscillator) input.**
- **LO (Local Oscillator) generation and output.**
- **Sampling clock generation and distribution to AMC modules.**
- **Interlock input and output.**
- **2x trigger input and distribution to AMC modules.**
- **ARM processor with IPMI support.**
- **Lattice FPGA .**
- **PCIe endpoint implemented in FPGA.**
- **1x PCIe link to the card edge connector.**

# Software architecture



# Fast feed-back with feed-forward




**Used by EMMA in Daresbury:**

- **non-scaling FFAG**
- **19 RF cavities**
- **Normal conducting cavities**
- **Pulsed operation mode**
- **1600 μs pulse length**
- **3 – 20 Hz repetition rate**
- **1.3 GHz RF frequency**

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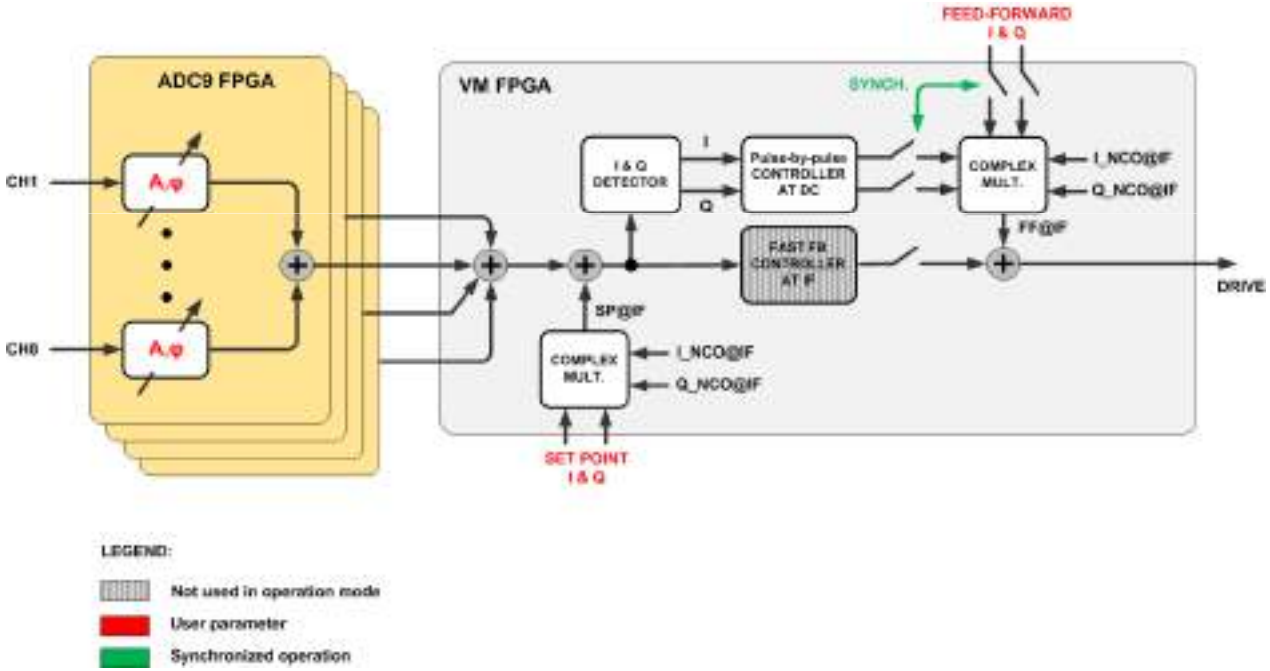
# Pulse-by-pulse feed-back




**Delivered to CANDLE in Yerevan:**

- **Injector LINAC**
- **Travelling wave structure**
- **1 RF structure per LLRF**
- **Pulsed operation mode**
- **1 μs pulse length**
- **2 Hz repetition rate**
- **3 GHz RF frequency**

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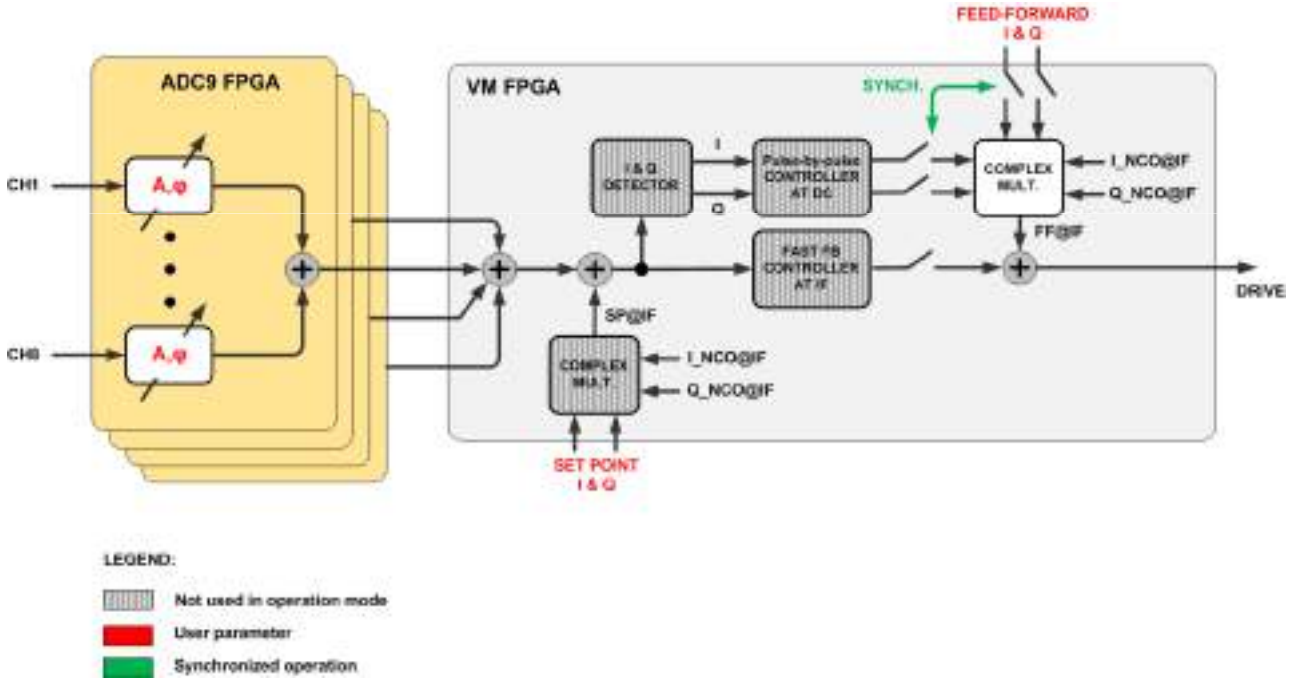
# Transfer function measurement




**Used at DESY in Hamburg:**

- **Test stand for waveguides and power amplifiers**
- **Measurements performed at up to 24 different locations**
- **Pulsed operation mode**
- **1350 µs pulse length**
- **30 Hz repetition rate**
- **1.3 GHz RF frequency**

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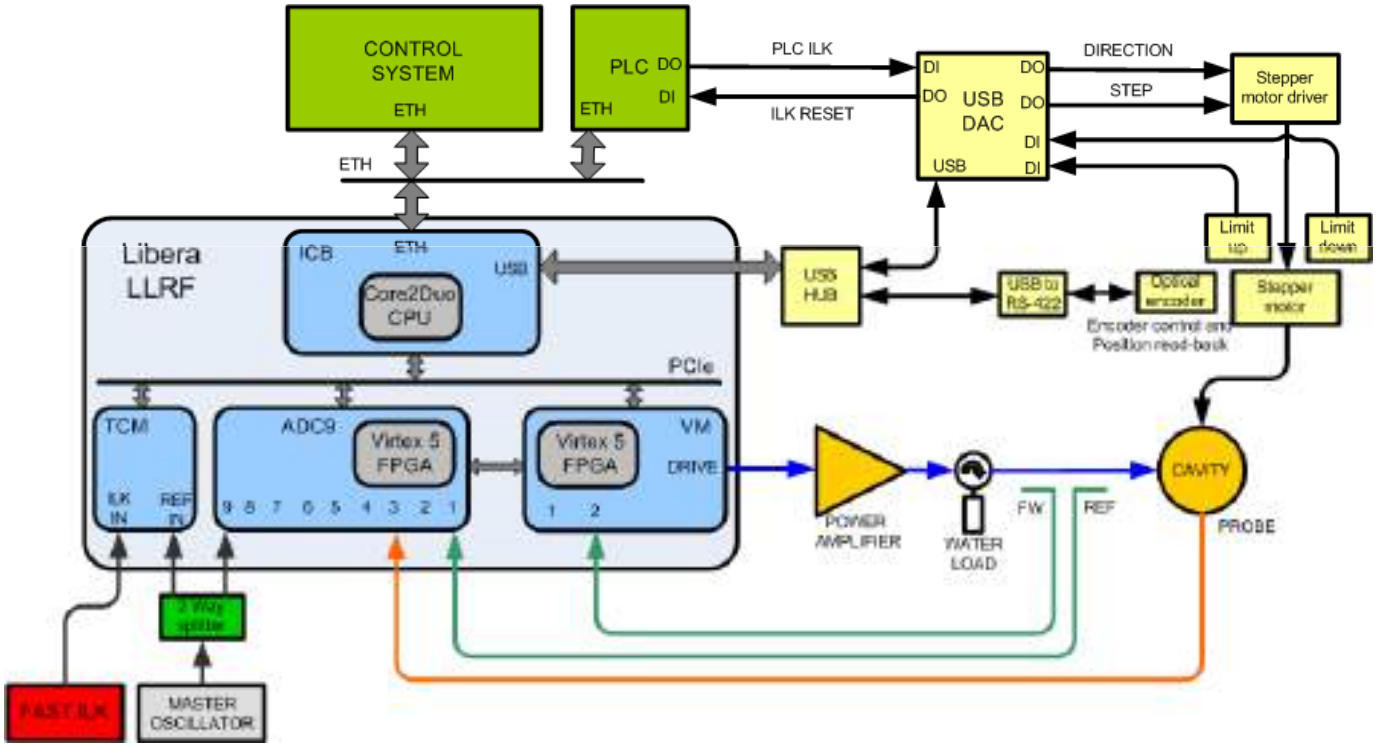
# Recent hardware topology design




- **External interfaces using USB DAC**
- **Second loop for the power amplifier**

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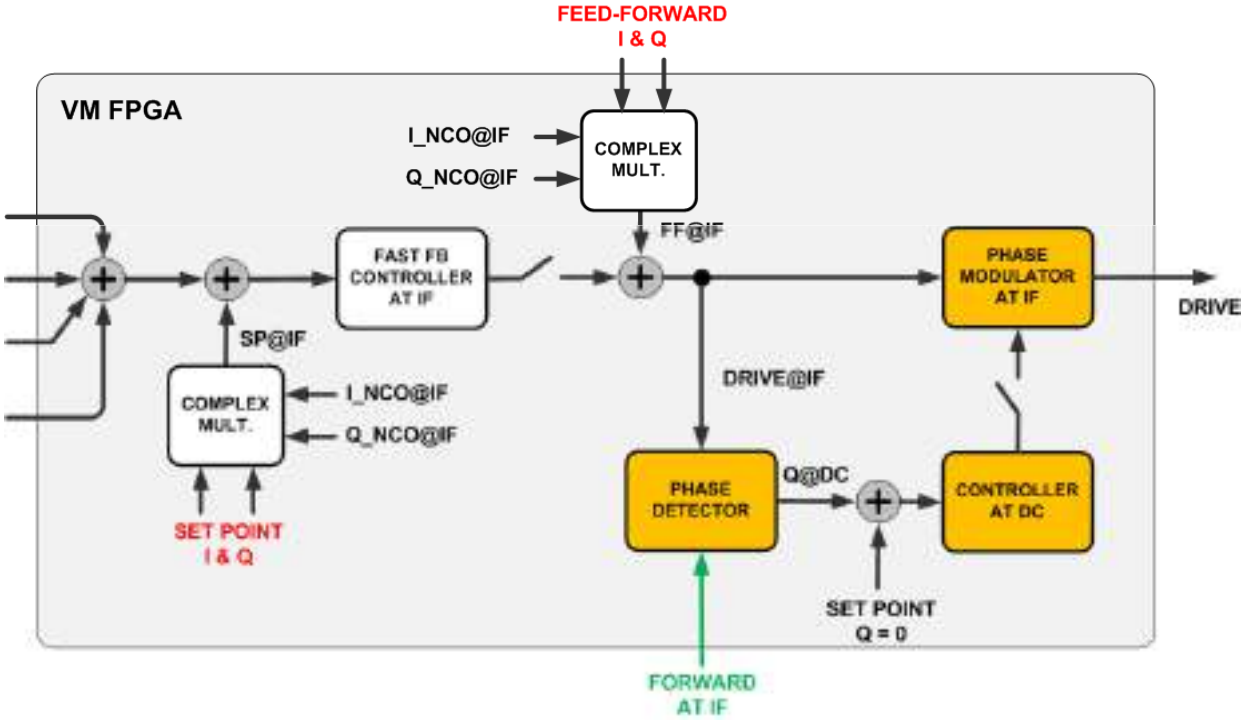
# Power amplifier phase loop 1/2




- **Using additional input on the VM module**
- **Efficient implementation without phase calculation**

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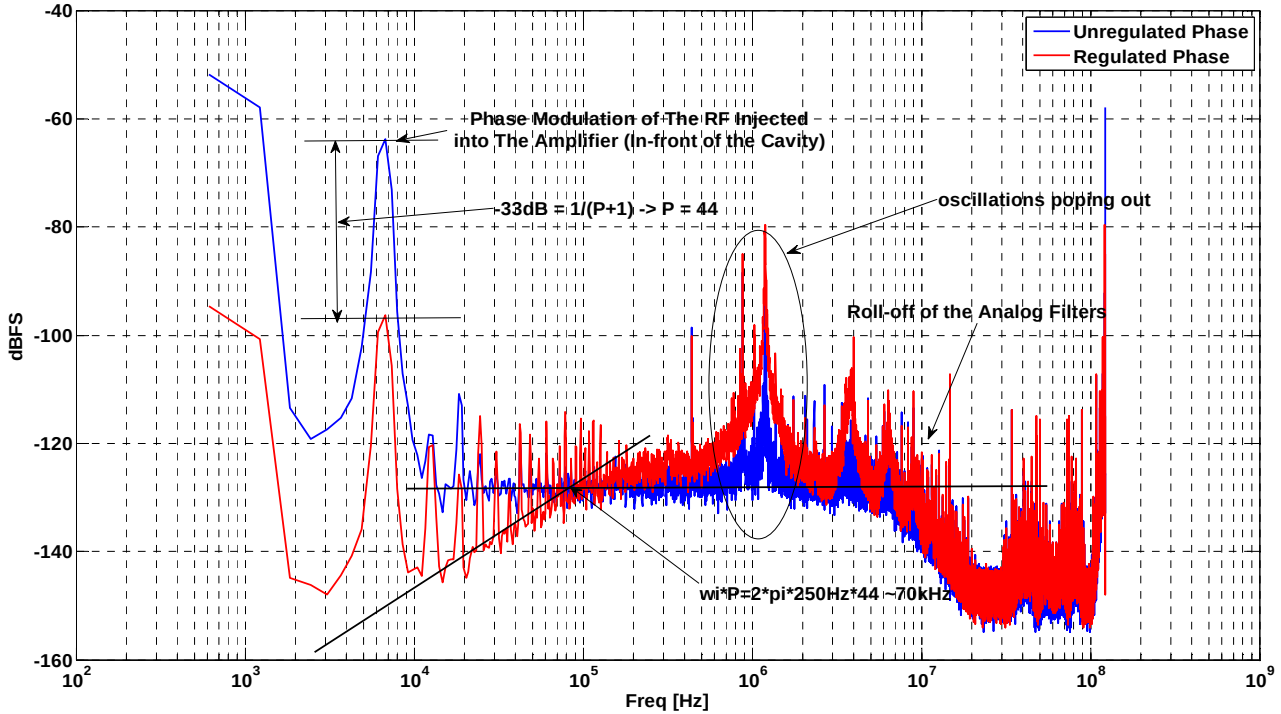
# Power amplifier phase loop 2/2




- **Phase modulation injected at the amplifier output**
- **Modulation frequency is 7 kHz**
- **Achieved attenuation in closed loop is -33 dB.**

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# Conclusions

- **Specific product offering approach.**
- **The product has the key characteristics of a modern and high performance LLRF system.**
- **The installed Libera LLRF systems are used in applications that are quite different.**
- **Recent development includes:**
  - **Investigation of hardware topology enhancement**
  - **Implementation of a second simultaneous feed-back loop using an input on the transmitter module.**