A launch customer's experience of the early days of Libera Electron: From a concept to an operating system

Guenther Rehm

Libera Workshop 2013

March 03:Common Diagnostics between Soleil and Diamond?

SOLEIL SYNCHROTRON

COMPTE RENDU

Summary of the Diagnostic meeting of March 20, 2003 between DIAMOND and SOLEIL

Auteur : J.C. DENARD

STORAGE RING		
diagnostics	quant	collaboration
BPM	120	no

- Control system and local bus standard: SOLEIL uses Tango control system with Compact PCI chassis. DIAMOND uses EPICS control system with VME chassis. There is no possible common equipment at that level.

diamond

May 03: First Glimpse at what will become Libera Electron

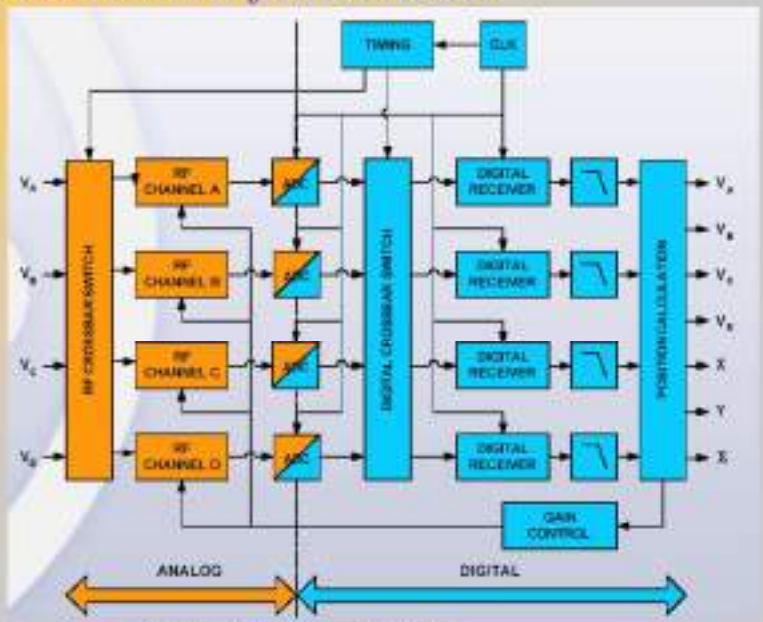
SOLEIL BPM Electronics

- Basic Principles: one type of monitor and one type of electronics
  - Keeps system simple
  - Reduces engineering and installation efforts
  - Eases maintenance
- New SOLEIL electronics developped by I-Tech
  - Multiplexing the 4-channels brings the best of both worlds
  - 0.2 µm resolution; submicron stability with current, bunch pattern, temperature →← fits Slow and Fast feedback systems
  - All BPMs are equipped with 1st turn and machine study capabilities
  - Beam loss history to all BPMs
  - Adjustable threshold interlock output on all BPMs

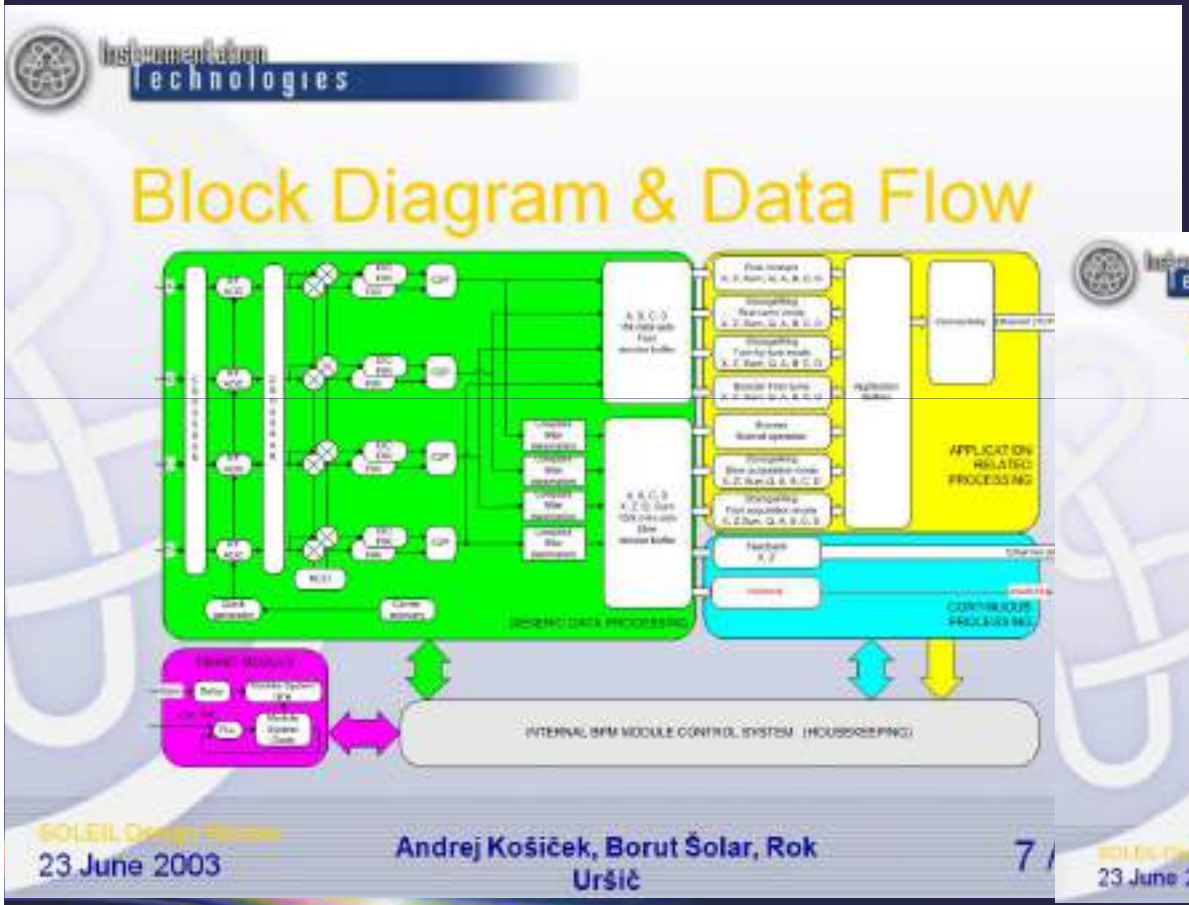
New I-Tech Electronics for SOLEIL

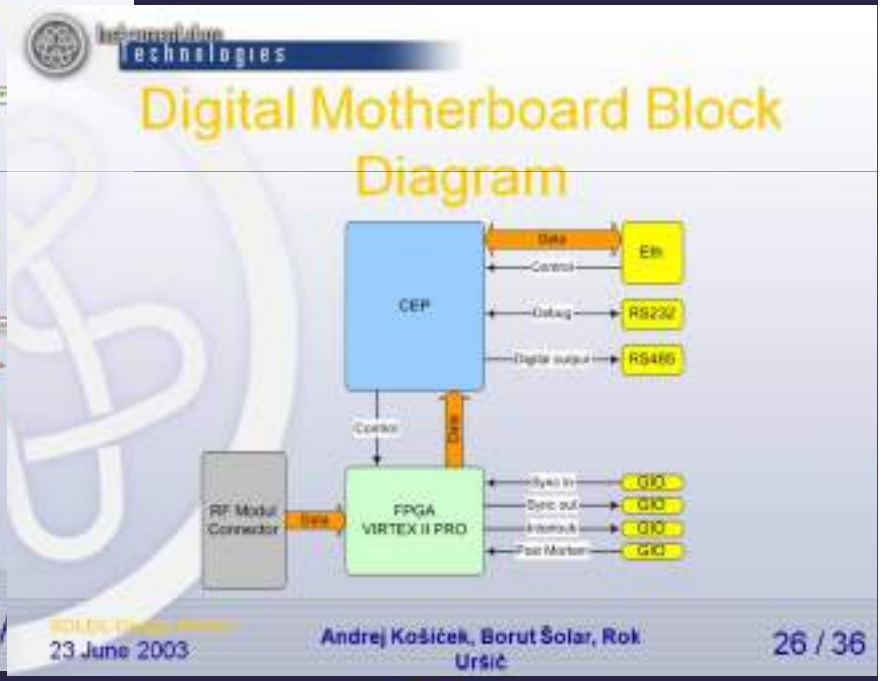
Has advantages of both worlds:

multiplexed and 4-channel systems



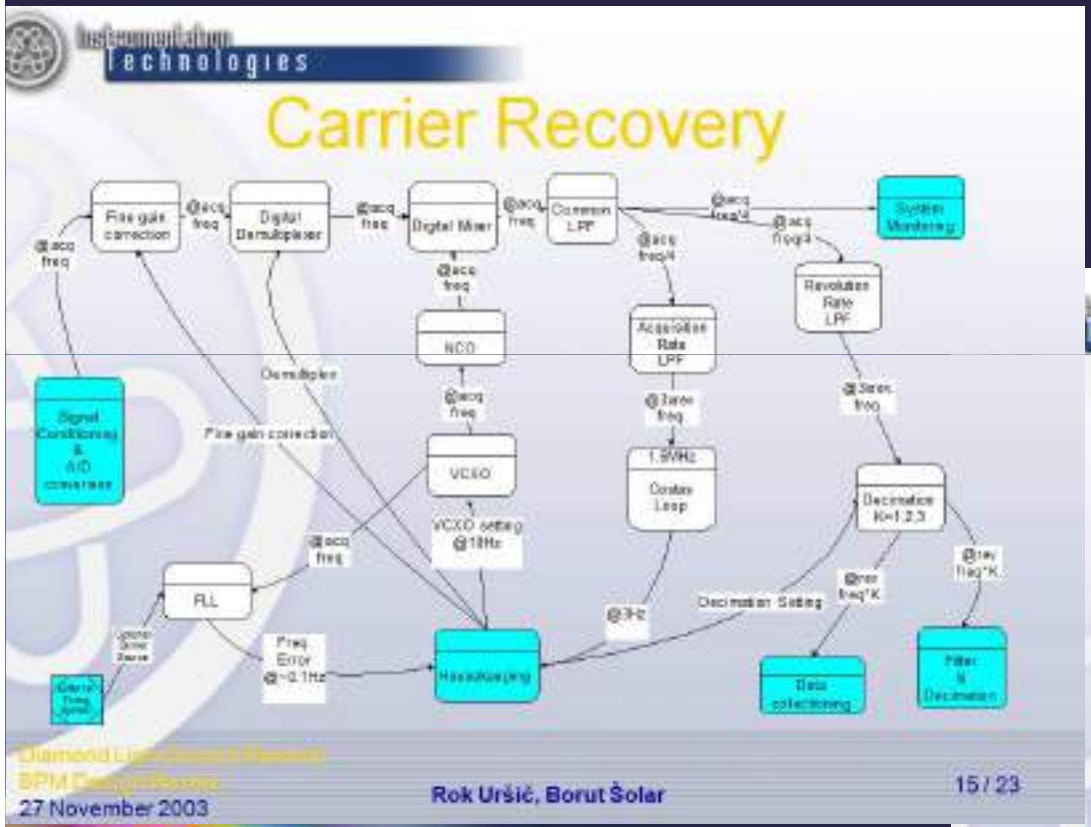
June 03: Design Review at Soleil provides unique Insight

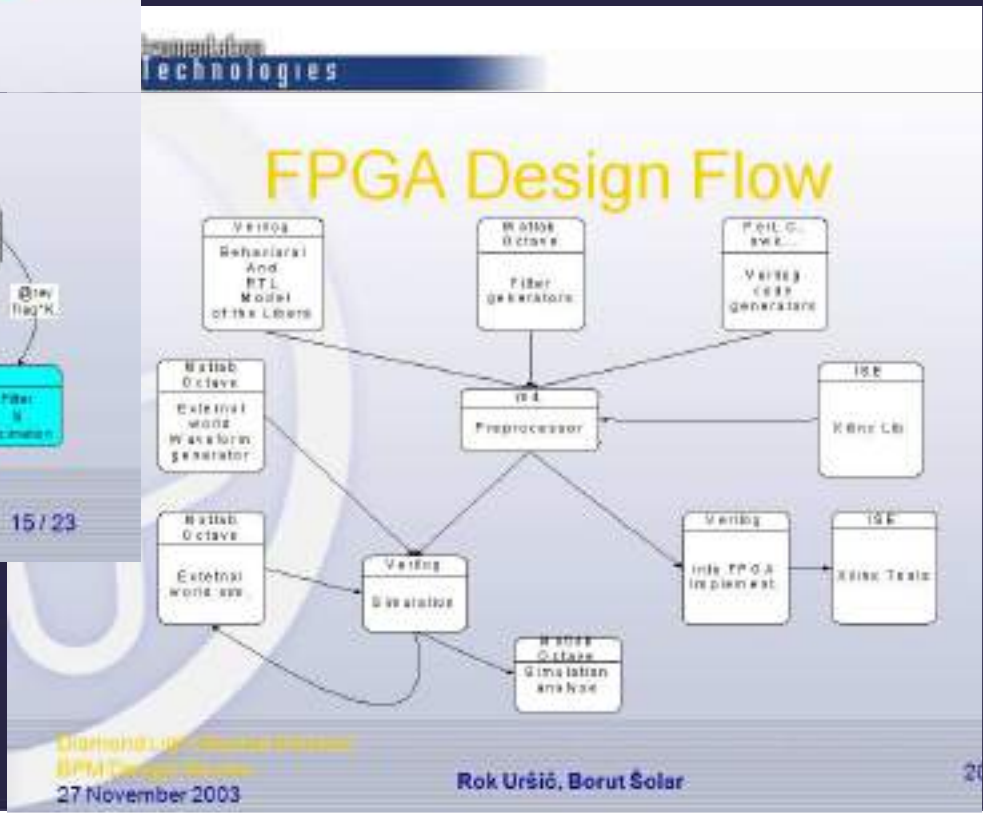




diamond

Nov 03: Design Review at Diamond: More Block Diagrams

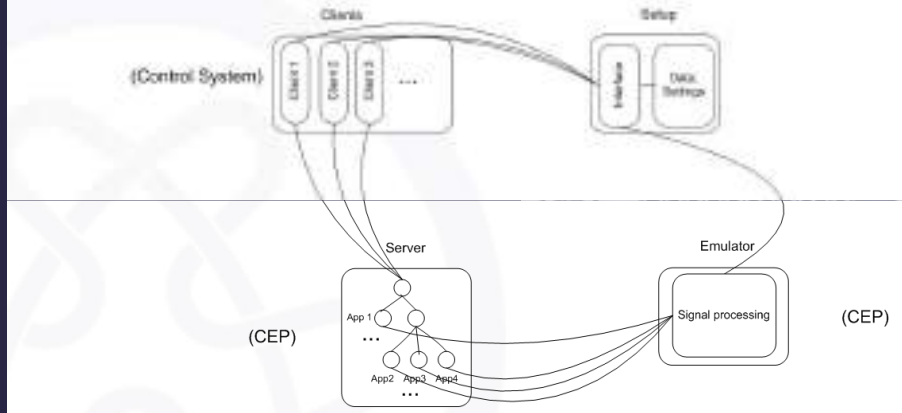




Jan 04: First DLS Visit to IT: Hardware fine. Any Software ?

Control system interface

- SOLEIL case



Timing and Synchronization

#	Name	Type	Connector	Description
1	**Time Reference** (CK)	input	Differential LEMO	**Time reference (PECL)** Synchronizes Libera with the accelerator timing system. Suggested frequency is 10 MHz. The Libera on-board clock (125MHz) is frequency locked to this signal. The setting of absolute time is done with Trigger.
2	**TBT Reference** (TT)	input	Differential LEMO	**Turn-by-turn reference (PECL)** Synchronizes Libera with the accelerator revolution frequency. The Libera sampling clock on the analog board is frequency locked to this signal. Variable on-board delay enables time resolved measurements. In case of failure or absence of this signal, a carrier recovery loop is used to lock the sampling frequency of the Libera analog board to the RF input signal.
3	**Trigger** (FT &IT)	input	Differential LEMO	**Trigger (PECL)** It is an universal trigger that synchronizes Libera with asynchronous external events, such as injection. Its functionality is programmable. It can also used for absolute time synchronization. In order to implement this functionality, a broadcast message containing absolute time reference is sent to all Libera modules over a network in advance.
4	**Post Mortem** (PM)	input	Differential LEMO	**Post mortem (PECL)** When this signal is set, digital signal processing stops. Buffered measurements are then available for "post mortem" analysis.

Feb 04: Original Libera EBPP Tech Specs: Generic on Software

Instrumentation Technologies

Libera

Electron Beam Position Processor
Technical Specification

Original Issue

February 2004

6. Software

The software part of the Libera EBPP is divided into three main groups:

- System software
- Application software
- Tryout software

The software code is executed in two places. One part of the low level application dependable software is running on the PowerPC 405 core, inside the FPGA. This is very dedicated software, tightly integrated into the FPGA. It improves flexibility of the Libera EBPP. The other application related software is implemented in the Linux kernel on the CEP, where it is mainly performing the connectivity to the control system. System software is completely placed in the Linux environment and it is tailored to the accelerator control software for better system integration. The rest of the system software, including the high-level integration software and time synchronization will be prepared according to the user requirements.

6.1. System Software

6.1.1. Maintenance and Start-up Software

6.1.1.1. Bootstrap Loaders

They are responsible for initiating the hardware from completely fresh state by loading the most primitive loaders. This software package depends is hardware dependent and should be changed only at the coarse hardware changes. Procedure for loading this part of the software is automated by using special download JTAG hardware, rs232 serial port connection, and PC with supplemental software.

6.1.1.2. Loaders

They load design image of the reconfigurable FPGA logic and system description files. The utility software for loading a new software revision is part of the EBPP tools package. The new version is loaded at the fully functional Libera EBPP and Operating System and could be integrated in the main control software as RPC. The new version of the hardware and firmware is active after the next booting process. This procedure allows remote firmware upgrades.

6.1.2. Networking Software

It provides main system functionality and the most direct software integration into the accelerator control system. It comprise mostly of standard network utilities and daemons, including: FTPclient, TELNETServer, TELNETclient, NFSclient, NFSserver, RSHserver, FTPserver, Timed.

6.1.3. Diagnostic Software

It provides diagnostics about power supply, cooling fans, electronics status, Libera EBPP and air temperature, booting log files, log files for maintenance and installation procedures, parameter changes and all auto calibration and local time adjusting traces.

6.2. Application Software

Application software is mainly used for additional data processing and for connectivity with the accelerator control system. The first part is running on the FPGA internal PPC. Data processing is split between FPGA and PPC to optimise speed and resources.

The rest of application related software is implemented in the Linux kernel, running on the CEP, where it is mainly performing the connectivity to the accelerator control system.

Application software comprises also all the software necessary to implement Applications functionality as described in paragraph 4 of this document.

6.3. Tryout Software

The tryout software provides an environment that allows an hour start-up time for beginners. With the graphical user interface it enables the user to fully control the Libera EBPP. It is running in the networked MS Windows or PC Linux environment. The tryout software foresees Fast Ethernet connection. It also allows exercising the most generic functionality in the emulated environment.

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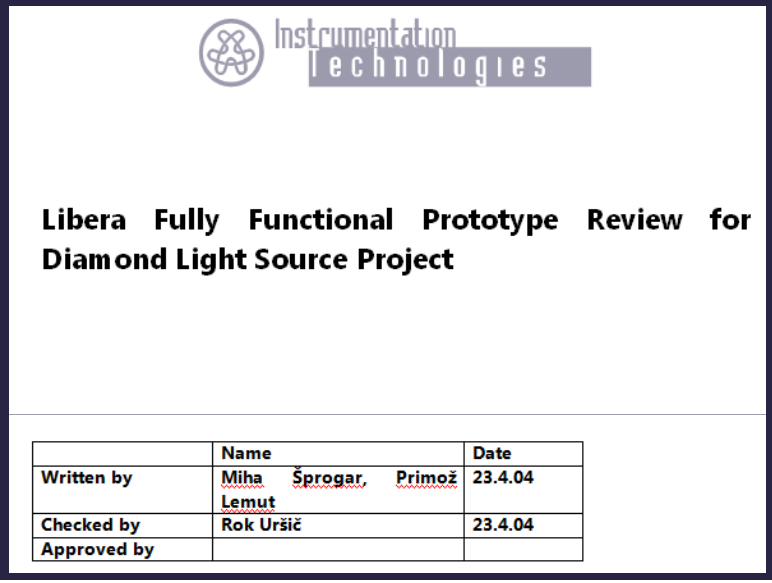
Apr 04: Demonstration of ‘Fully Functional’ Prototype to DLS



Instrumentation Technologies

Libera Fully Functional Prototype Review for Diamond Light Source Project

	Name	Date
Written by	Miha Šprogar, Primož Lemut	23.4.04
Checked by	Rok Uršič	23.4.04
Approved by		

2.4 Beam current dependence

Beam current dependence was measured using Libera hardware for data acquisition and transfer to a PC. Data processing was performed in Matlab environment using FFT method with one neighboring peak on each side of highest peak.

In all measurements 499.654MHz sinus wave signal was used and was 66% gated with 533.818376 kHz rectangular signal. Both signals were using common 10MHz reference to be in phase.

Single sequence sampling (8K samples) was used for first group of measurements and results were within limits only in the middle range.

3.1 DDC within FPGA

Final DDC model was presented and discussed. Presentation of current test implementation of DDC in FPGA served as a proof of principle. Difference between current and final implementation of DDC is in use of module custom development instead of ready-made third party modules. The reasons for custom development are optimization of filters to process signals from accelerators and limited resources within the FPGA.

- Hardware is there, nearly final version (production run imminent!)
- FPGA code ‘bare minimum’ for ADC sample capture, no DDC, **no switching**
- No Driver FPGA to Linux
- No CSPI or EPICS

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Apr 04: First Concepts of a Software Stack emerge

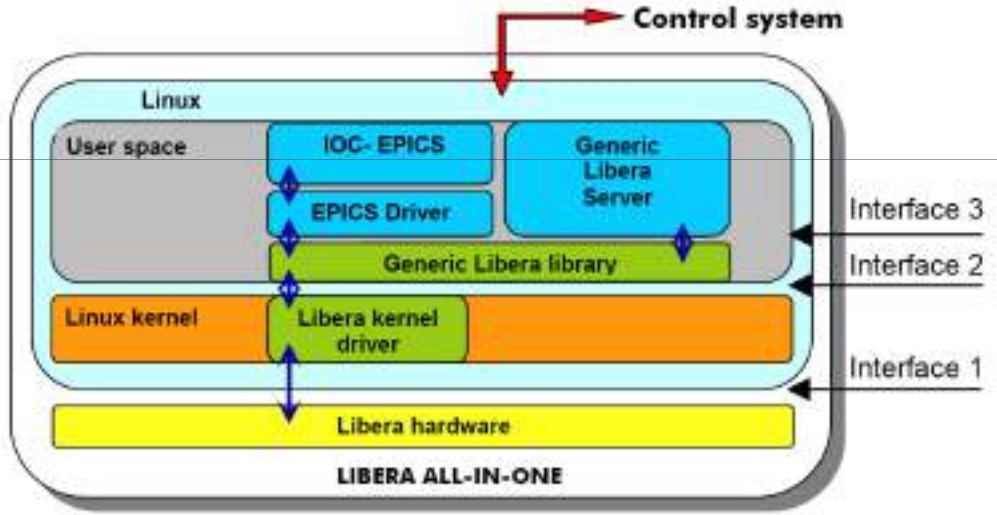
Instrumentation Technologies

Diamond Light Source Electron Beam Position Monitor

Status Report April 2004

	Name	Date
Written by	Rok Ušlič & Primož Lemut	11.05.2004
Checked by	Rok Ušlič	11.05.2004
Approved by		

As for EPICS itself, it has been agreed with Mr. G. Rehm during the acceptance test, that EPICS should be interfaced to the Libera hardware through an API, based on a user space "Generic Libera Library". Compared to the picture below, that would be at the level of "Interface 3". Control System Interface requirements have been further detailed and complemented.



Interfaces 2 and 1 were rejected as they are too hardware dependant and an intimate knowledge of Libera hardware is required to use it in an efficient way. On the other hand the interface 3 offers:

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June 04: Software Stack evolves during Soleil CS review

Libera Control System Software (CSS)

Design and Implementation Recommendations

Author: A.Košiček, M.Šprogar, T.Karčnik
N.Leclercq
Creation Date: 19-Apr-2004

Libera Control System Programming Interface (CSPI)

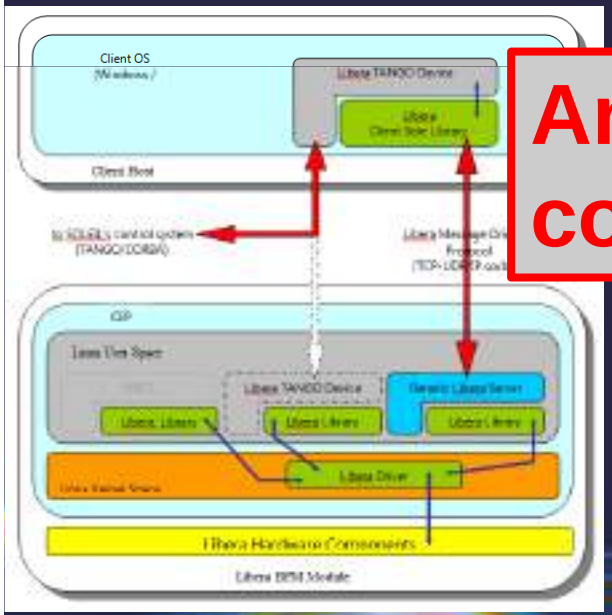
Prototype

Author: M. Šprogar, T. Karčnik
Creation Date: 27-May-2004
Last Updated:

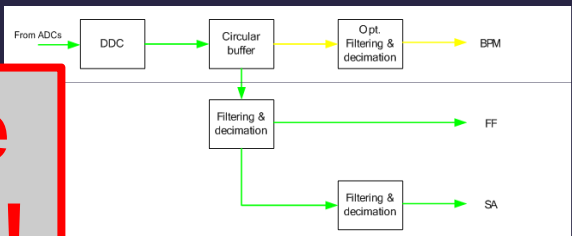
Digital Board Programming Interface (DBPI)

Interface between the FPGA and the XCEP Single Board Computer

Author: M. Šprogar, T.Karčnik, B.Šolar
Creation Date: 10-Jun-2004



Anticipates software complete by Sept 04!



The BPM, FF and SA ends of the signal processing chain. Green and yellow arrows represent data flow and data on demand, respectively.

DIGITAL BOARD GNU/LINUX ON XCEP

Figure 5: Continuous acquisition of sequential data. FIFOs are employed internally in the Libera GNU/Linux driver to dispatch data to CSPI applications and compensate for fluctuations in speed at which data is read and processed in the CSPI layer. During the connection phase, L_connect sets registers with the Libera driver and allows it to setup a FIFO buffer. To an application, the mechanism to dispatch data is completely transparent.

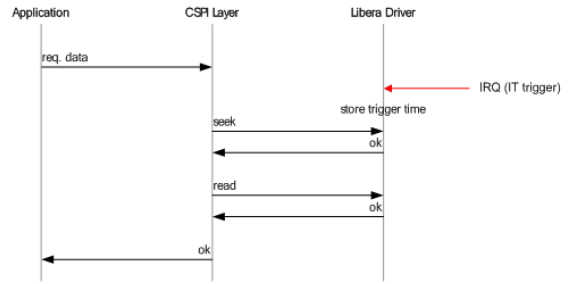
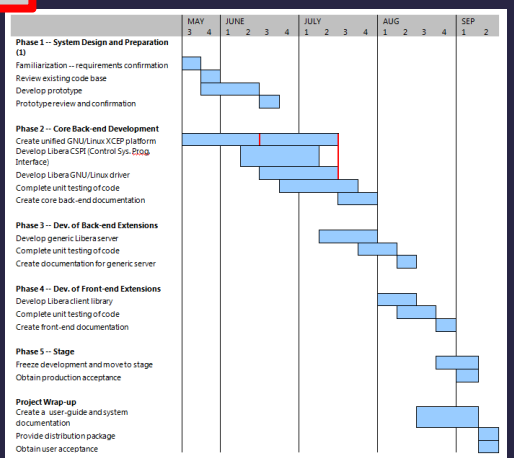


Figure 6: Time diagram for data-on-demand request. By default, seek sets the current access point to the time of last trigger.



Instrumentation Technologies is prepared to commence work on this project upon approval from SOLEIL. Given a start date of June 7, 2004, our estimated completion date for this project is middle of September, 2004.

Aug 04: DLS contract SCS with Design of FOFB

- Super Computing Systems signs NDA with IT to agree interfaces inside FPGA
- Scope of supply by SCS (beyond original EBPM specs) is agreed
- The result of this work later becomes the ‘Diamond Communication Controller’, which now runs at Diamond, Soleil, ESRF, ALBA and Delta

Sept 04: Software/Firmware delayed, new schedule

Delivery Milestones DIAMOND	1st	2nd	3rd	4th
Date	10.12.2004	10.2.2005	10.4.2005	10.6.2005
TBT data (@rev freq) Booster & SR	x	x	x	x
SA data (@10Hz)	x	x	x	x
MC, SC sync	x	x	x	x
Injection Trigger	x	x	x	x
GC, AGC 1st phase	x	x	x	x
Switching scheme fast (100Hz) for SA	x	x	x	x
FFAI to FPGA interface		x	x	x
Time Set SC		x	x	x
Triggering Full		x	x	x
I2C diagnostics		x	x	x
Switching scheme advanced slow			x	x
Linearization			x	x
Crosstalk compensation			x	x
AGC 2nd phase			x	x
Post filtering (Booster Normal)			x	x
Carrier recovery loop				x
Fast Feedback accessories				x
Advanced auto data checking				x

Anticipates software complete by June 05!

diamond

Jan 05: First Liberas received, software/firmware rudimentary

- Only Turn-by-Turn data is available, limited to 130008 samples
- Conversion from ABCD-IQ to XY is in software using emulated floating point (slow!)
- Input switches only under manual software control, no fast switch rotation, filtering etc.

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Feb 05: Software delivery schedule slips further

Delivery Milestones (RELEASE)	1st	2nd	3rd	4th	5th
Date	10/2/2005	7/4/2005	19/5/2005	14/7/2005	15/9/2005
TBT data (@rev freq) Booster & SR	+	+	+	+	+
MC, SC sync	+	+	+	+	+
Injection Trigger	+	+	+	+	+
Manual GC	+	+	+	+	+
Acquisition over driver and CSPI	+	+	+	+	+
SA data (@10Hz) with switching scheme		-	-	-	-
Post filtering for Booster		-	-	-	-
Specified Fast Feedback interface		-	-	-	-
AGC 1st phase			-	-	-
Implemented Fast Feedback interface			-	-	-
Triggering Full			-	-	-
I2C diagnostics			-	-	-
AGC 2nd phase: uninterupted Fast Feedback data stream				-	-
Signal conditioning				-	-
Carrier recovery loop*					-
Fast Feedback accessories*					-
Advanced auto data checking*					-

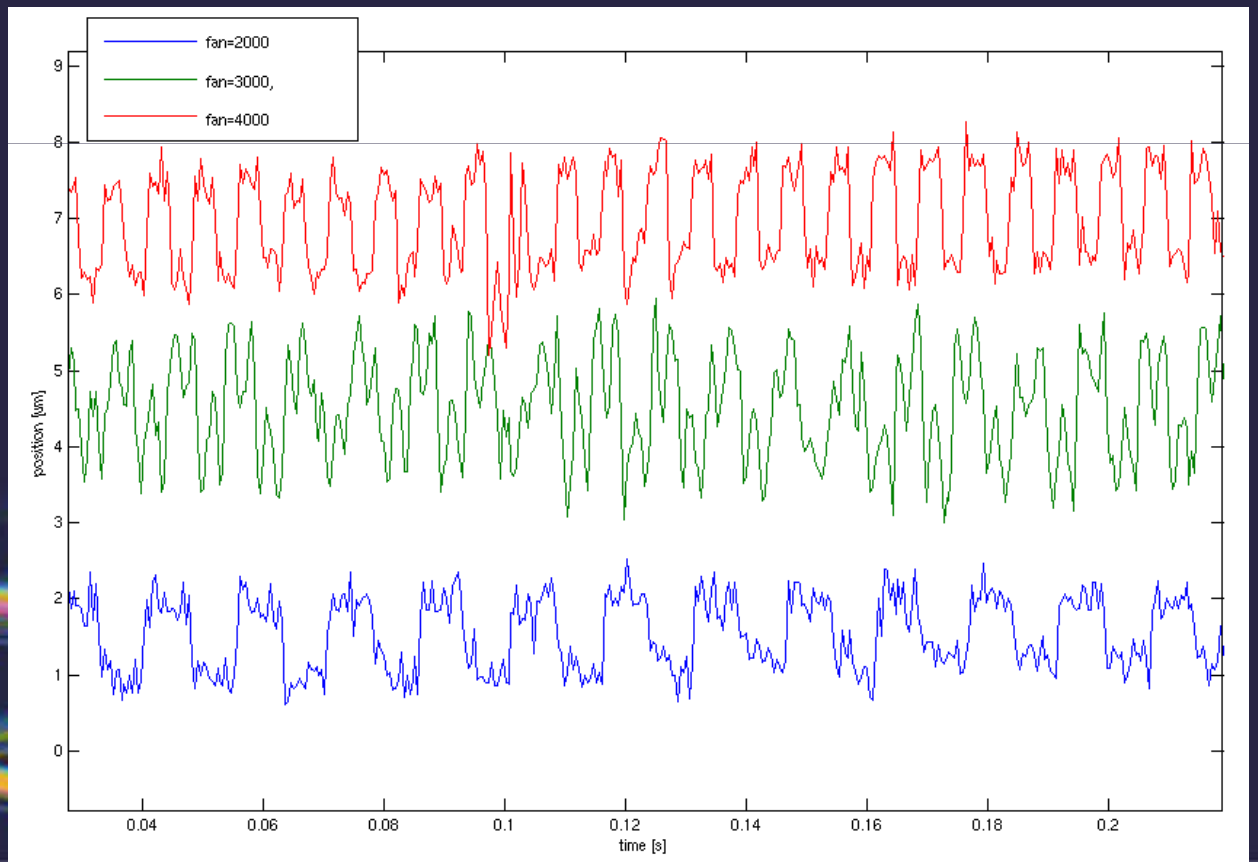
Outside scope of contract

Anticipates software complete by Mid July 05!

diamond

Feb 05: Testing at DLS shows up two Problems (1)

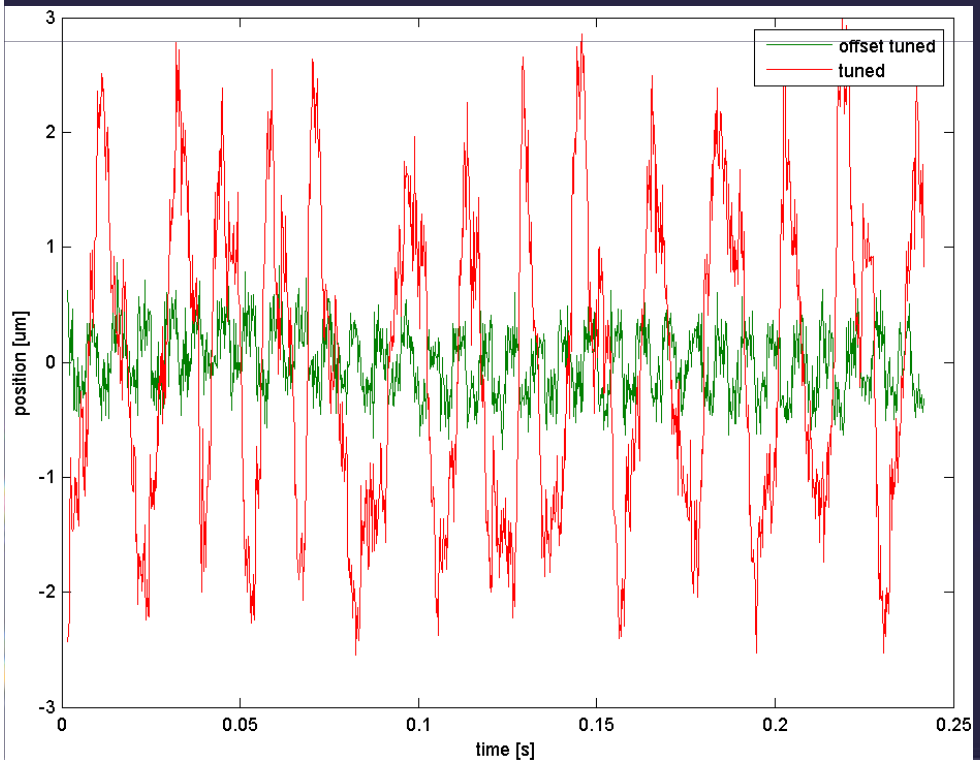
- Fan rotation signal appears in position signal
- Removed by adding filtering on tacho signal

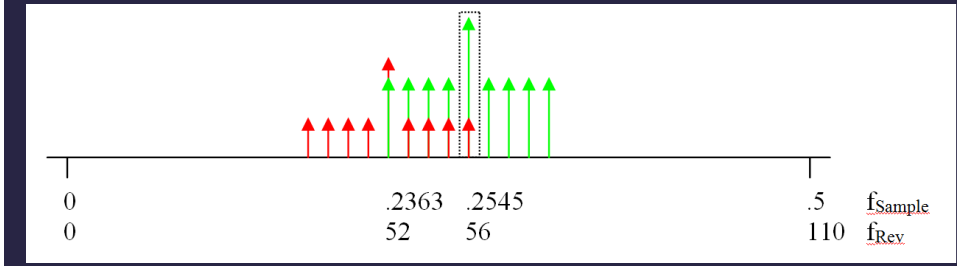


diamond

Feb 05: Testing at DLS shows up two Problems (2)

- ADC sample rate at precise multiple of revolution frequency creates noise
- Addressed by offset tuning of VCXO





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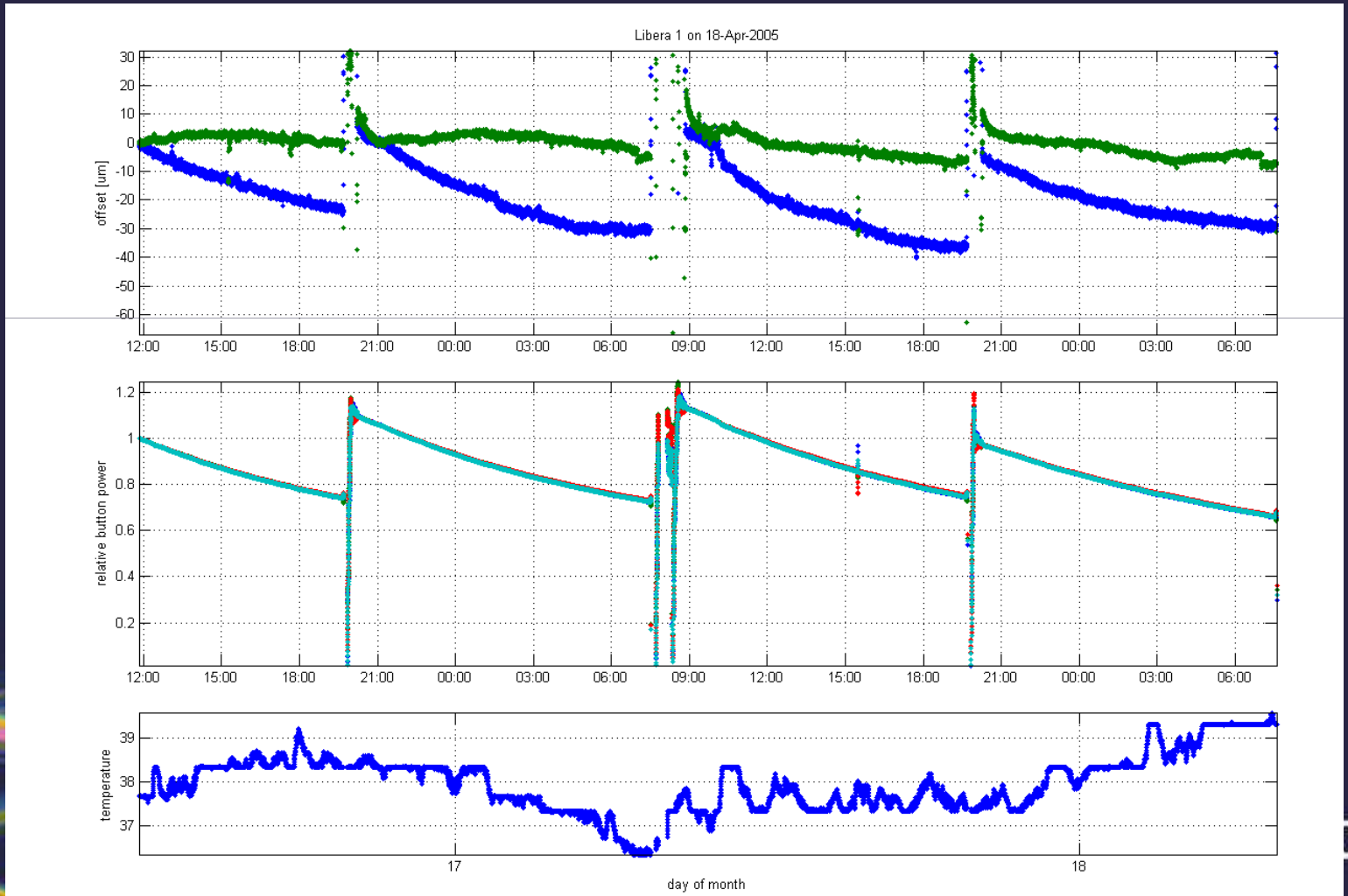
Apr 05: First results from ‘real beam’ at SRS Daresbury



May 05: Signal Conditioning Design Specs evolve

Libera Signal Conditioning Subsystem

Design Specifications

	Name	Date
Authors	Borut, Uros, Ben	10-April-2005
Editor	Ben Rolfe	
Approved by		

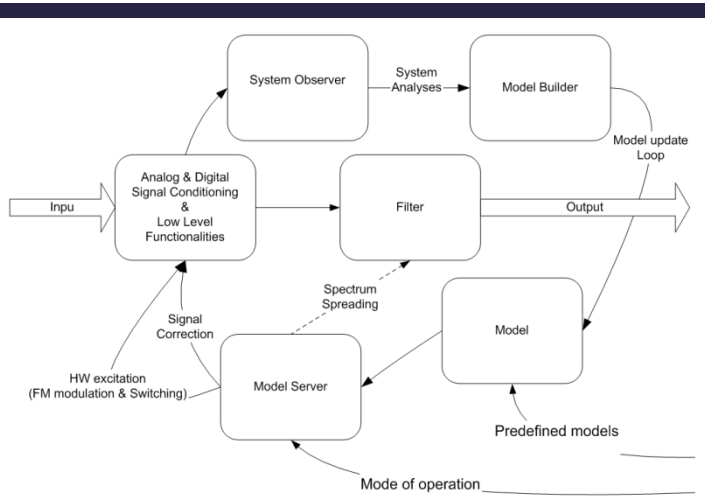


Figure 1: Signal Conditioning Architecture

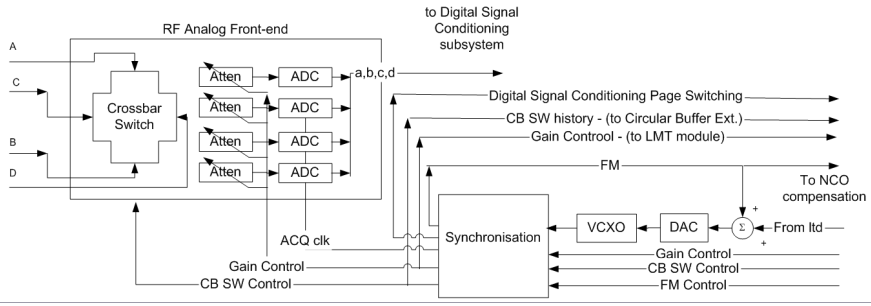


Figure 3: Analog Gain, FM and Crossbar switching low level functionality

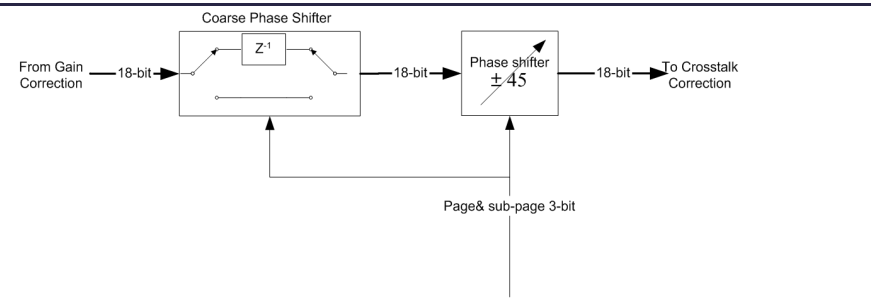


Figure 9: Phase shifter

Phase shifting FIR filter has two coefficients (Coefficient_0 and Coefficient_1) for fine grain phase shift definition and selection for step shifter with one clock delay. The transients are finished in two clocks. The filter has four sets of coefficients for all four CB switch patterns. The additional page of four sets enables active/passive page swapping.

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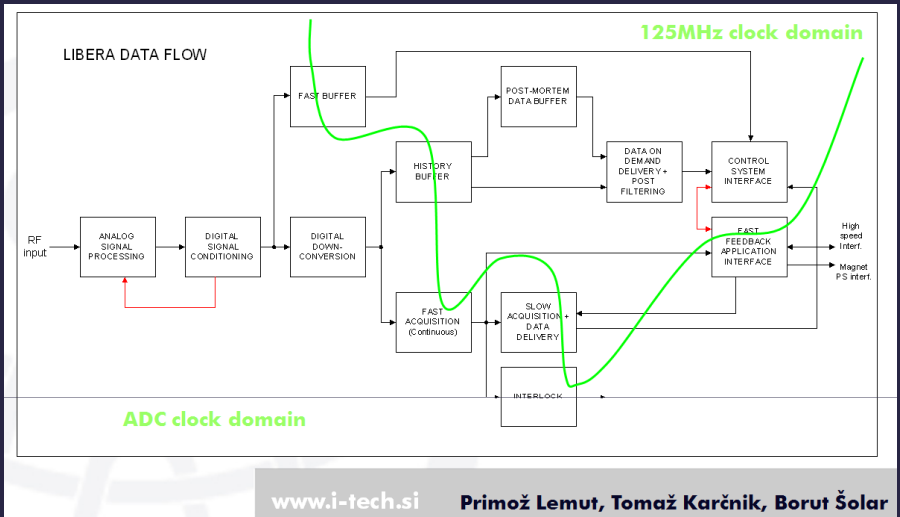
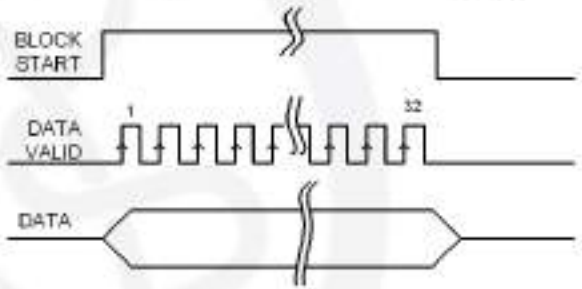
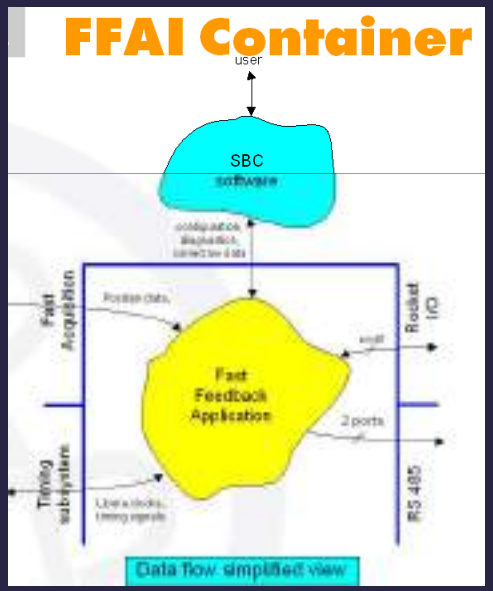
July 05: Fast Feedback Application Interface proposed



- Parallel data clocked out serially
- 32 blocks of 16-bit data transferred
- BLOCK START signal @ FA output rate
- ENABLE signal at max $f_{ADC}/2$ rate





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Oct 05: Slow Progress on Software

- 2nd milestone including SA data and switching still not delivered or in sight
- Instrumentation Technologies decides to ‘Call in the cavalry’ and outsources FPGA design
- New plan sees 1.0 software/firmware (including all important functionality) by Jan 06

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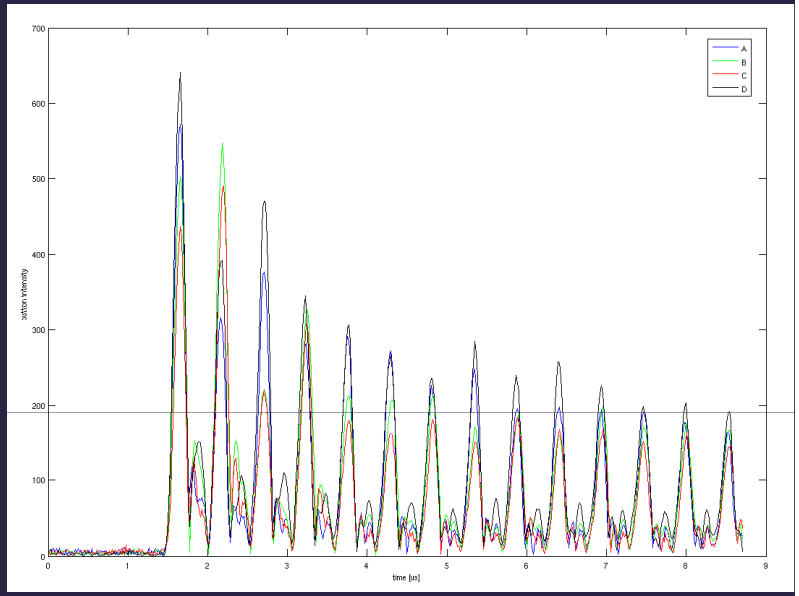
Jan 06: Software release 1.0!

- Adds ADC rate buffer, just in time to see first turns in our booster
- Adds SA data rate, but still no switching in FPGA (postponed to May 06)
- Adds FFAI, so DCC is integrated and first FA data is received



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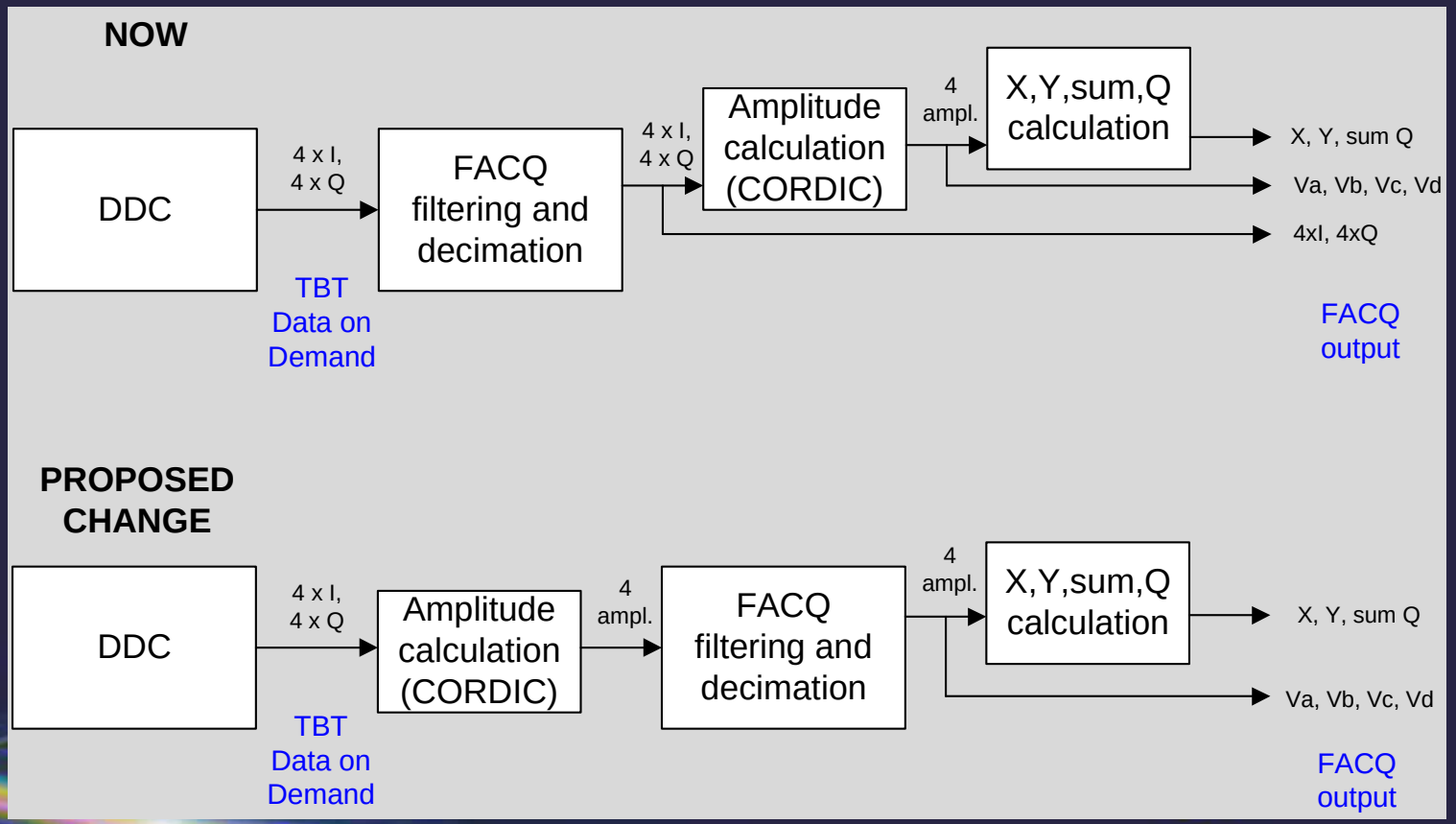
May 06: A Small Change which will later limit a nice functionality



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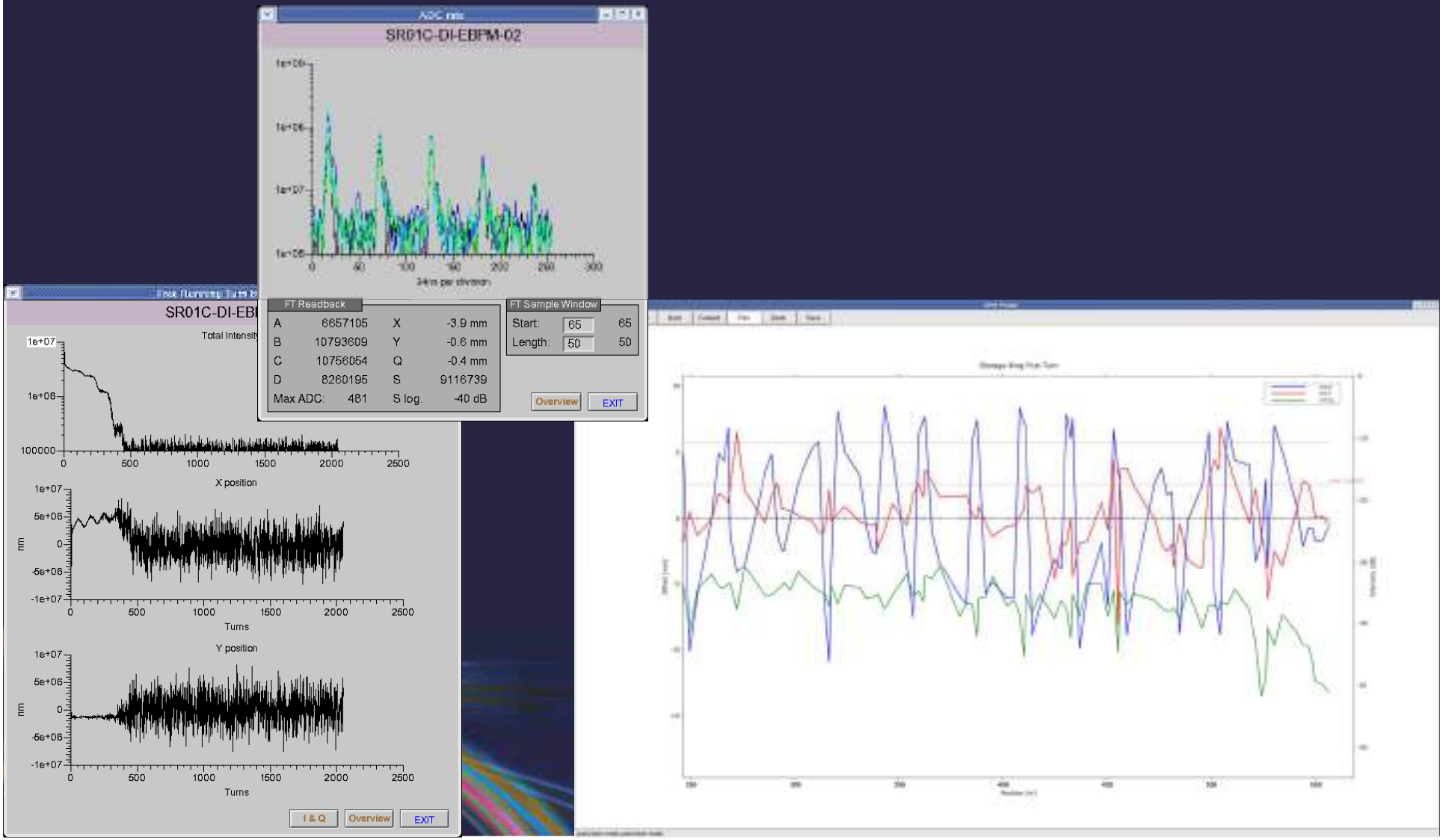
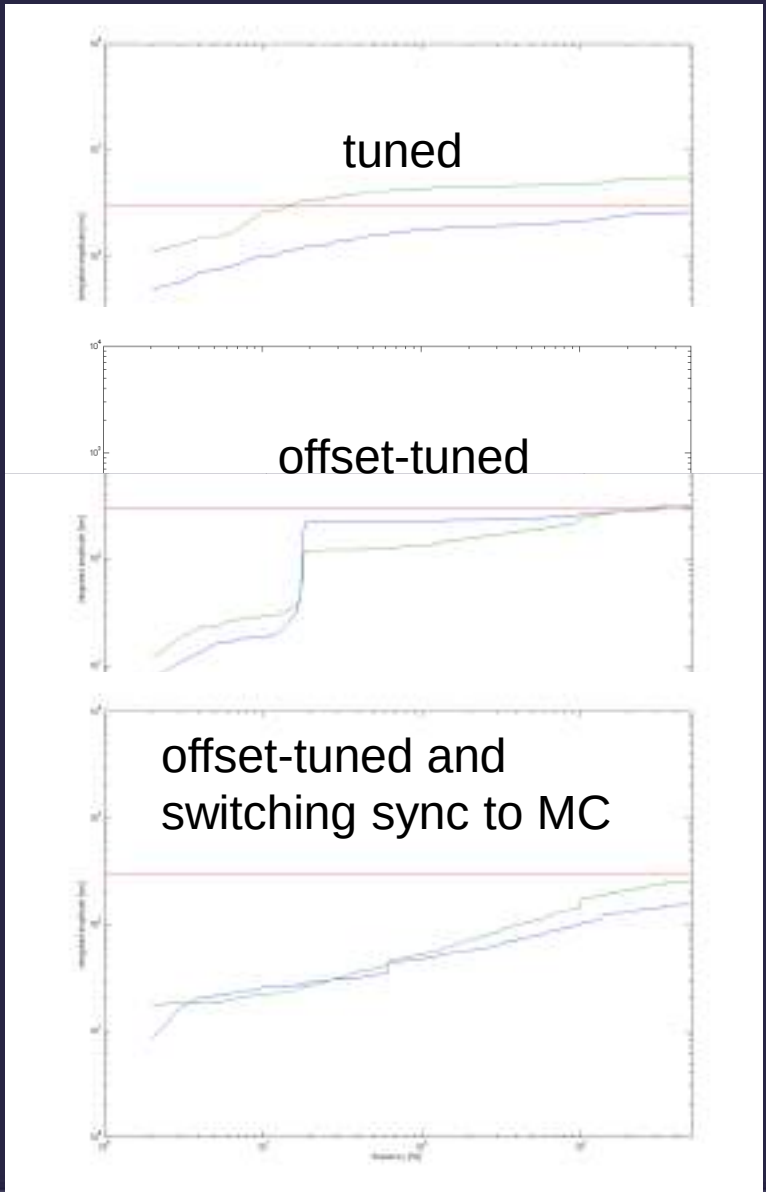
May 06: First turns in Diamond Storage Ring, Liberas help



July 06: Software release 1.2

- Finally, Switching in the FPGA and Digital Signal Conditioning are included!
- This reveals new issue with offset-tuning and switching, mitigated by changing the switch to be in sync with MC
- Orbit Interlock functionality included (needed for Sept 06 storage ring commissioning)
- Manual gain/attenuator control and AGC



Dec 06: Software release 1.4

- DSC contains phase compensation (essential for performance)
- Switching can now be sync'ed to MC when offset-tuning in use
- Interlock no longer dropped when attenuators switch
- Offset-tuning finally in an official release (22 months after showing it is necessary!)

diamond

What happened next?

- Diamond began user operation in Jan 07
- Further software releases as part of support contract
- 1.60 in July 07
  - Linux kernel 2.6 and everything related (fixes long standing Ethernet problems)
  - Introduces ‘proper’ threads and stops using emulated floating point operations
- 1.80 in Dec 07
  - New PLL daemon and health daemon
  - More parameters through CSPI
  - More Interlock diagnostics

And even later...

- Sept 08: IT licenses DCC for packaged distribution to ESRF and ALBA
- Feb 09: Software release 2.0 adds features requested by user community
- Oct 09: DLS helps to track down problems with DCC producing lots of errors at ESRF
- Mar 10: DLS upgrade to completely self built OS: uboot, Linux, rootfs, driver (based on IT), EPICS

Summary: What did we put in?

- Supplied lots of time from 3 people
- Endless testing both in the lab and on beam
- Nearly 1000 emails sent over the years
- Dug deep into hardware / schematics / firmware / software
- Supplied various features/patches
  - Communication Controller, parts of PLLd
  - MAXADC, ADC overflow variation

Email Traffic Statistics

Year	Sent by DLS	Sent by IT
2003	42	36
2004	87	104
2005	225	200
2006	142	181
2007	116	197
2008	96	149
2009	90	200
2010	64	41
2011	43	63
2012	87	90
Total	**992**	**1261**

Summary: What did we get out?

- ‘Access to all areas’: All sources and schematics, allowing us to fix problems ourselves
- Learned a lot about digital signal processing, software development, project management
- Able to influence a number of design decisions

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One Problem remained: Spontaneous Crashes/Reboots

- About one crash observed every 1-2 weeks on a population of 200.
- Most lead to driver or kernel crash and halt
- **A few (about 1 per year) spontaneously reboot, thus dropping the interlock and the beam**
- A problem only at Diamond?

Results of Poll in 2011

Institution	No. Liberas	Crashes seen?	I/locks?	Serial Console?
Diamond	210	32 in 1½ y	174	Logged
ESRF	224	10–20/y	8	No
DESY				No
Taiwan Photon Source				No
SINAP				No
ALBA				No
Soleil	147	2/y	half	No
Australian Synchrotron	98	A couple	limited	No
Elettra	100	None	IDs only	No

Now: 50 crashes in 3 years.
Beam trips: 1 in 2010
0 in 2011
1 in 2012
3 in 2013

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Solution found!

- In the meantime, we had received the sources for the CPLD on the CEP
- We worked through those, and checked timing of interlock loss relative to CPU reset
- It turned out, it was not the CPU reset which caused the FPGA init, but a register write in uboot, which was easily changed
- New uboot and small change to init scripts rolled out in March 13
- On a reboot the FPGA will not be reset, interlock is not dropped, but FOFB will stop and EPICS alert.

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- The audience for listening

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All the best for the next 10 years, the DLS Libera Family