Instrumentation Technologies

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Coping with Coupled Bunch Instabilities, 2/2

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Libera Bunch-by-Bunch Setup

- Libera Bunch-by-Bunch
- Clock source – 352.202 MHz
- Input Signal source – 100 kHz
- Output signal over DAC to oscilloscope

Graphical User Interface – GUI

- Matlab created
- Intuitive
- General Libera Bunch-by-Bunch settings

FIR Filtering

- FIR filtering on all processing chains
- 16-tap FIR filter, frequency response
- Loading of coefficients
- ‘Straight-through’ coefficients

Delay of Output Signal

- Adjustable delay of output signal
- Steps ~ 2ns (2.84 ns)
- In the final implementation stage: delay in steps of 1ns/32 ~ 31ps
- Setting delay through GUI
- Constraints

Phase of Output Signal

- Adjustable phase of output signal at the desired frequency
- Range: $(-\pi, \pi)$
- Setting phase through GUI
- Constraints

FIR Filtering on Single Processing Chain

- Each processing chain has its own set of coefficients
- GUI download of different FIR coefficients for each processing chain

FIR Filtering of a Single Bunch in One Processing Chain

- Deployment of FIR filtering in one processing chain
- One bunch in one processing chain filtered with independent set of coefficients
- GUI download of FIR coefficients for single bunch in one processing chain

FIR Filtering of a Single Bunch in All Processing Chains

- One bunch in all processing chains filtered with independent set of coefficients

- Time domain of signal output. Bunch numbering: 1,2,3,4,5,6,7,8,9,10,... (one color belongs to one processing chain) i.e. A0,B0,C0,D0, A1,B1,C1,D1, A2,B2,...

FIR Filtering of a Single Bunch in All Processing Chains

Absolute bunch number (relative bunch number)				
Chain A	1 (0)	5 (1)	9 (2)	13 (3)
Chain B	2 (0)	6 (1)	10 (2)	14 (3)
Chain C	3 (0)	7 (1)	11 (2)	15 (3)
Chain D	4 (0)	8 (1)	12 (2)	16 (3)

Features in the final development stage

- Application of 3 set of coefficients for transient grow-dump experiments

- Sending bunch samples to DAC from memory. Actual bunch samples from ADC are disregarded. Samples loaded to FPGA memory are sent directly to DAC.