Instrumentation Technologies
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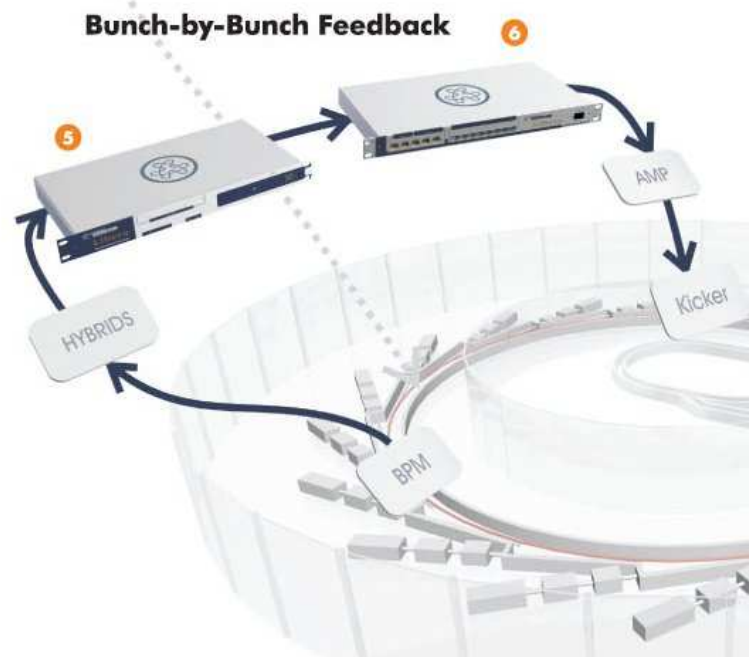
Libera Bunch-by-Bunch Feedback System

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Libera WORKSHOP 2009

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Libera Bunch-by-Bunch

Libera Bunch-by-Bunch is a digital processing unit (6) that is a core part of Bunch-by-Bunch feedback loop. It can be used for bunch cleaning as well.
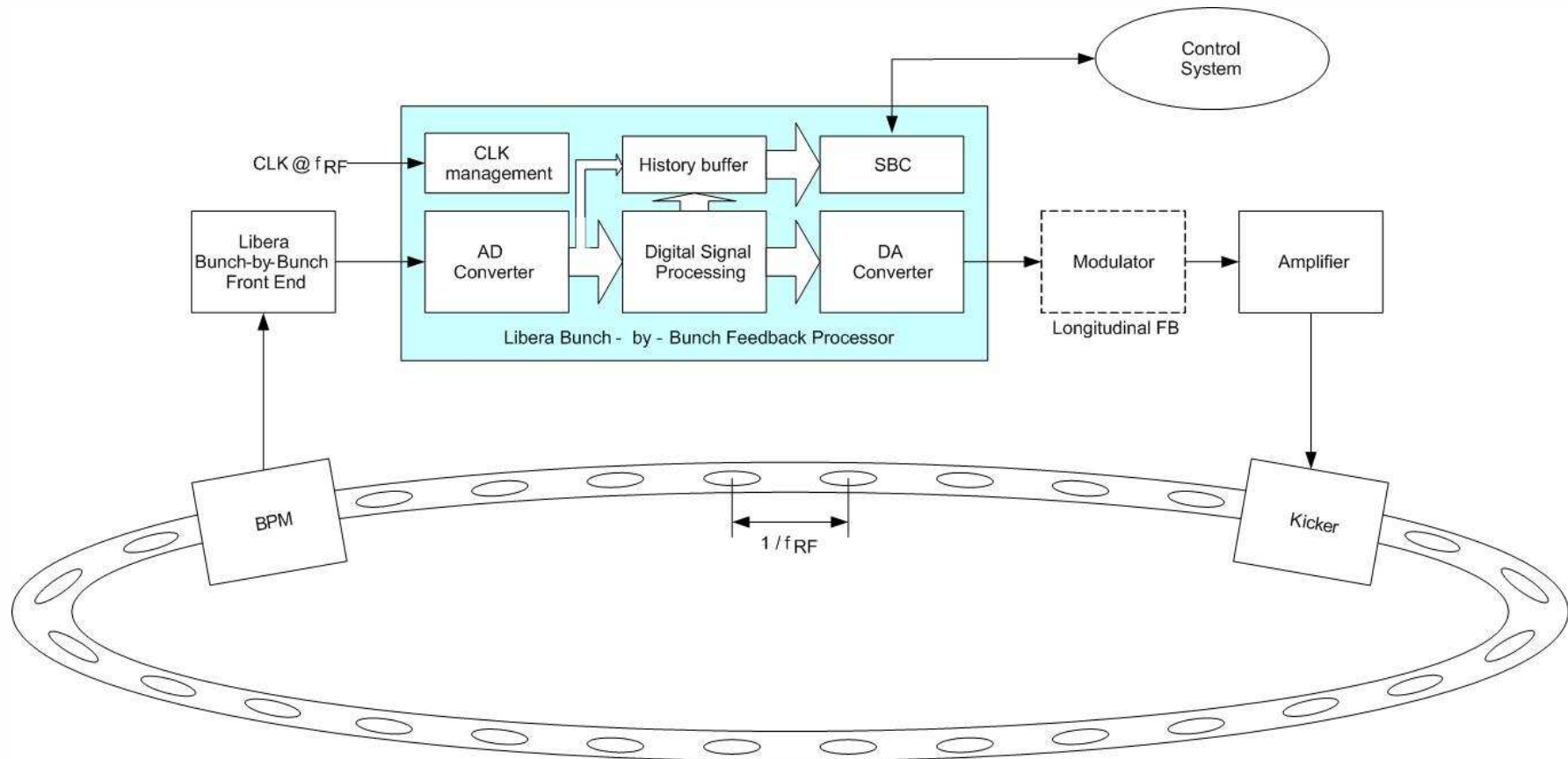
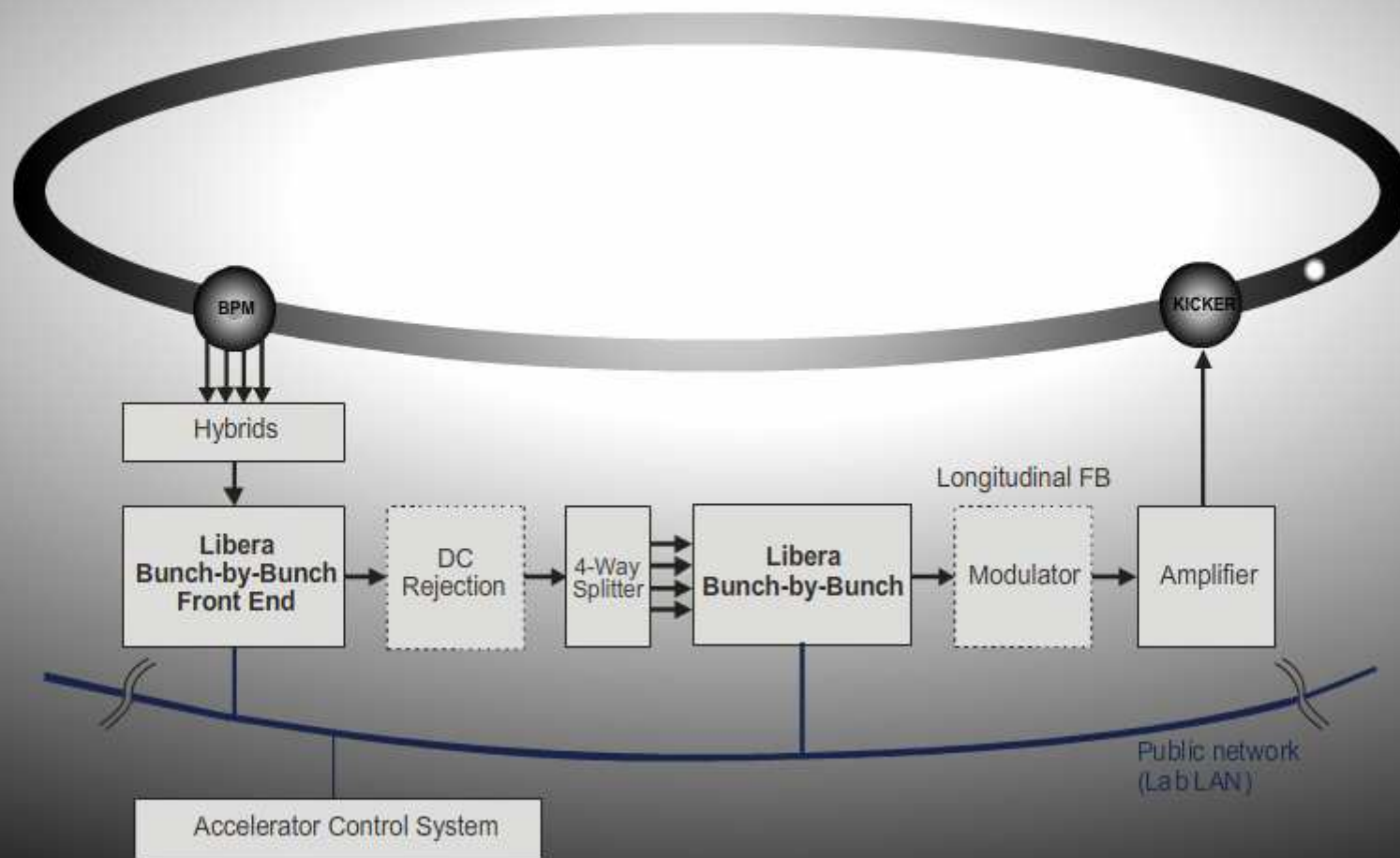

Bunch-by-Bunch Feedback

Libera Bunch-by-Bunch Front End

Libera Bunch-by-Bunch Front End (5) is a multi channel unit that provides amplitude or phase demodulation of the bunch position signals from the hybrids and passes demodulated signals to the processing unit (6).
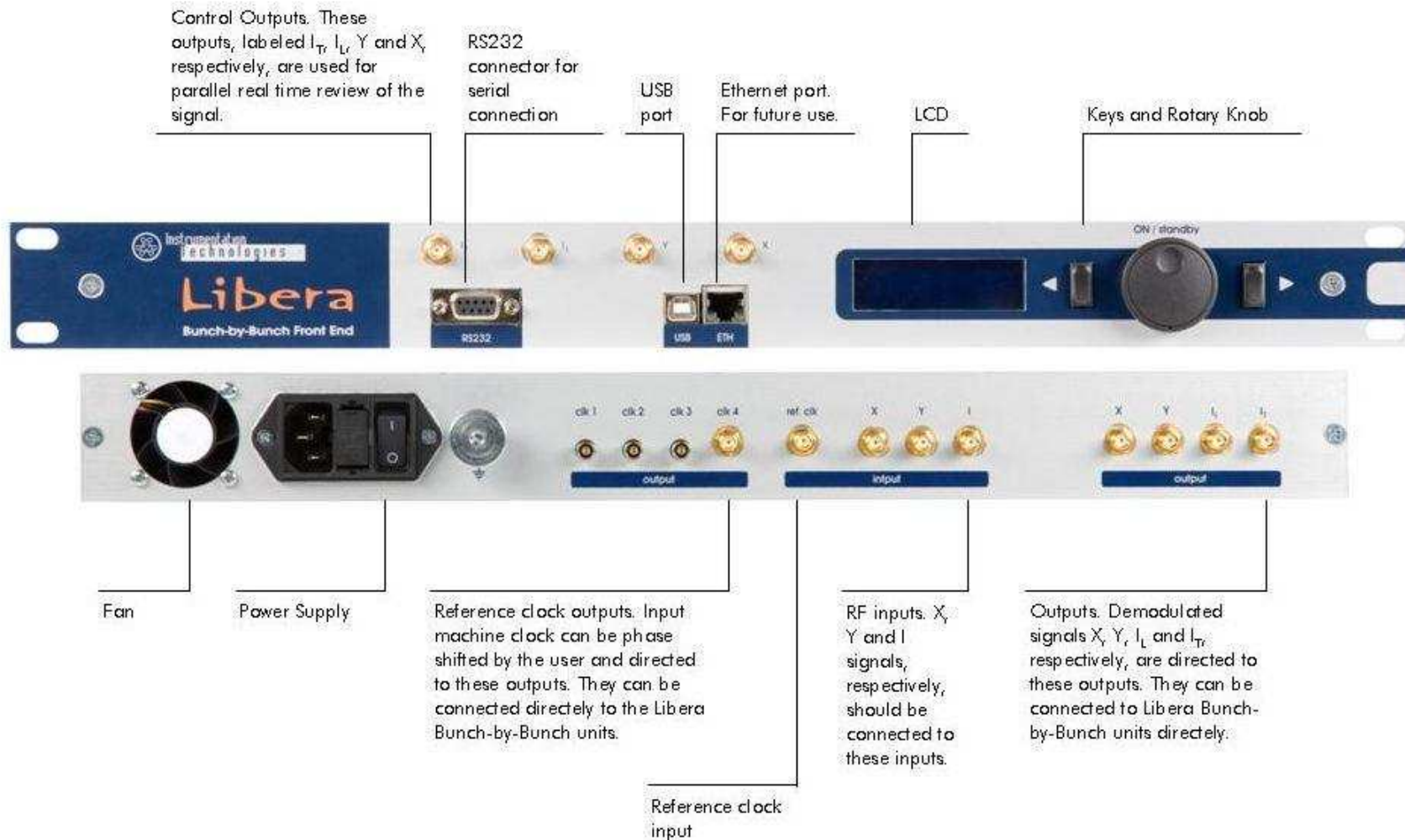
Bunch-by-Bunch Feedback Loop

Bunch-by-Bunch Feedback Loop

- **Hybrids combine BPM pick-ups. The outputs are X, Y, I (sum).**
- **Libera Bunch-by-Bunch Front End converts X, Y, I signals to baseband.**
- **Libera Bunch-by-Bunch (processing unit) digitizes the signal, does the processing and converts the signal back to analog.**
- **The modulator is used only in longitudinal feedback and translates the correction signal to the frequency of the kicker.**
- **The power amplifier supplies the power to the kicker.**

Libera Bunch-by-Bunch Front End

Control Outputs. These outputs, labeled I_T, I_L, Y and X, respectively, are used for parallel real time review of the signal.

RS232 connector for serial connection

USB port

Ethernet port. For future use.

LCD

Keys and Rotary Knob

Fan

Power Supply

Reference clock outputs. Input machine clock can be phase shifted by the user and directed to these outputs. They can be connected directely to the Libera Bunch-by-Bunch units.

RF inputs. X, Y and I signals, respectively, should be connected to these inputs.

Outputs. Demodulated signals X, Y, I_L and I_T, respectively, are directed to these outputs. They can be connected to Libera Bunch-by-Bunch units directely.
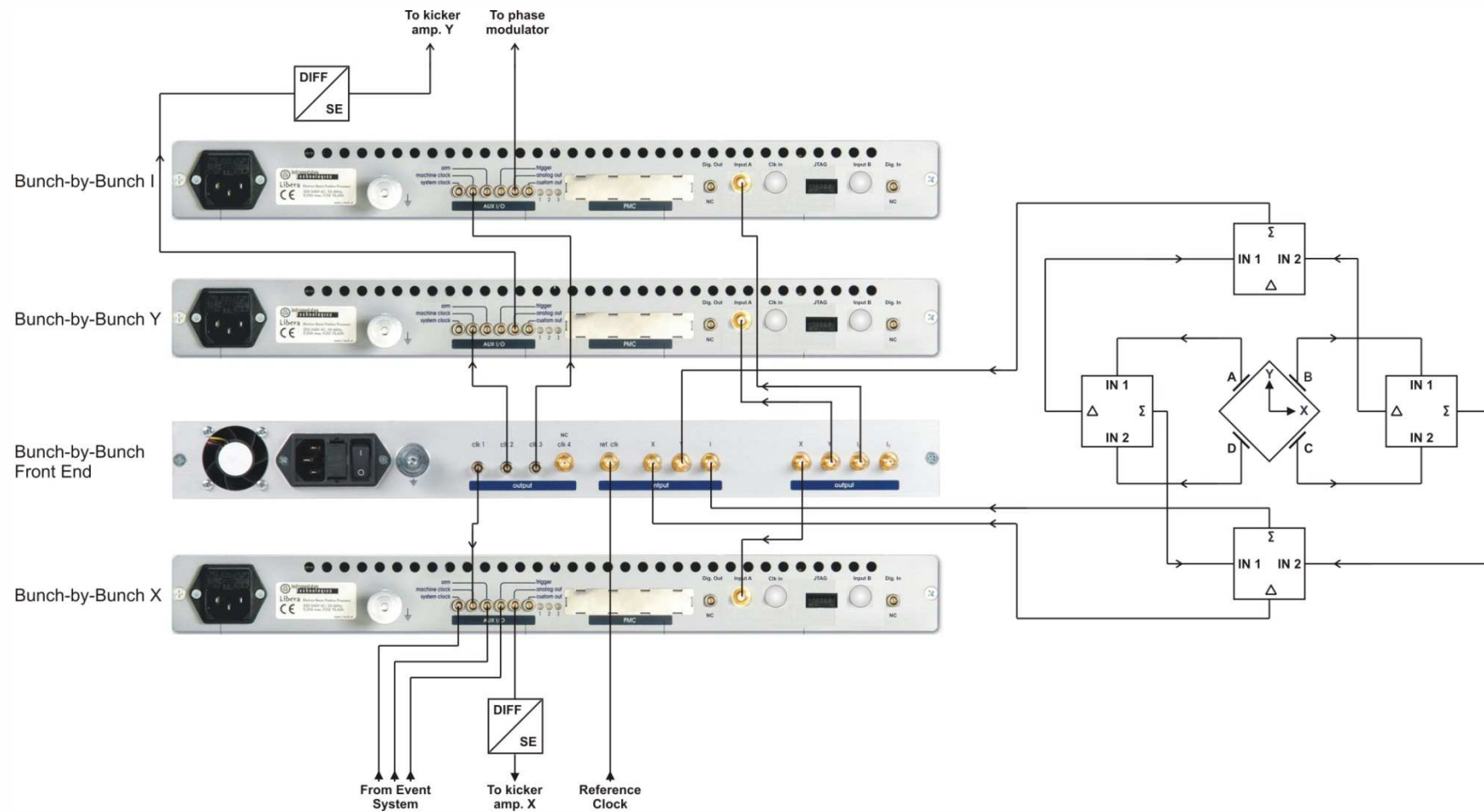
Reference clock input

Libera Bunch-by-Bunch Front End Block Diagram
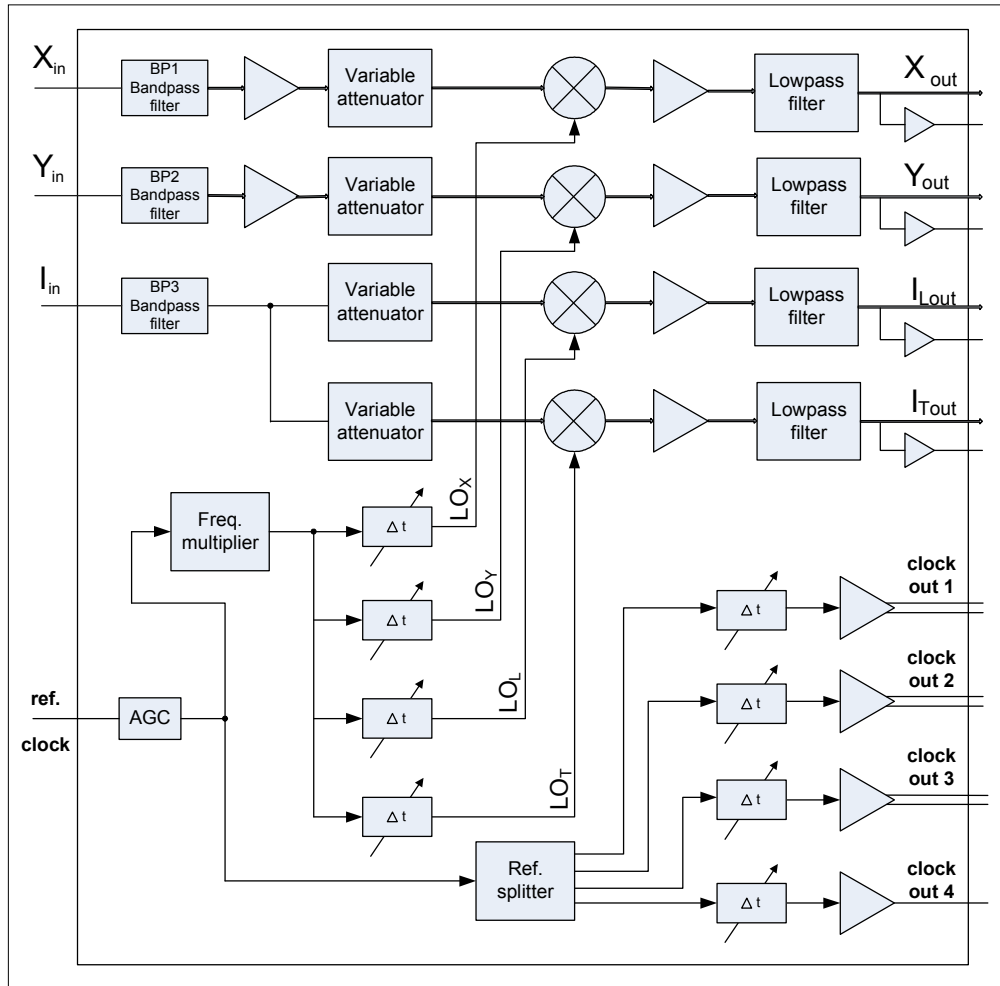
- **Input BandPass filters**
- **RF gain block**
- **Mixers**
- **IF gain**
- **Output LPF**
- **Reference input**
- **Freq. multiplier**
- **Phase shifters**

System Connection Schematic Diagram

Libera Bunch-by-Bunch Front End Principle of Operation

Transverse instabilities→ Amplitude modulation

Mixing: $A(t) \sin(3\omega RFt) \sin(3\omega RFt) = A(t) (\cos(0) - \cos(6\omega RFt))$

After LPF: $A(t)$

Longitudinal instabilities→ Phase modulation

Mixing: $\sin(3\omega RFt + \varphi(t)) \cos(3\omega RFt) = \sin(6\omega RFt) + \sin(\varphi(t))$

After LPF: $\sin(\varphi(t)) \rightarrow \varphi(t)$

Libera Bunch-by-Bunch Front End Level Setting

- **Separate for X, Y and I channels**

- **-20 dBm to -60 dBm for X and Y**

- **-10 dBm to -50 dBm for I**

Libera Bunch-by-Bunch Front End Demodulation Angle Setting

- **Separate LO angle setting for X, Y, IL and IT (-π to +π)**

- **Additional common angle setting for all channels**

- **1 degree step**

Common phase setting
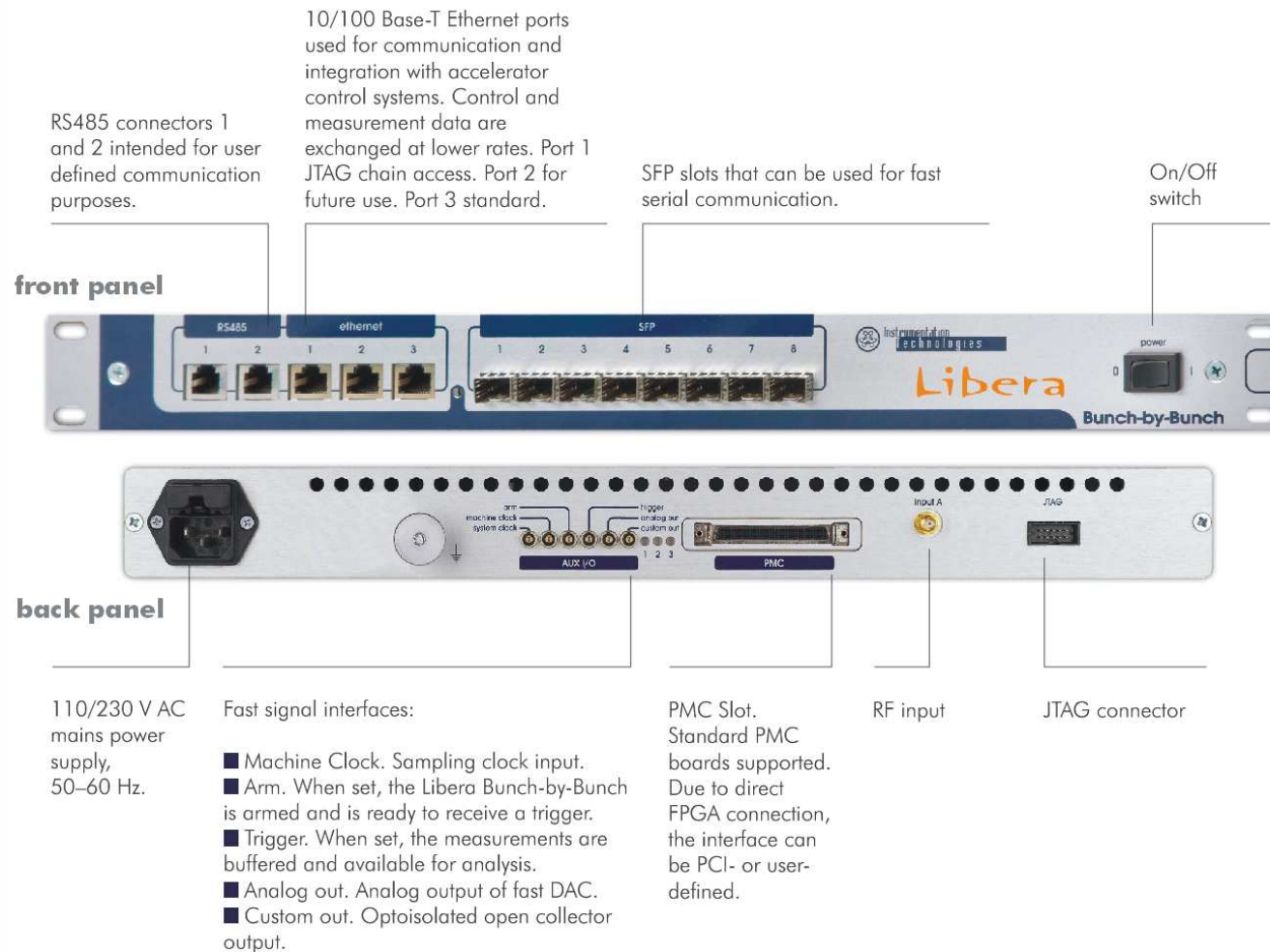
Local oscillator Y phase setting

Libera Bunch-by-Bunch Front End Software

- **The SW release is fully functional:**

    — **Control of all processing parameters**

    — **USB interface**

    — **Ethernet interface (telnet)**

- **Software is upgraded through the serial port on the front panel, simple procedure**

Libera Bunch-by-Bunch Front End
Main User Benefits

- All-in-one standalone unit, standard 1U factor.

- One unit for pre-processing of signals for all feedback loops.

- Independent phase and amplitude adjustment for each processing channel.

- High dynamic range.

- Low noise.

- Ethernet interface for integration in the control system.

- Simple for installation and use.

Libera Bunch-by-Bunch
Front and Back Panel

10/100 Base-T Ethernet ports used for communication and integration with accelerator control systems. Control and measurement data are exchanged at lower rates. Port 1 JTAG chain access. Port 2 for future use. Port 3 standard.

RS485 connectors 1 and 2 intended for user defined communication purposes.

SFP slots that can be used for fast serial communication.

On/Off switch

front panel

back panel

110/230 V AC mains power supply, 50–60 Hz.

Fast signal interfaces:

■ Machine Clock. Sampling clock input.
■ Arm. When set, the Libera Bunch-by-Bunch is armed and is ready to receive a trigger.
■ Trigger. When set, the measurements are buffered and available for analysis.
■ Analog out. Analog output of fast DAC.
■ Custom out. Optoisolated open collector output.

PMC Slot. Standard PMC boards supported. Due to direct FPGA connection, the interface can be PCI- or user-defined.

RF input

JTAG connector

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Communication with
Libera Bunch-by-Bunch

Interfaces:
- **Ethernet**
- **RS-232**

Software Interfaces:
- **CSPI Library**
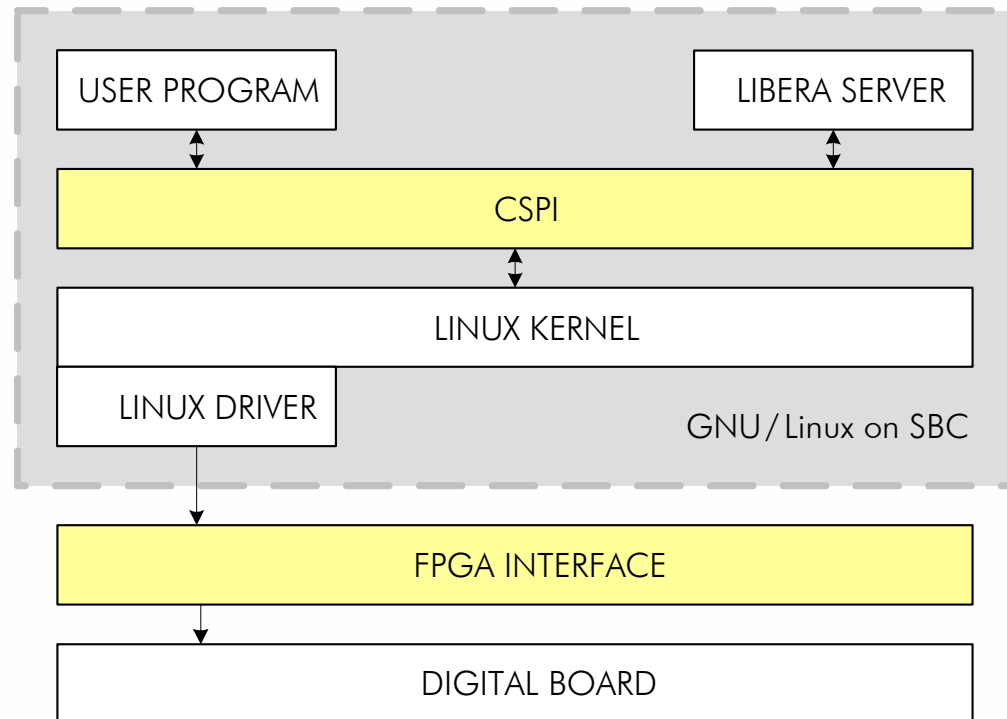- **Remote CSPI (over Generic Server). Example is GUI communication with Bunch-by-Bunch unit.**

Software Architecture

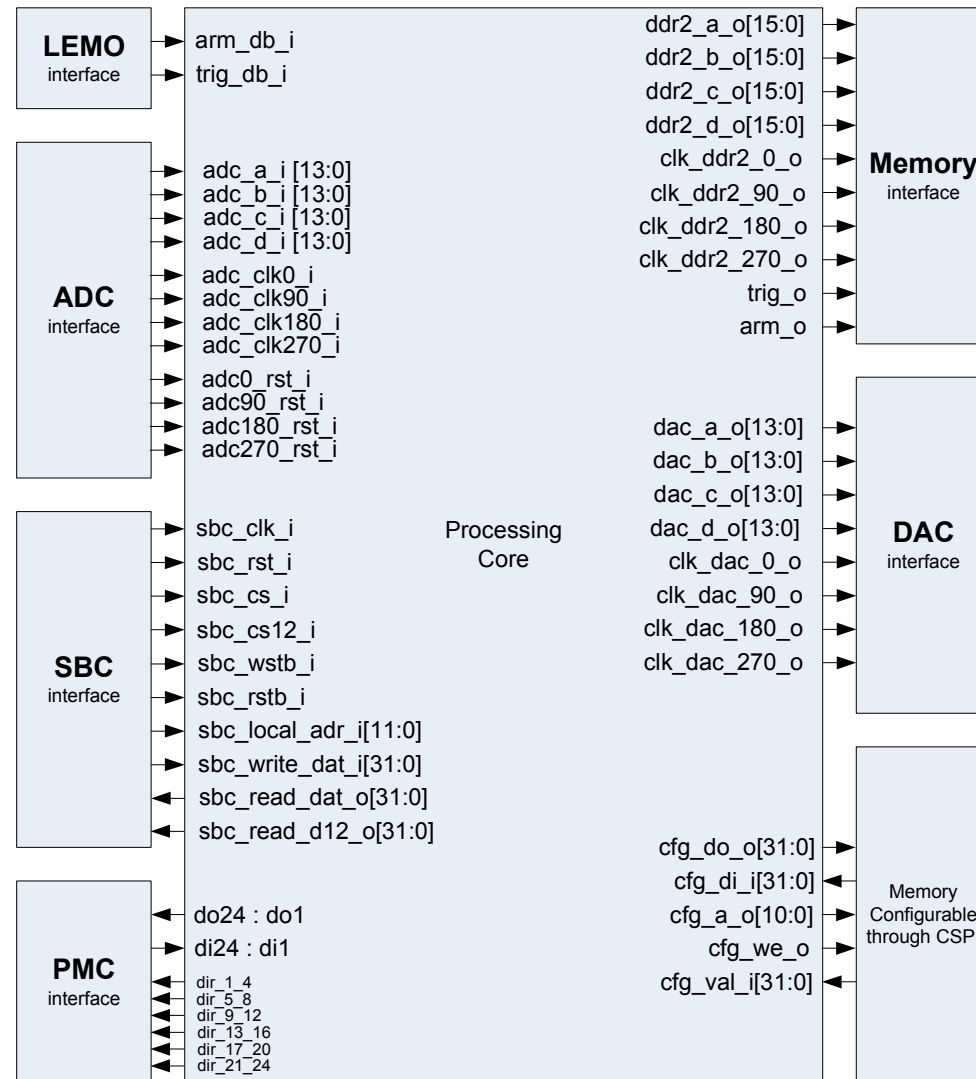**CORE:**

- **GNU/Linux**
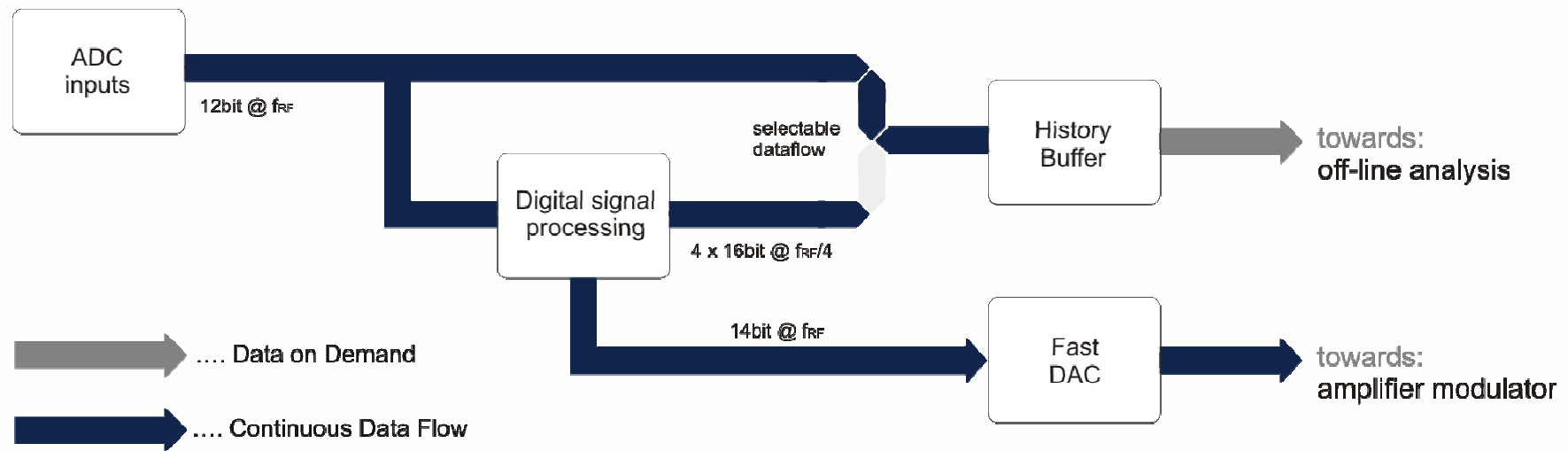- **Linux driver**
- **CSPI**

EXTENSIONS:

- **Libera Server**
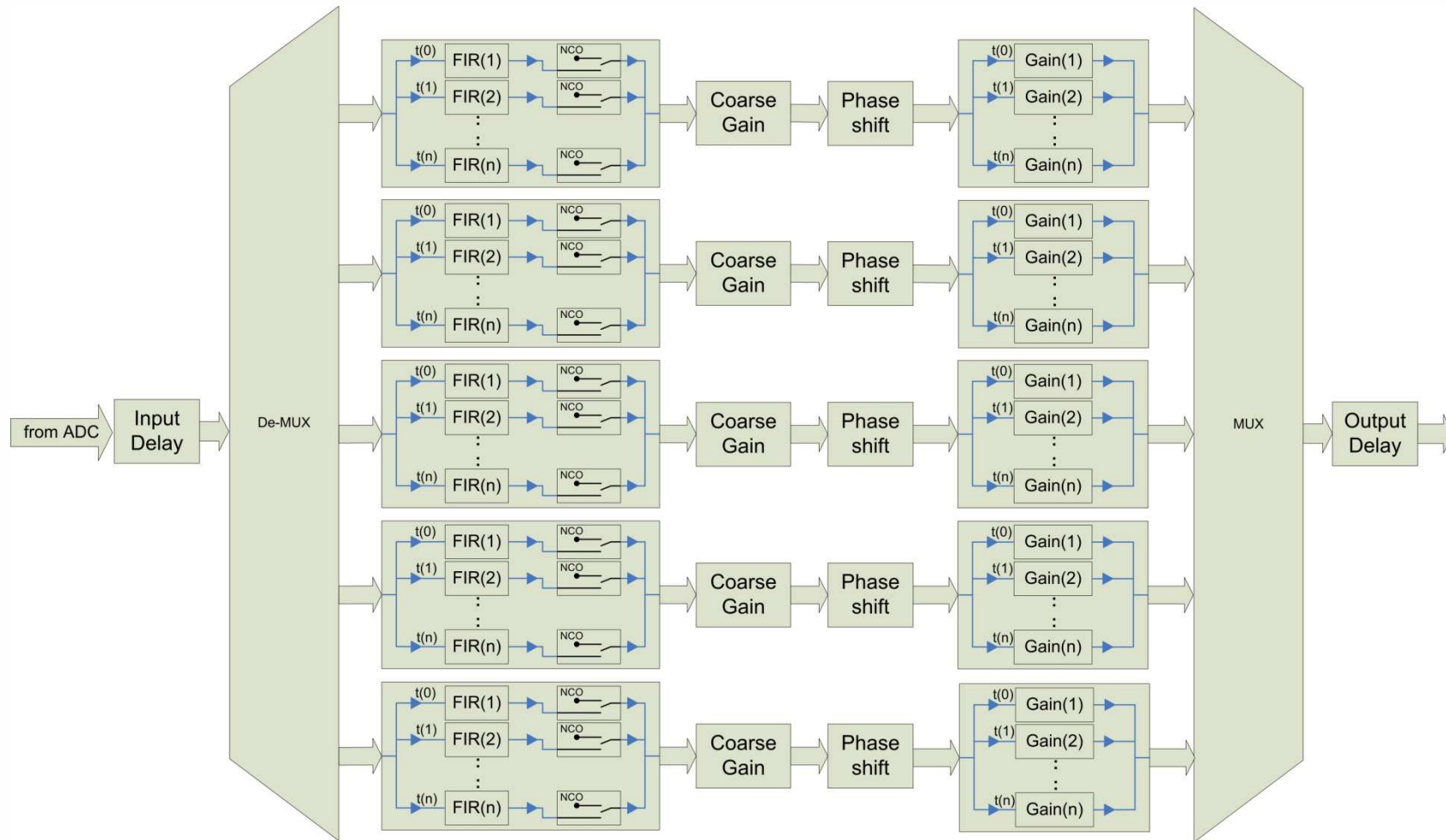- **User's Application**
- **Matlab based GUI**

USER PROGRAM		LIBERA SERVER
	CSPI	
	LINUX KERNEL	
LINUX DRIVER		GNU/Linux on SBC

FPGA INTERFACE

DIGITAL BOARD

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FPGA Architecture

LEMO interface
- arm_db_i
- trig_db_i

ADC interface
- adc_a_i [13:0]
- adc_b_i [13:0]
- adc_c_i [13:0]
- adc_d_i [13:0]
- adc_clk0_i
- adc_clk90_i
- adc_clk180_i
- adc_clk270_i
- adc0_rst_i
- adc90_rst_i
- adc180_rst_i
- adc270_rst_i

SBC interface
- sbc_clk_i
- sbc_rst_i
- sbc_cs_i
- sbc_cs12_i
- sbc_wstb_i
- sbc_rstb_i
- sbc_local_adr_i[11:0]
- sbc_write_dat_i[31:0]
- sbc_read_dat_o[31:0]
- sbc_read_d12_o[31:0]

PMC interface
- do24 : do1
- di24 : di1
- dir_1_4
- dir_5_8
- dir_9_12
- dir_13_16
- dir_17_20
- dir_21_24

Processing Core

- ddr2_a_o[15:0]
- ddr2_b_o[15:0]
- ddr2_c_o[15:0]
- ddr2_d_o[15:0]
- clk_ddr2_0_o
- clk_ddr2_90_o
- clk_ddr2_180_o
- clk_ddr2_270_o
- trig_o
- arm_o

Memory interface

- dac_a_o[13:0]
- dac_b_o[13:0]
- dac_c_o[13:0]
- dac_d_o[13:0]
- clk_dac_0_o
- clk_dac_90_o
- clk_dac_180_o
- clk_dac_270_o

DAC interface

- cfg_do_o[31:0]
- cfg_di_i[31:0]
- cfg_a_o[10:0]
- cfg_we_o
- cfg_val_i[31:0]

Memory Configurable through CSPI

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Data Flow

ADC inputs

12bit @ f_{RF}

Digital signal processing

selectable dataflow

4 x 16bit @ $f_{RF}/4$

History Buffer

towards: off-line analysis

14bit @ f_{RF}

Fast DAC

towards: amplifier modulator

.... Data on Demand

.... Continuous Data Flow

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Digital Signal Processing in Libera Bunch-by-Bunch

Libera Bunch-by-Bunch Processing Core
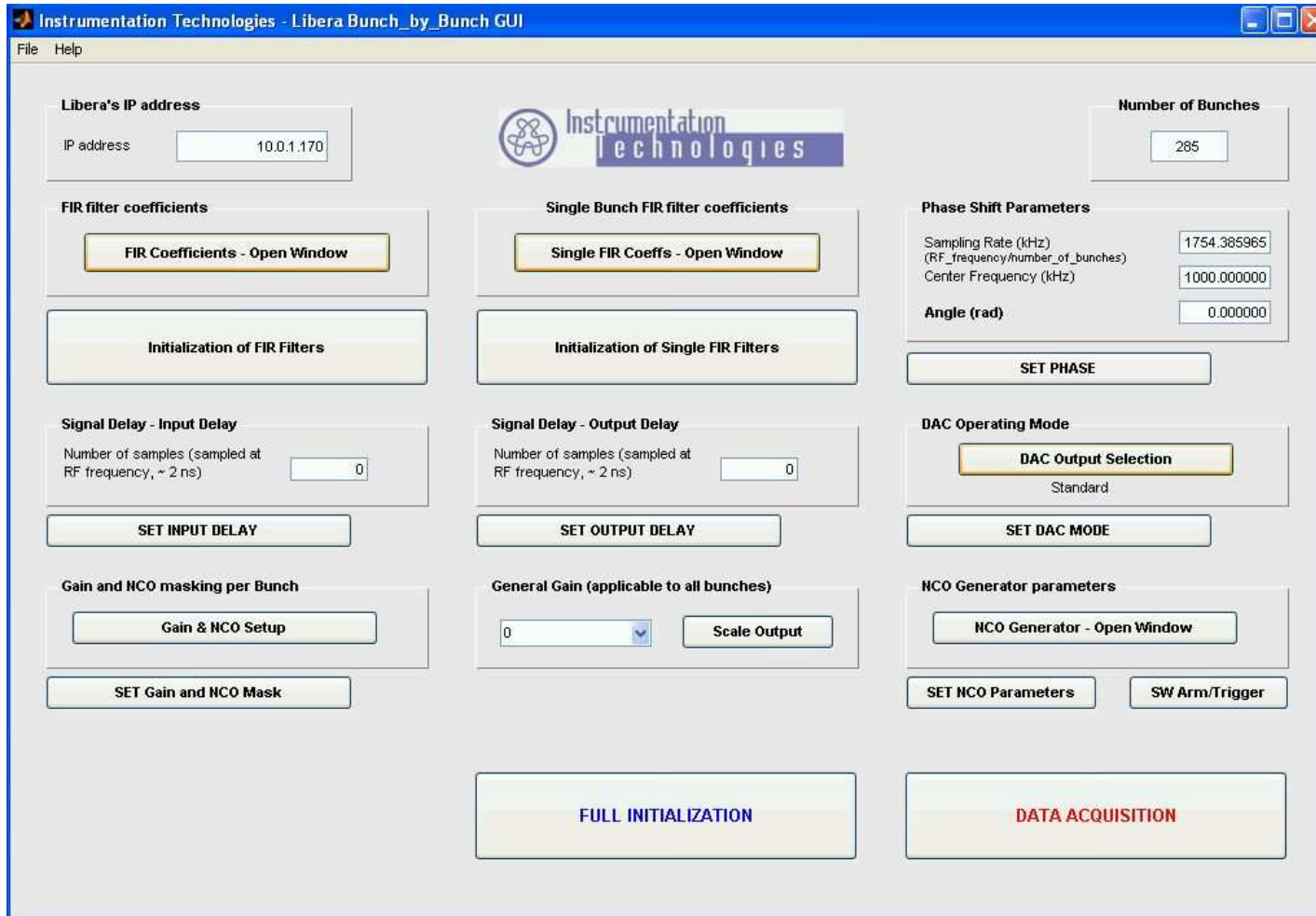
Features of the Libera Bunch-by-Bunch software release 2.00:

- **FIR filter, 16-tap**
- **Single bunch FIR filtering**
- **Input and output delay**
- **Phase shift**
- **DDR2 RAM input selection (ADC or processed data)**
- **Trigger type (standard or initiated at the start of data processing cycle)**
- **Gain setting (general gain for all bunches and gain per bunch)**
- **NCO generator for bunch purification (selectable per bunch)**
- **DAC operating mode (OFF – sends constant value to the output, ON – sends processed samples to the output)**

FPGA Development Kit - FDK

- Proprietary development environment, made by Instrumentation Technologies

- Uses Xilinx and Matlab tools.

- Processing core (almost all functionalities) are embedded in the System Generator Simulink Matlab model.

- User can enrich the existing functionalities.

Matlab based Graphical User Interface

Data Acquisition with GUI

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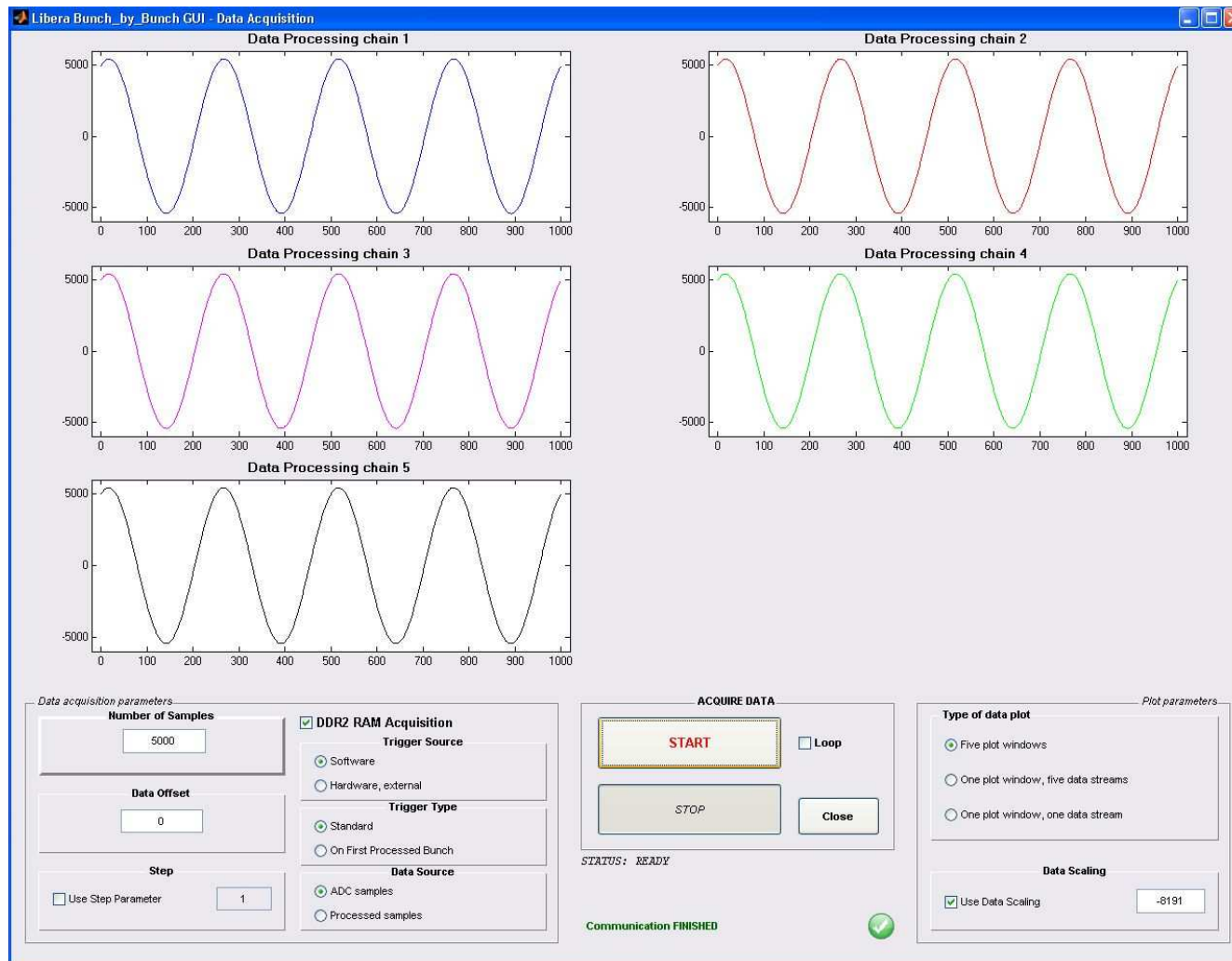
Reference List

Libera Bunch-by-Bunch:
- **ASP – Australia.**
- **ALBA – Spain.**
- **ANKA – Germany.**
- **CLS – Canada.**
- **Diamond Light Source – Great Britain.**
- **ESRF – France.**
- **LNLS – Brasil.**
- **NSRRC – Taiwan.**

Libera Bunch-by-Bunch Front End:
- **ASP – Australia.**
- **CLS – Canada.**
- **LNLS – Brasil.**
- **NSRRC – Taiwan.**

Libera Bunch-by-Bunch
Main User Benefits

- All-in-one standalone unit, standard 1U factor.

- Built on proven technology. Sharing of experience and support from the Libera community.

- Libera Bunch-by-Bunch can be directly connected to the Libera Bunch-by-Bunch Front End.

- Data sampling, digital signal processing and data storage up to 500 MHz rate. Bunch processing without decimation.

- Out-of-the-box ready for closing bunch-by-bunch feedback loop. All must-have features for successful loop closure are embedded.

Libera Bunch-by-Bunch
Main User Benefits

• **Easy to integrate in the control system; well documented and maintained high-level software library (CSPI API).**

• **Bunch cleaning, or bunch purification. Based on embedded NCO, selectable per bunch.**

• **FPGA Development Kit. Proprietary development environment for further processing core enrichment.**

• **Open Source model. All SBC software is under GNU/GPL License.**