Basic Functionality Presentation with Live Demonstration

Libera Electron Five Data Paths

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  - Turn by Turn Acquisition
  - Decimated Turn by Turn
  - Fast Acquisition
  - Slow Acquisition
- Some interesting features and principles with live demonstration
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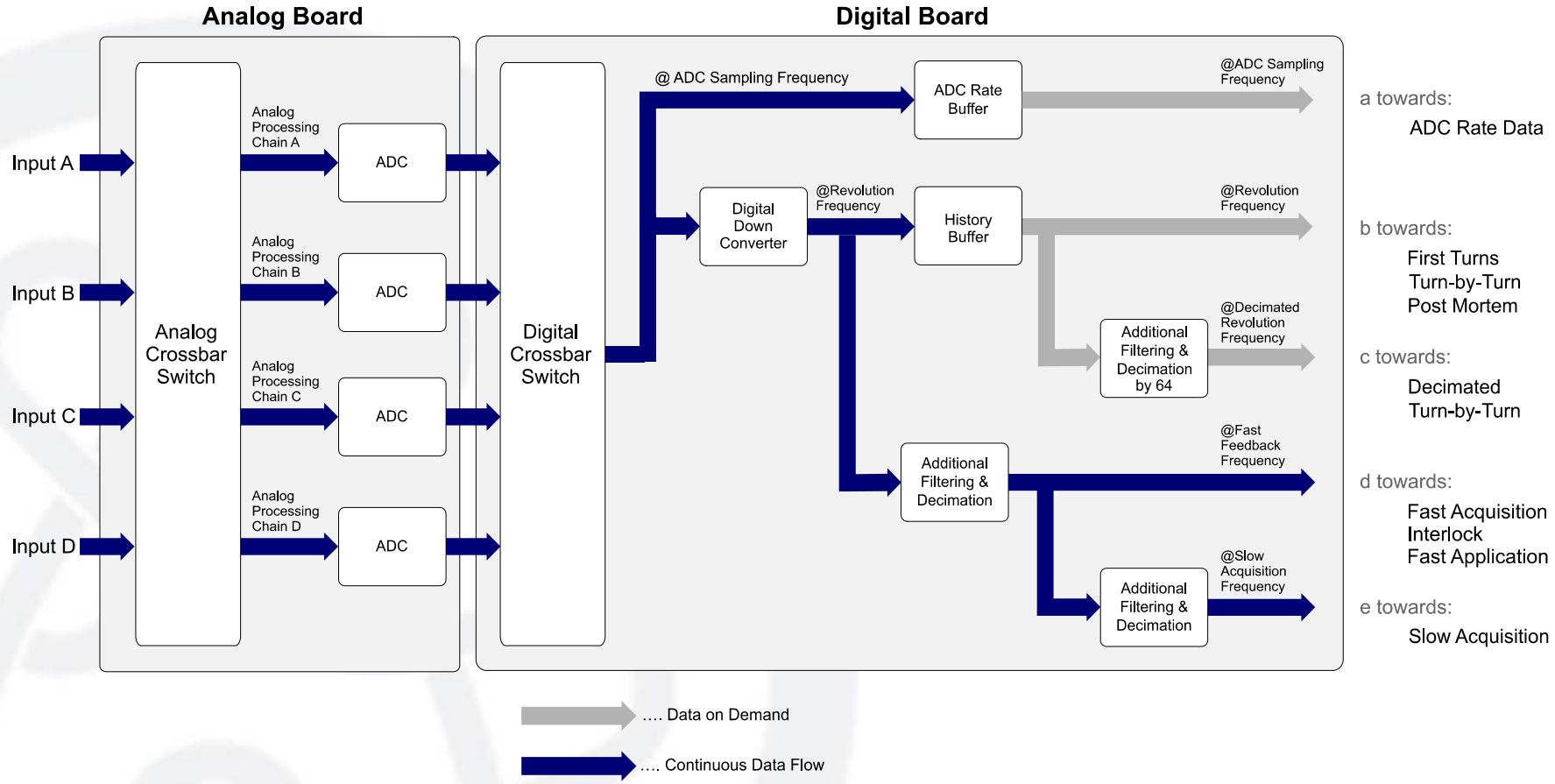
  - Synchronization
  - Interlock
  - Test-event utility

Introduction

- Libera Electron is growing into complex instrument.
- Users must put quite some effort to be able to take full advantage of Libera.
- We are getting lots of great ideas from the users. We are also getting idea of what features are important and what is less important for the user.
- This workshop is intended to gather Libera community and to make the above processes faster and more efficient.

Understanding Libera Data Flow



a towards:
- ADC Rate Data

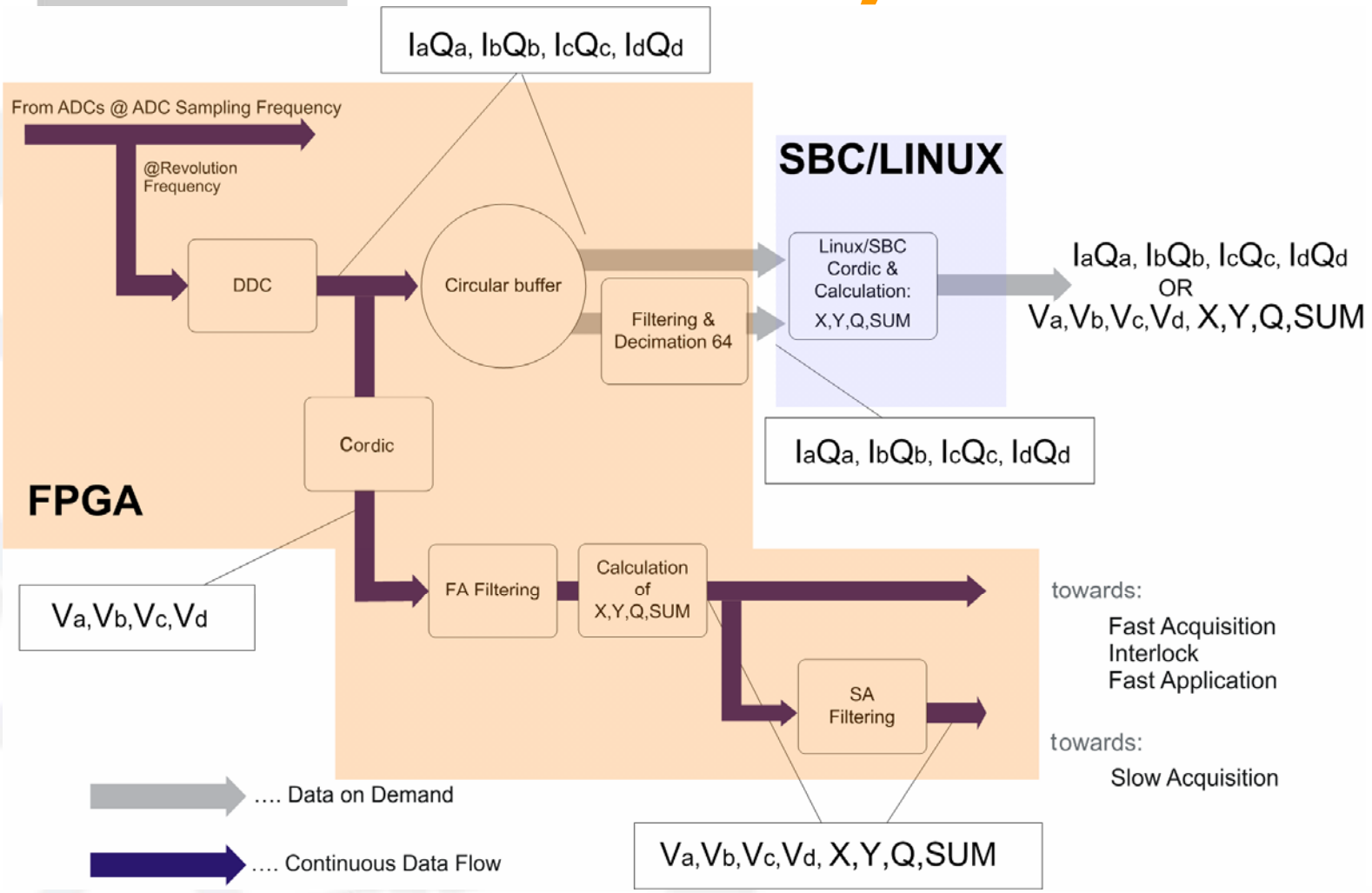
b towards:
- First Turns
- Turn-by-Turn
- Post Mortem

c towards:
- Decimated
- Turn-by-Turn

d towards:
- Fast Acquisition
- Interlock
- Fast Application

e towards:
- Slow Acquisition

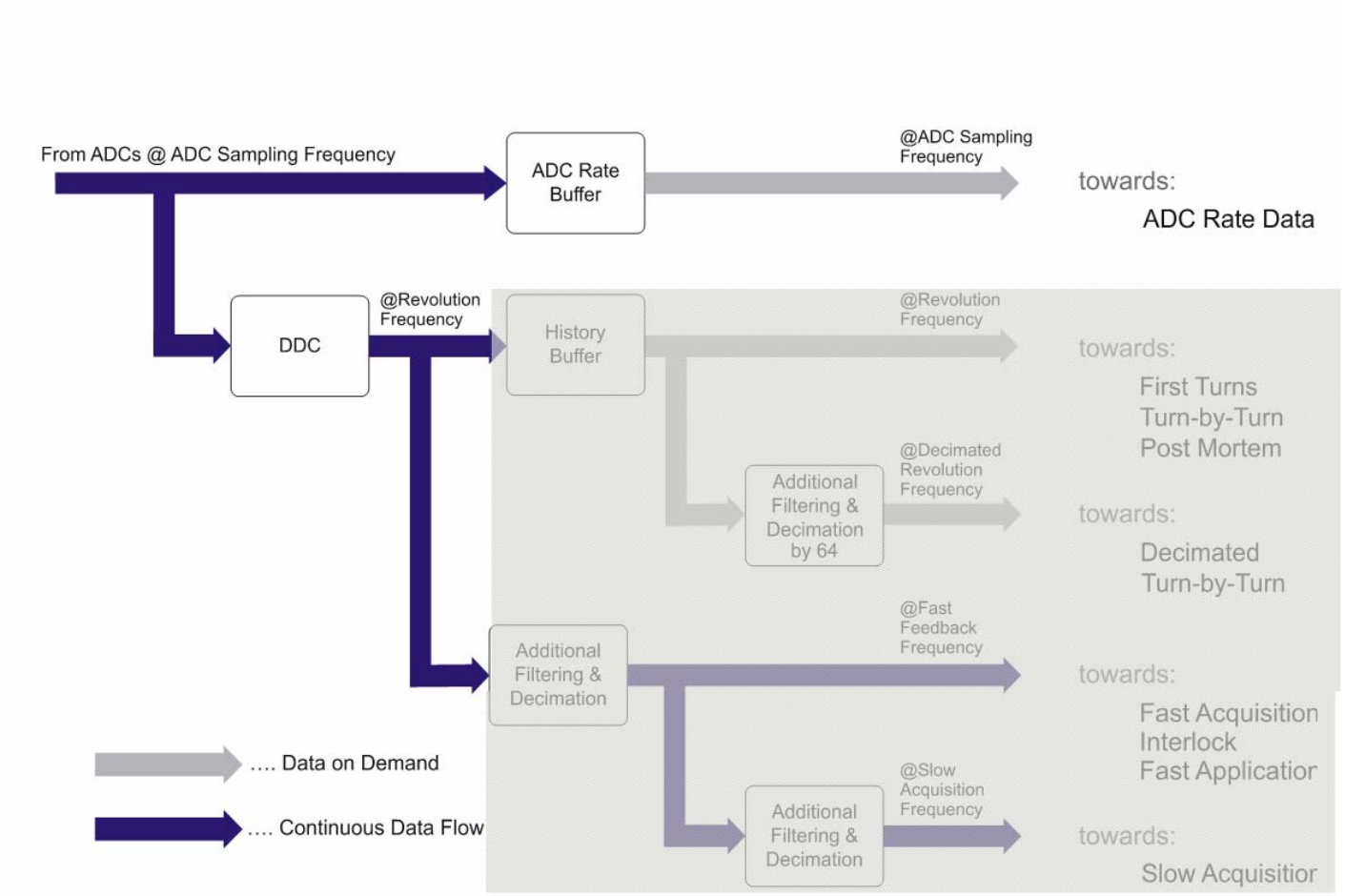
Data Format along the Data Paths, 1



Data Format along the Data Paths, 2

- Calculation of syntethic values:
  - ADC rate buffer data format
    - A, B, C, D
  - Turn by Turn data format
    - Either Ia, Qa, Ib, Qb, Ic, Qc, Id, Qd
    - or Va,Vb,Vc,Vd, X, Y, Q, Σ
  - Fast Acquisition data format
    - Va,Vb,Vc,Vd, Σ, Q, X, Y
  - Slow Acquisition data format
    - Va,Vb,Vc,Vd, Σ, Q, X, Y

ADC Rate Buffer, 1

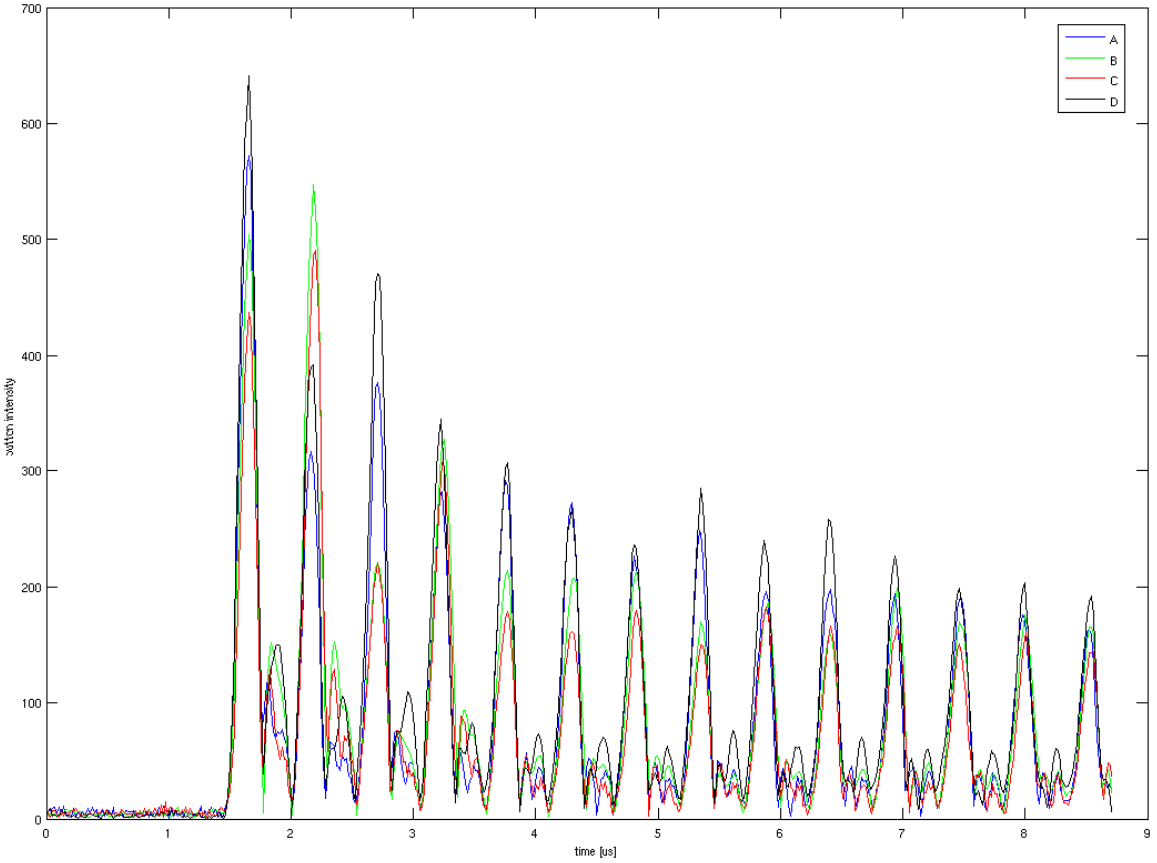


ADC Rate Buffer, 2

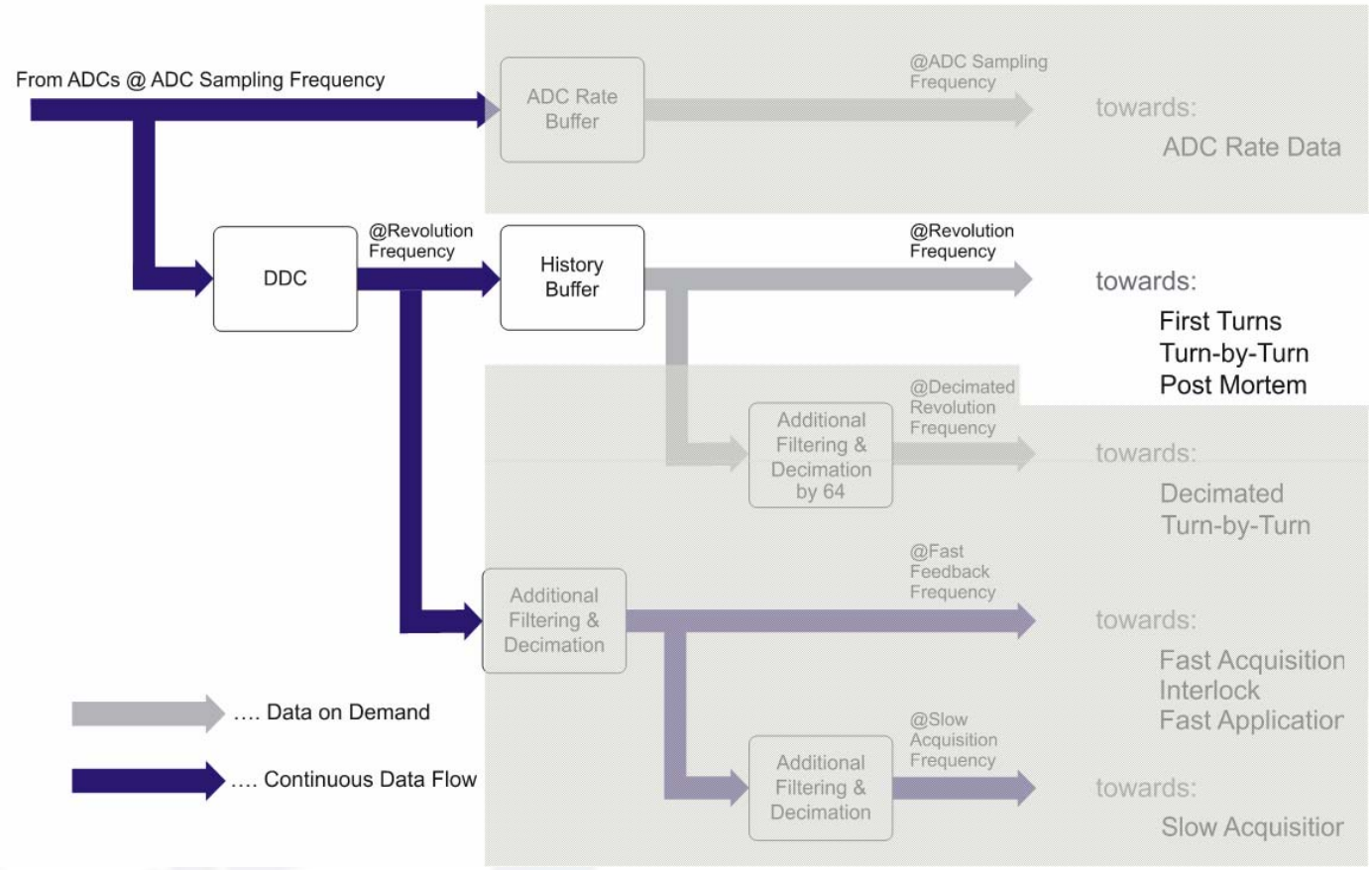
- Fast events, data rate 115-120MHz.
- BW of the measurement ~10MHz, determined by bandpass filters on the analog board.
- Acquisition on trigger.
- Buffer length 1024 samples.
- Typical delay 200-300ns, depending on RF board.

Diamond Booster Injection

Courtesy by G. Rehm



Turn by Turn Acquisition, 1

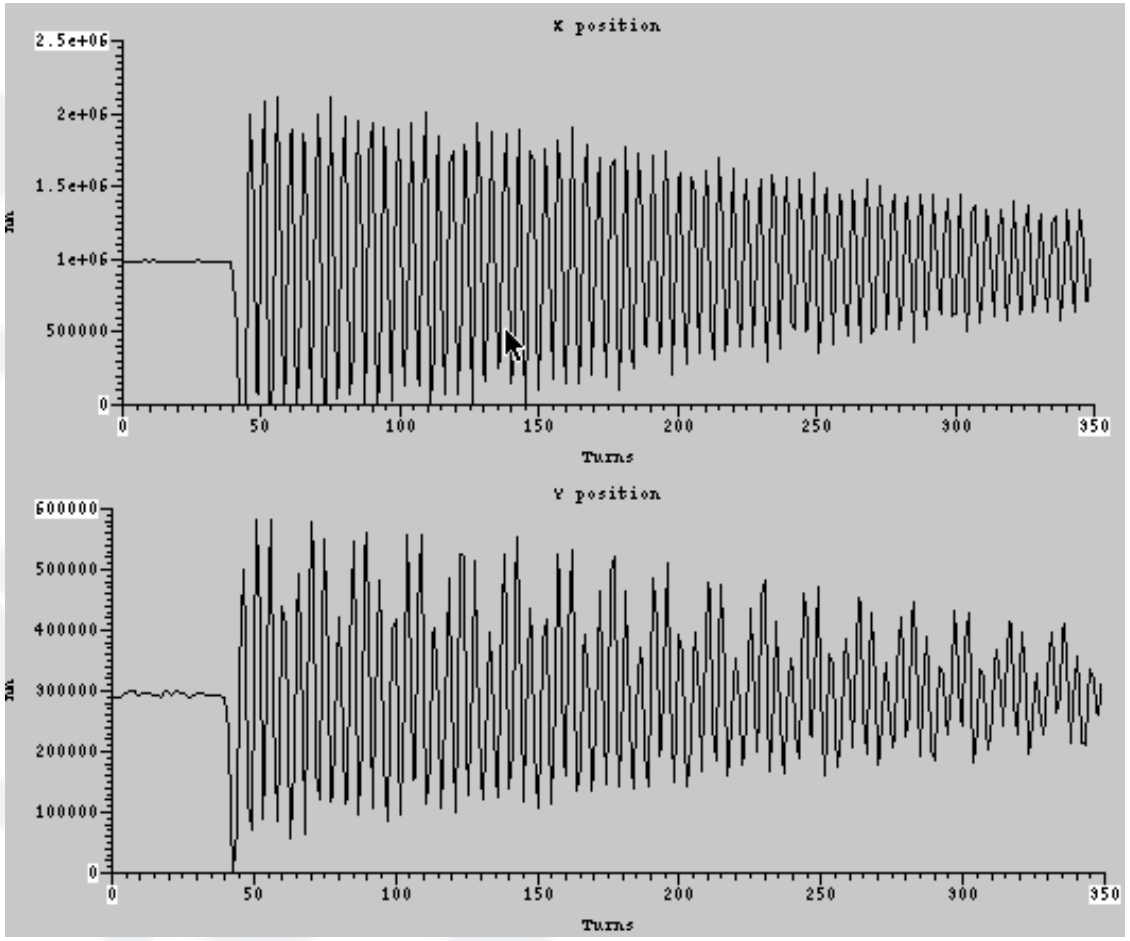


Turn by Turn Acquisition, 2

- Data rate at revolution frequency, data bandwidth approx 0.3*revolution frequency.
- Large circular buffer, implemented in SDRAM. Its length depends on the revolution frequency.
- Commissioning, machine physics studies.
- Post Mortem buffer 16k, copied to RAM on the PM trigger.

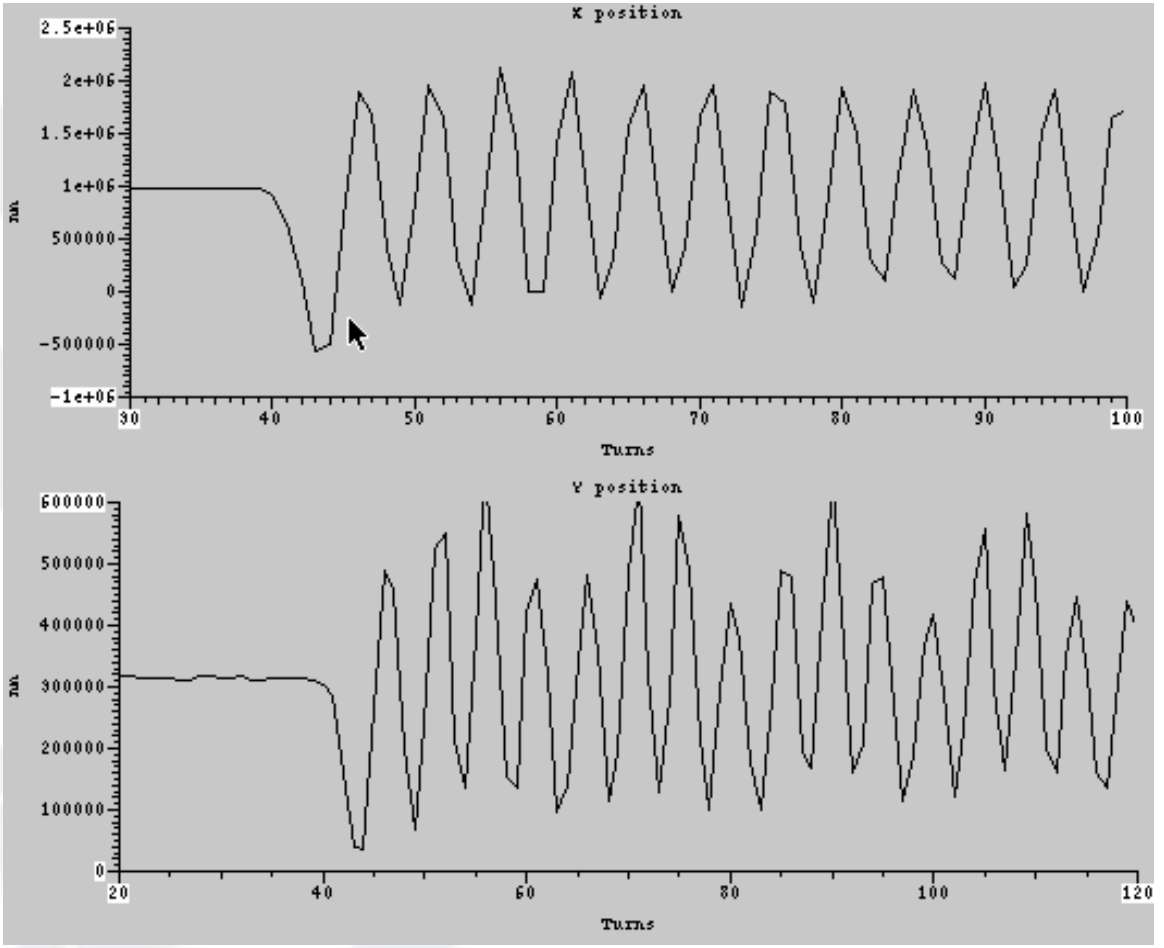
PLS Injection

Courtesy by K.M. Ha



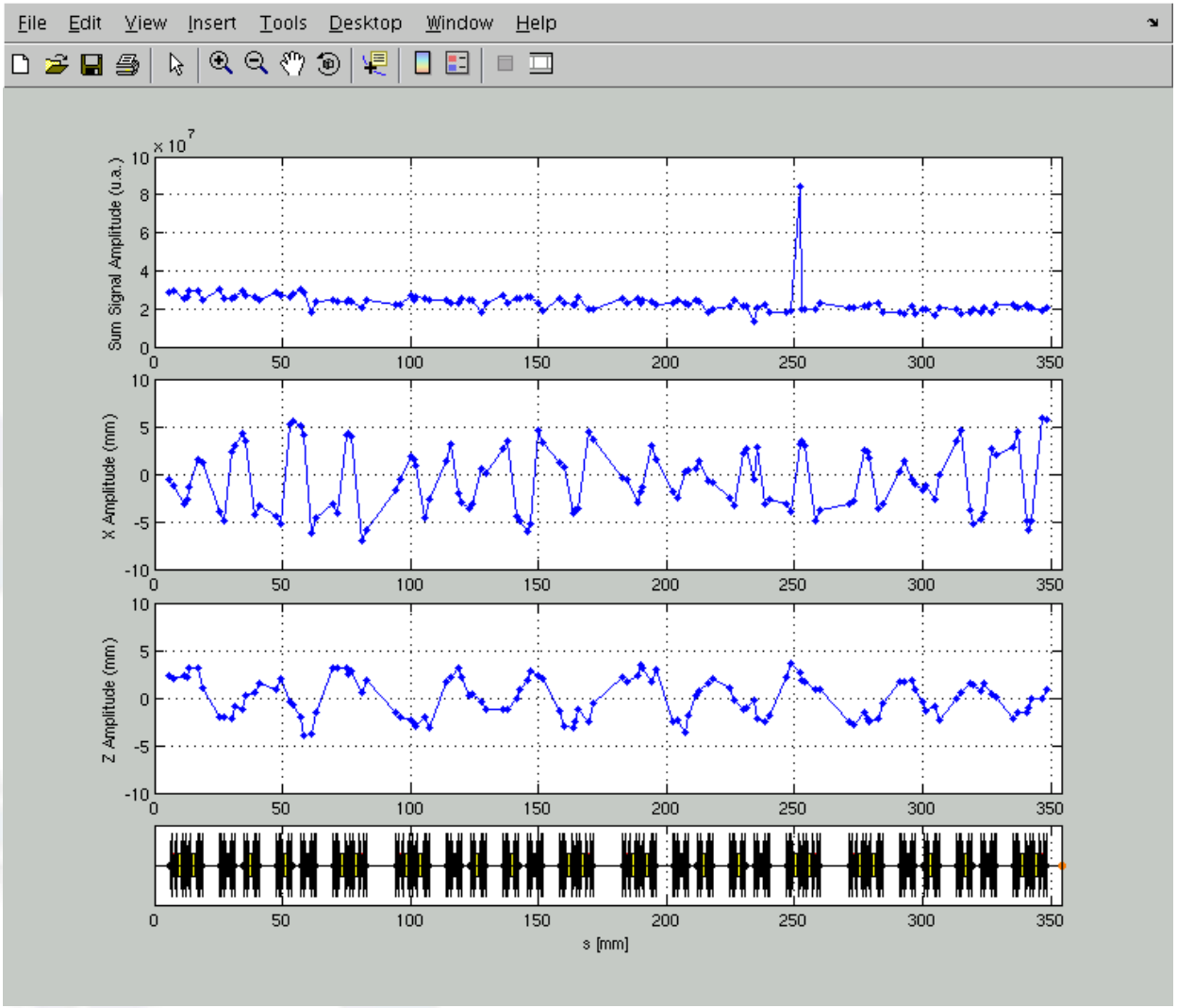
PLS Injection, Zoom

Courtesy by K.M. Ha

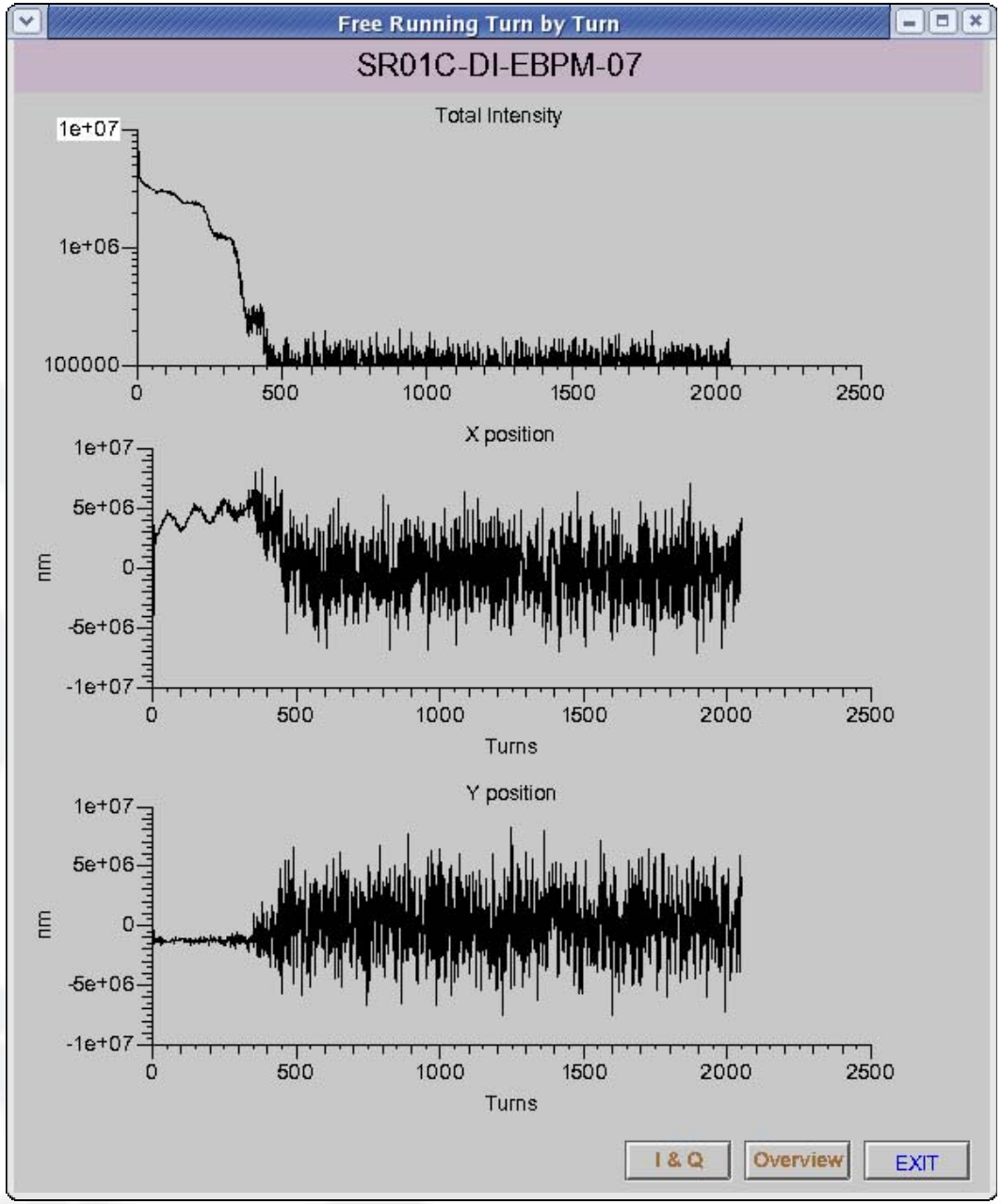


Soleil, Natural Orbit

Courtesy by J.C. Denard

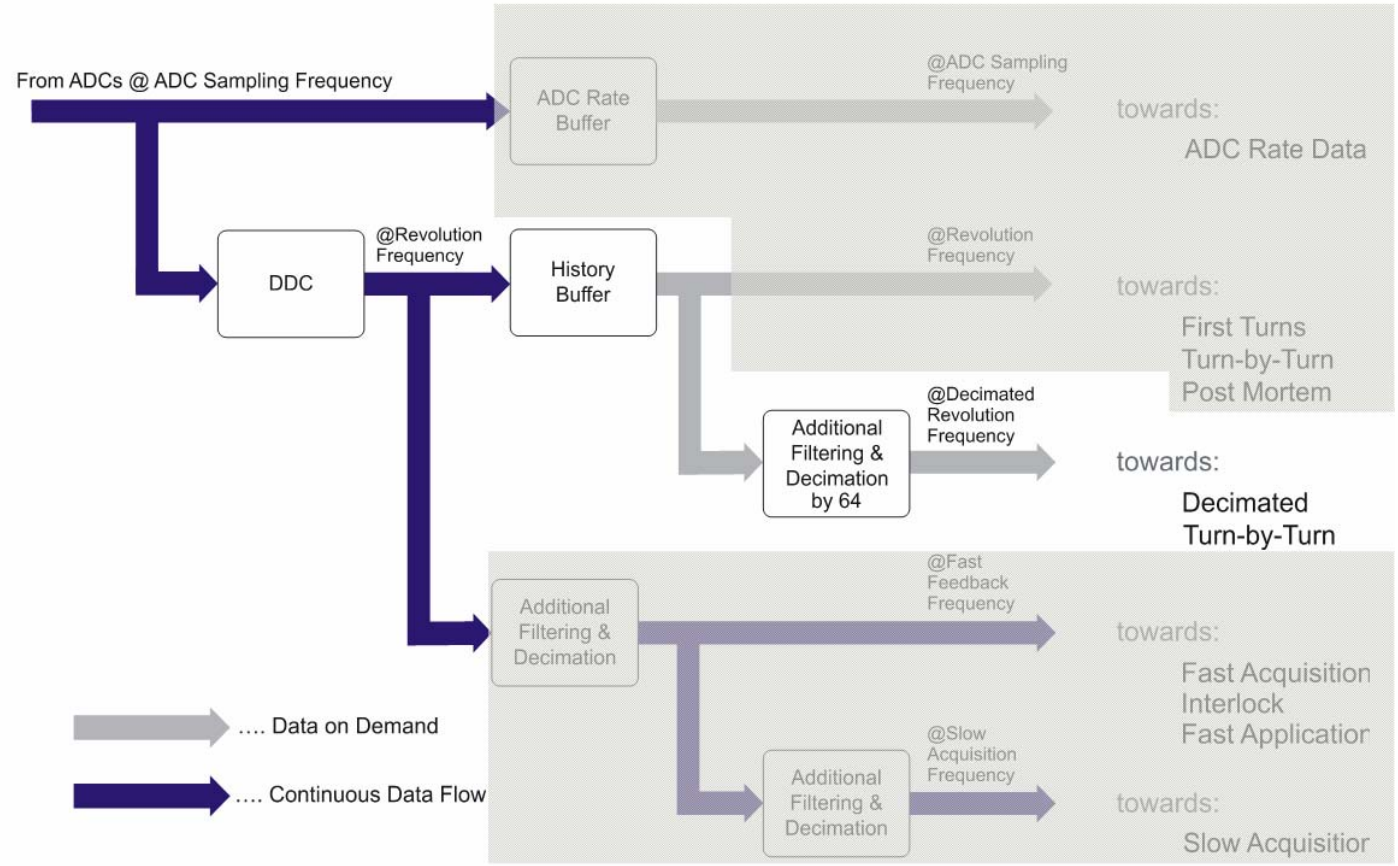


Diamond, Free Running TBT



Courtesy by G. Rehm

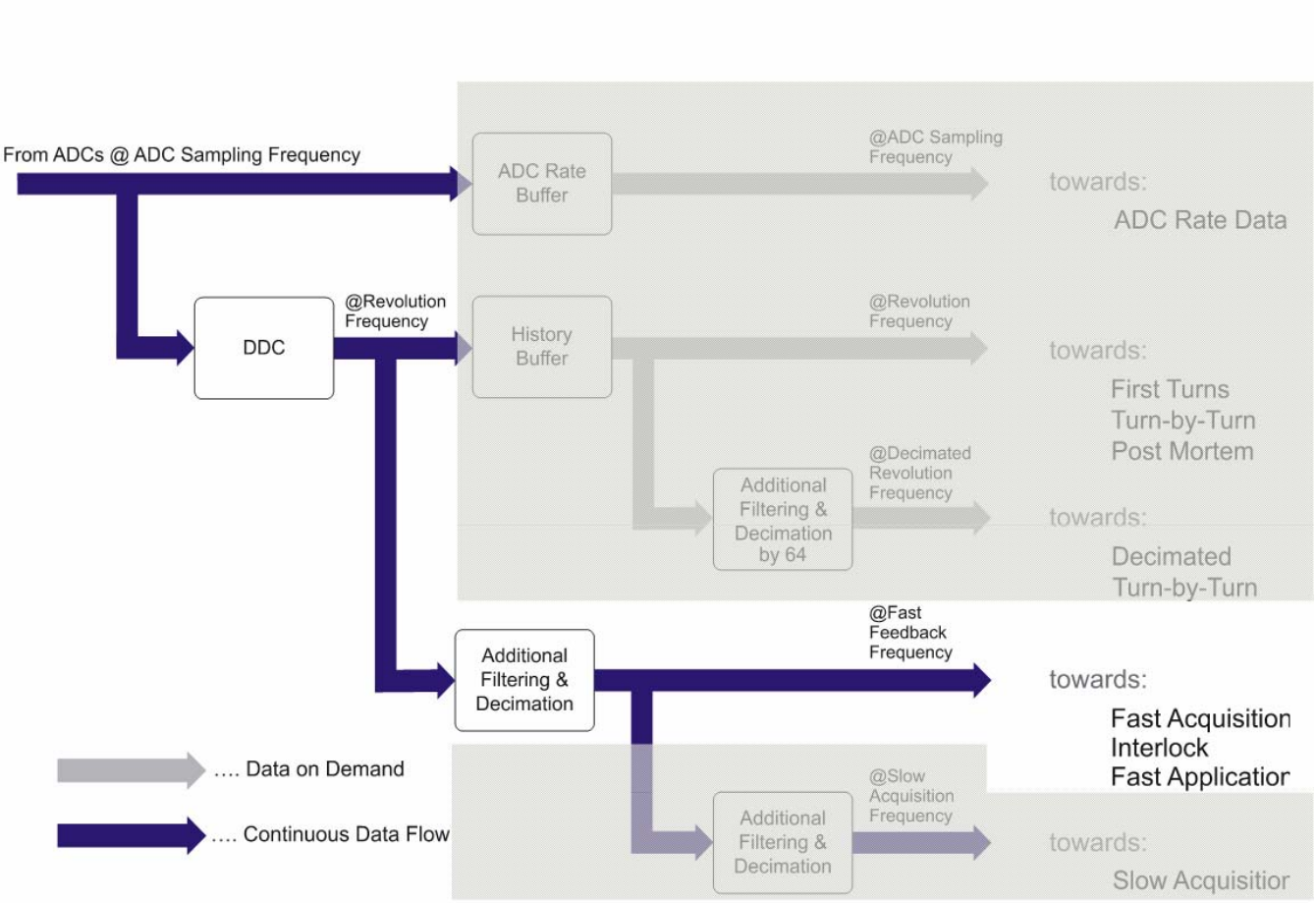
Decimated TBT, 1



Decimated TBT, 2

- Intended to follow relatively fast phenomena through longer time intervals.
- It simply averages the TBT data by a factor of 64.
- Max buffer length is 64ksamples, which usually equals a few seconds of history (>4 seconds if TBT = 1MHz).
- Example of usage: observation of few booster cycles.

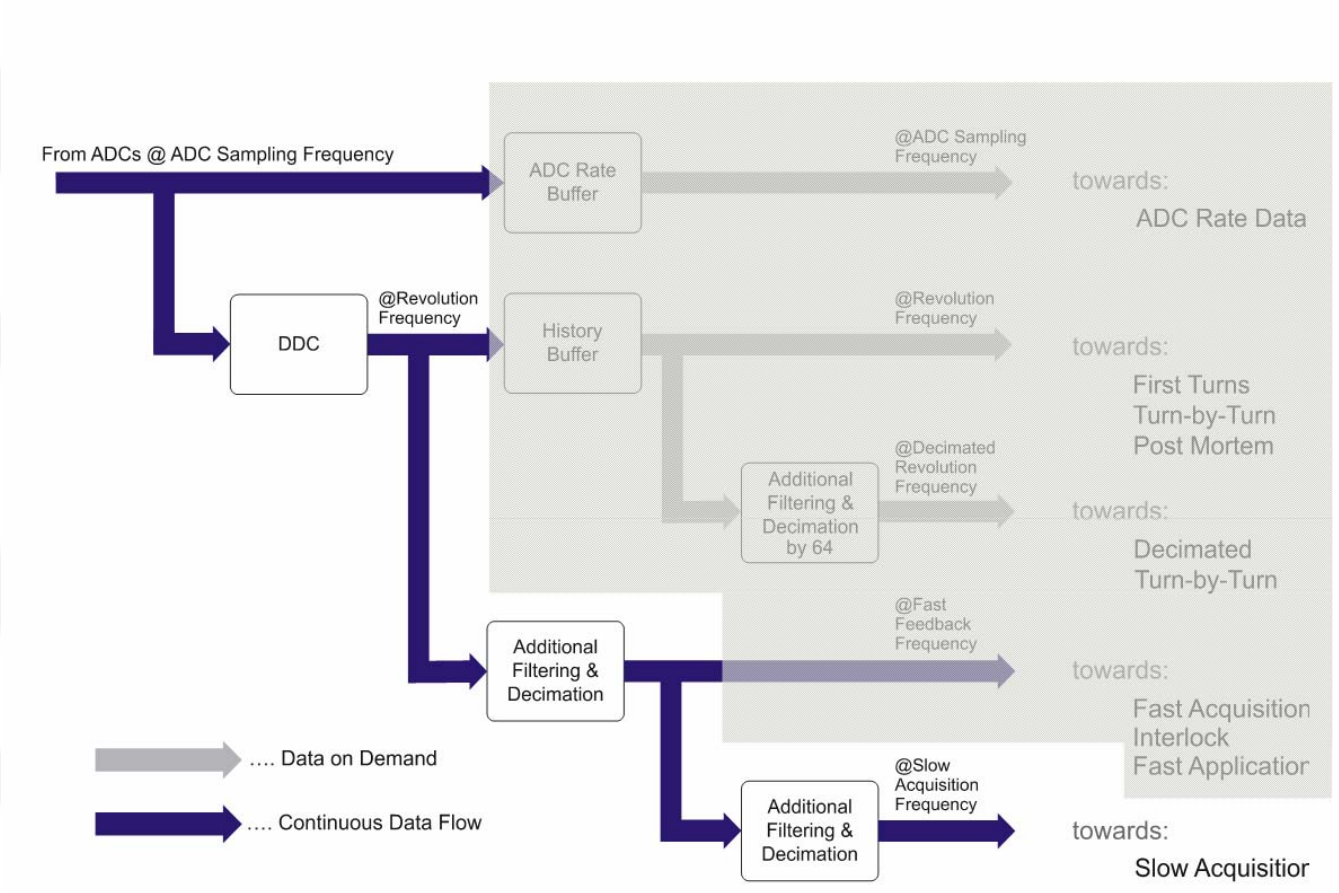
Fast Acquisition, 1



Fast Acquisition, 2

- Optimized filtering chain, Polyphase FIR.
- 2kHz bandwidth, ~10kHz rate.
- Input for:
  - Fast Application
  - Standard GB Ethernet output
  - SA filtering chain
- More about this in the next presentations.

Slow Acquisition, 1

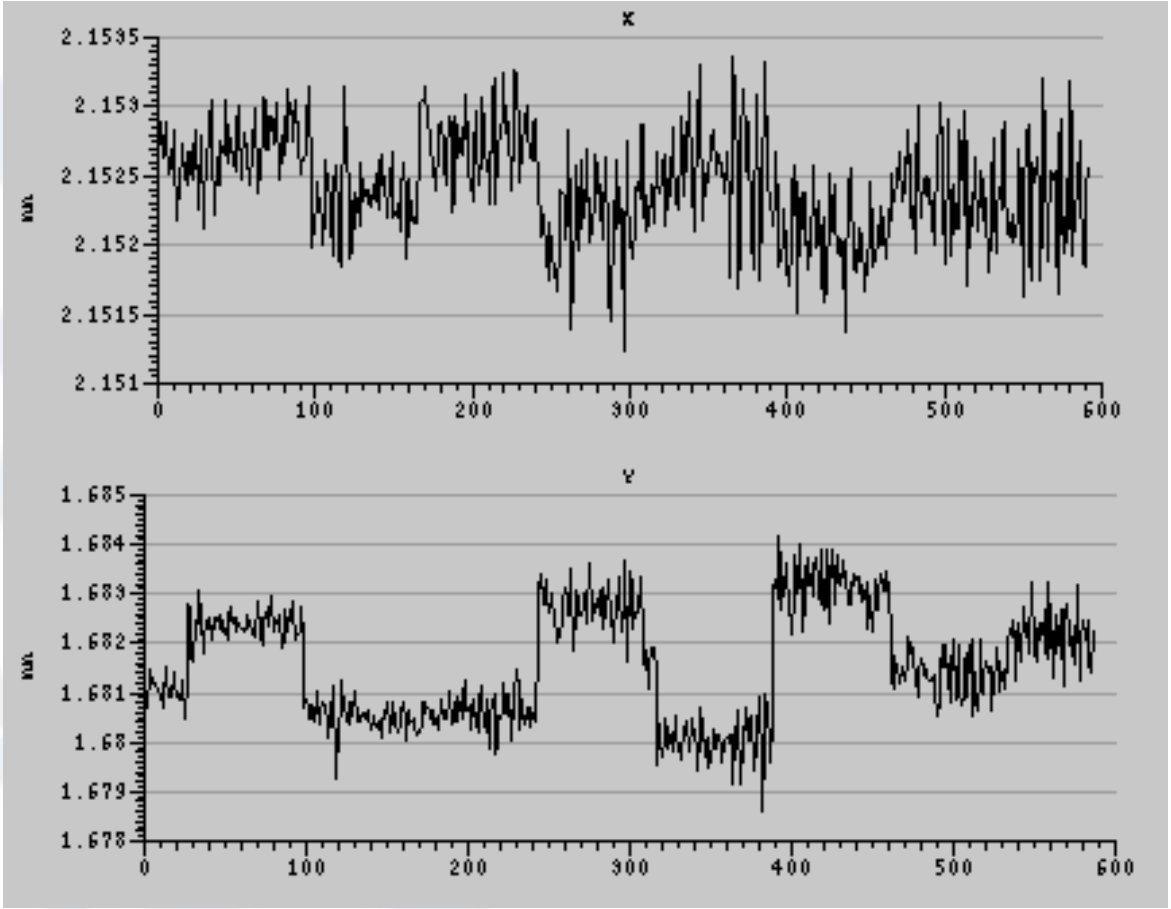


Slow Acquisition, 2

- For monitoring and for slow feedback calculation.
- Data rate at ~10Hz, accelerator dependent.
- ~4Hz bandwidth.
- Very low RMS.

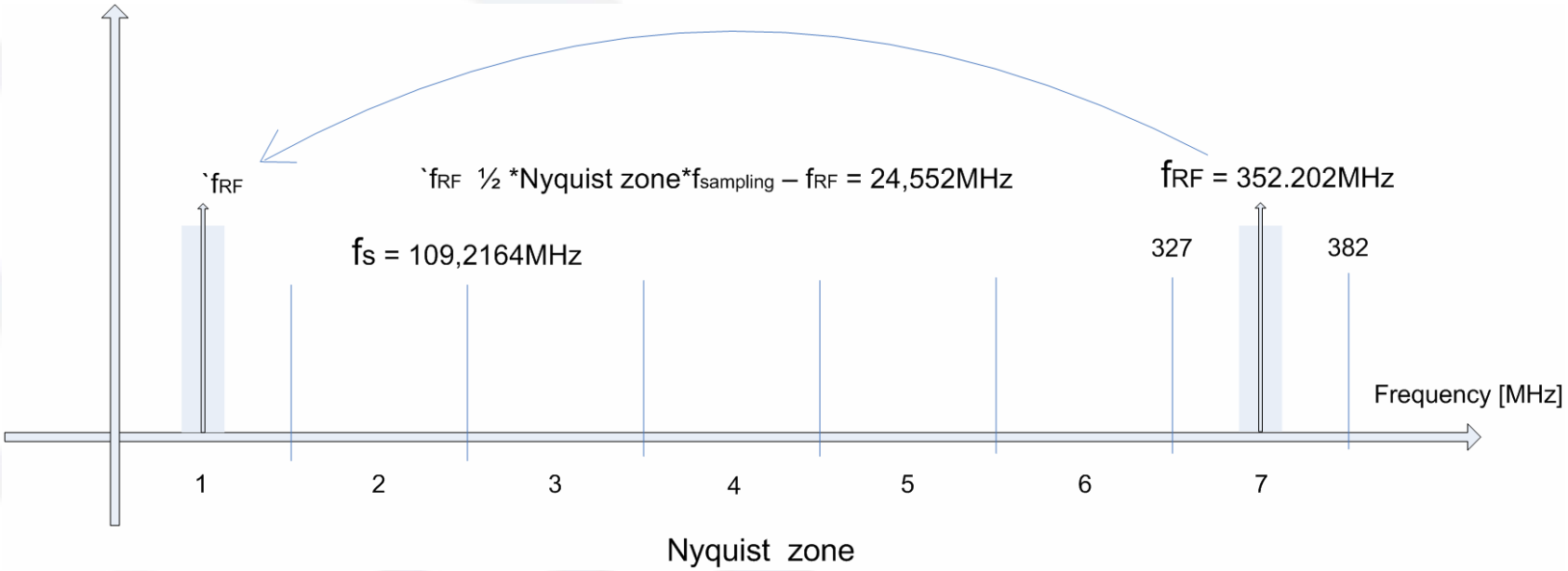
PLS, 60 Seconds

Courtesy by K.M. Ha

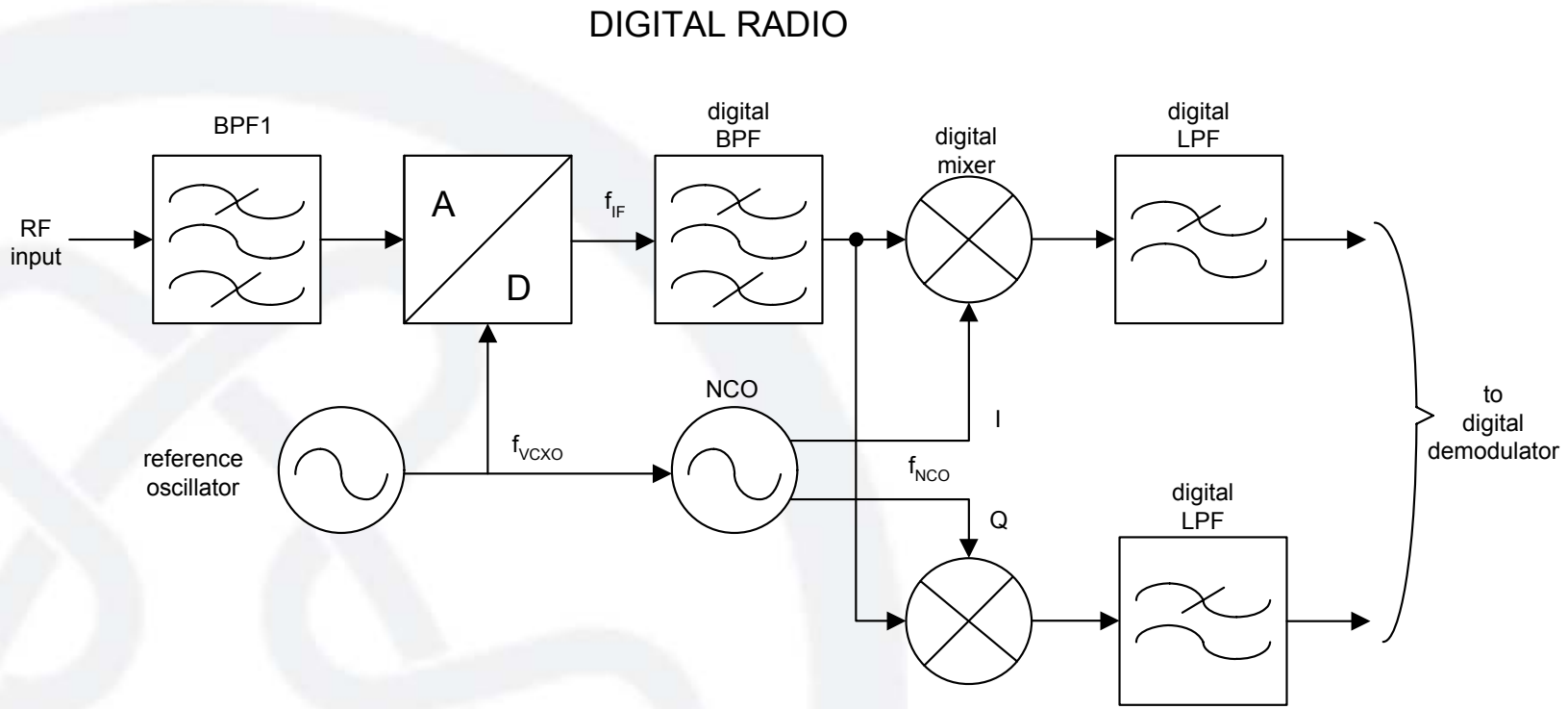


Undersampling

- Analog lowpass filters
- Analog bandpass saw filters



Mixing to Baseband



Synchronization of Acquisition

- ADCs driven by VCXO (Voltage Controled Crystal Oscillator).
- VCXO central frequency is an integer multiple of nominal revolution frequency of the accelerator.
- VCXO tuning range is ±90ppm
  - If VCXO is free running, it will go to its lower frequency limit (~45kHz below nominal @500MHz)
  - If VCXO is locked to MC reference, it will follow the changes of the RF frequency
- Synchronization mechanism
  - Needs MC reference input at revolution frequency
  - Synchronization with PLLs – low jitter
  - Precision of 1Hz
- Set_time trigger used for absolute synchronization of Liberas in the ring.

Synchronization of System Time

- VCXO with central frequency of 125MHz.
- VCXO tuning range is ±90ppm.
- Synchronization mechanism:
  - Needs SC reference input at 1MHz or 10MHz
  - Synchronization with PLLs
- Set_time trigger used for absolute synchronization with accelerator timing system

Interlock

- Measured at FA (10kHz) rate.
- Interlock is checking validity of X and Y position separately, lower and upper limit.
- Interlock can be disabled at low beam current levels (special setting), where there is lot of noise and no danger.
- Interlock can be disabled.
- ADC overflow (long enough) also triggers the Interlock.
- Interlock output is driven by an optocoupler, which is closed (shortcut) in normal operation.

Test-Event Utility

- Test-event utility is part of the CSPI debugging tests.
- It is included in the CSPI sources with each regular Release.
- The test-event utility can be used to monitor some or all events, depending on the mask parameter.
- For example, to monitor only the interlock signals, the mask should be set to 0x8

Test-Event Utility, Usage

- Usage (to follow just Interlock events): ./test-event 0x8
- Output examples:
  - id = 8 (INTERLOCK), param = 7 (-)

  Param=7 (00111), both X and Y positions are out of limit and Attenuator settings > limit value.
  - id = 8 (INTERLOCK), param = 28 (-)

  Param=28 (11100), points to ADC overflow, both filtered and non filtered and Attenuator settings > limit value.
- The usage and the parameters are well documented in the CSPI user manual.

Software Upgrades

- Regular software Releases are issued every 6 months. They have all latest features and bug fixes.
- It is recommended that the accelerators have the latest Release equipped.
- The installation is eased by well known (Red Hat like) structure of the software packets, with lpm (libera packet manager) extension.

Quality Assurance

- Each Libera goes through routine production testing (by the hardware manufacturer) and through final performance tests.
- A standard testing procedure is routinely performed on each Libera before shipping.
- The testing setup is standardized. Standard test record is issued and archived
- Each software release is thoroughly tested.
- All usage cases can't be foreseen in advance. We are therefore thankful for all possible problem reports, coming from users.
- The problems and possible bugs are always analyzed thoroughly. Libera performance gained a lot in the past from such collaboration with our users.

Libera Clock Splitter

- Splits the four inputs (system clock, machine clock, post mortem, trigger) to 40 LEMO outputs (four times ten)
- Merges ten Interlock input signals (from Liberas) to single Interlock output towards the control system