Elettra
Sincrotrone
Trieste

INSTRUMENTATION
TECHNOLOGIES

Development of eBPM Digital Board for Elettra 2.0

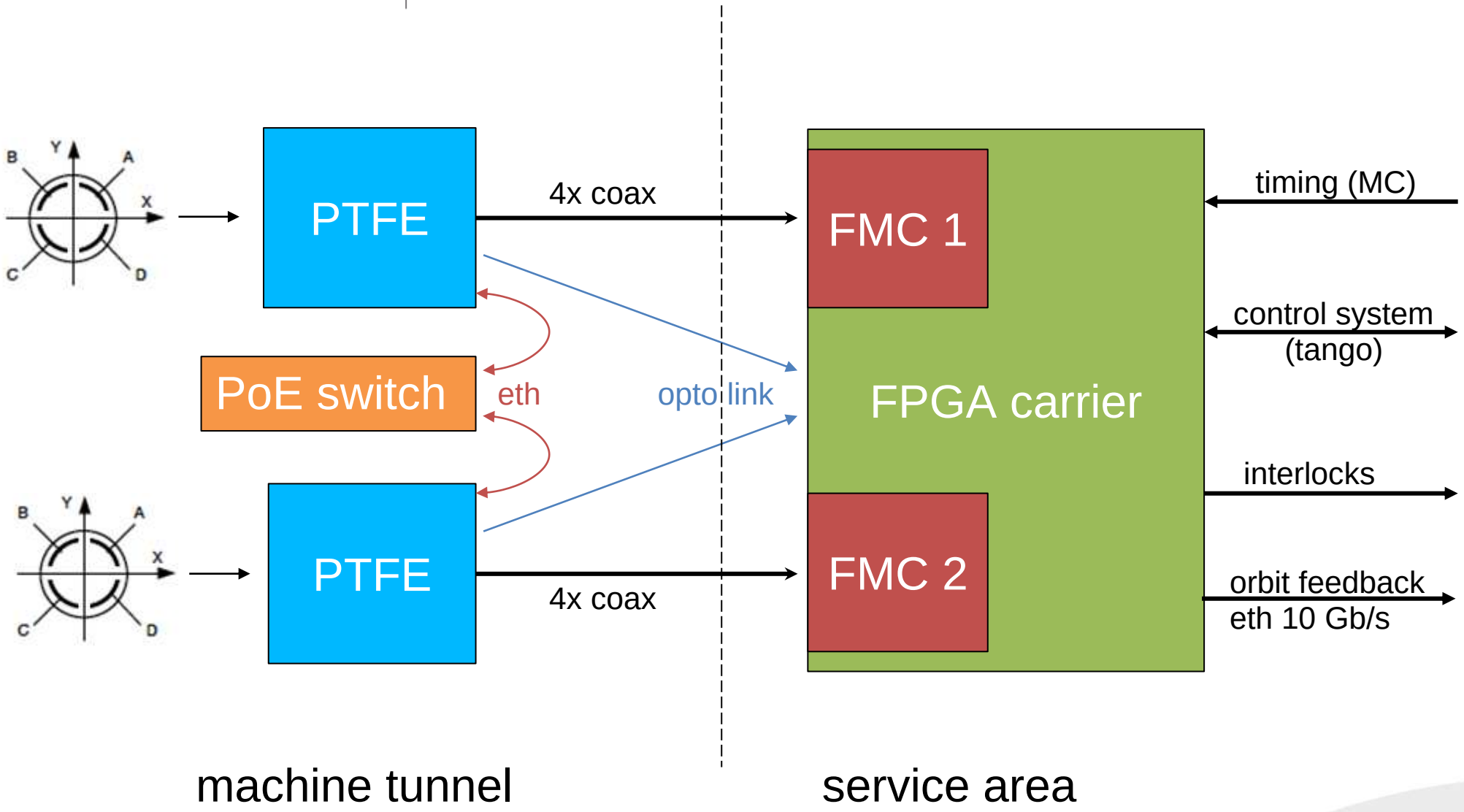
G. Brajnik, Elettra - Sincrotrone Trieste

Whole project overview

- Partnership with Instrumentation Technologies for the industrialization and production of 200 units of BPMs planned for Elettra 2.0, based on **pilot tone compensation**

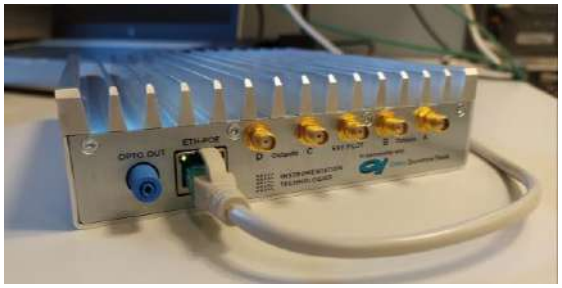
- Specifications:
  - Sub-micron resolution @ 10 kHz
  - Long-term stability better than 2 µm in 24 hours
  - Compensation of thermal drifts, channel variations, cables response
- Modular approach:
  - analog front end in the machine tunnel
  - digitizer in service area

Overall block diagram



Project current status

- First batch of 10 front ends produced and tested (FAT procedure on every unit)
- Additional 10 units already delivered at Elettra
- Mass production (remaining 190 units) is ongoing and expected to be finished in 2023
- Time to move on the digital part

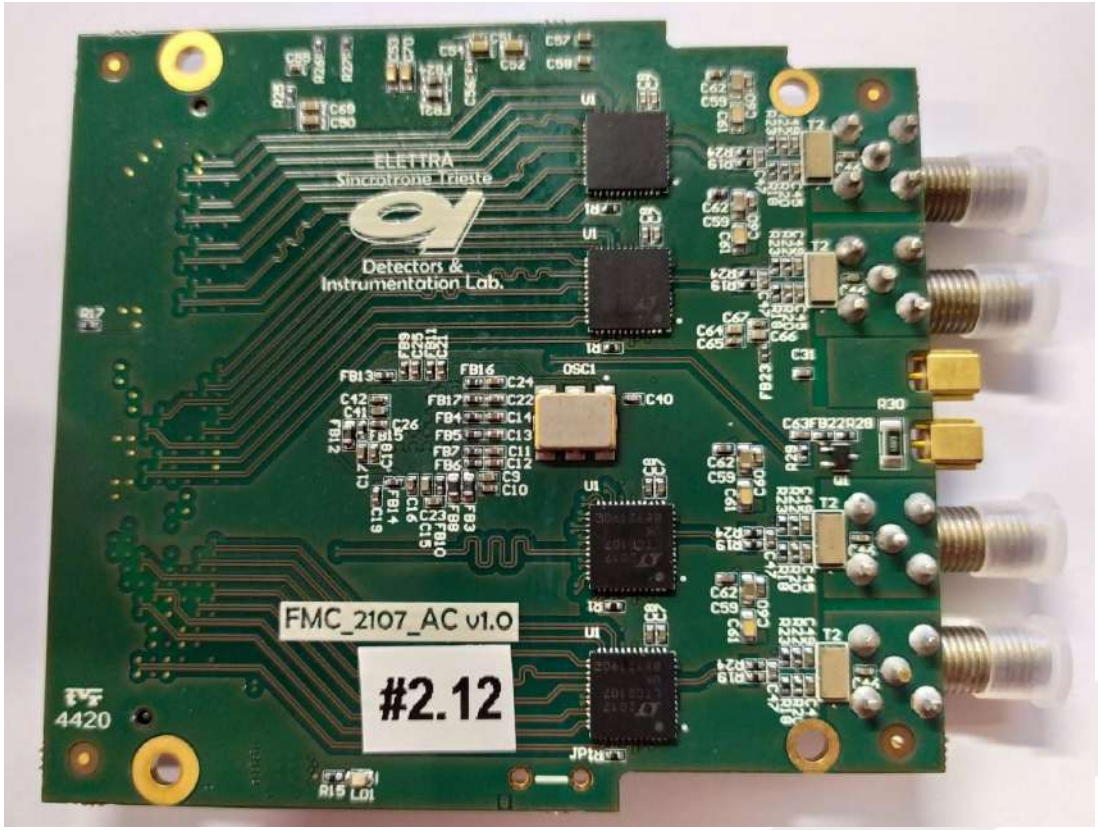


Digital board – FMC Cards

- Separation between **carrier board** and **FMC cards** with ADCs
- Pre-series of 4 FMC ADC cards completed with success

- Design confirmed and tested with extensive measurements (long-term tests)

- Additional 10 units currently in production at I-Tech



Digital board – Central Unit

- Board based on **Intel Arria 10 SoC FPGA**

- Previous experience with Intel/Altera FPGA family (Cyclone V/10, Arria 10 GX), used to verify FMC card performance and preliminary measurements of the overall BPM system

- Step forward
  - Bigger FPGA
  - Two FMC onboard -> **2 BPMs parallel processing**
  - From standard FPGA to SoC (with hard processor inside)

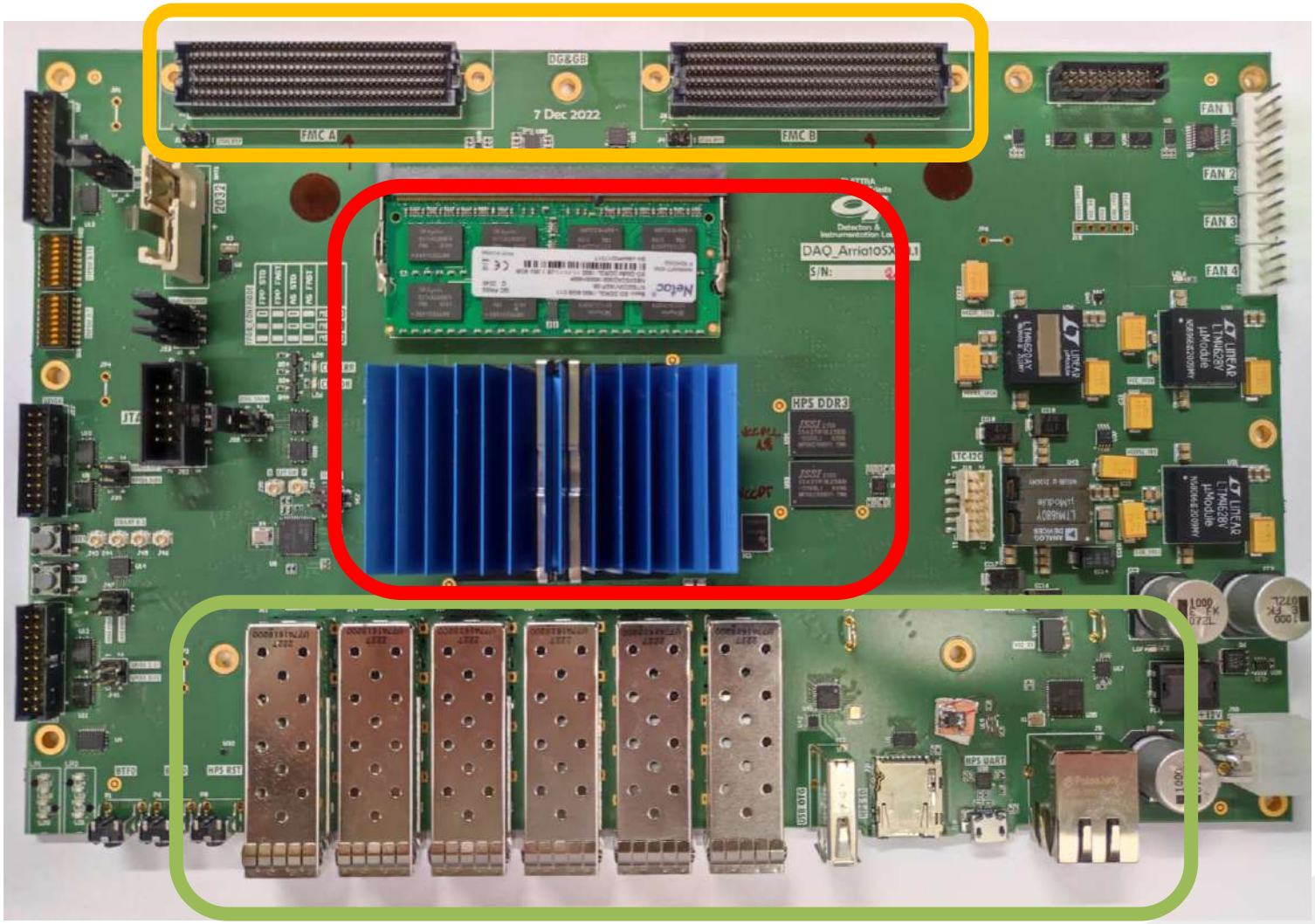
- **Dedicated chassis** designed by I-Tech

Digital board – Central Unit

FMC

DDR3
FPGA/HPS

SFP+
USB/ETH



Central Unit – front and back

CUSTOM 2U 19’ RACK

VENTILATION APERTURES

SFP+/ETH

I/Os

ADC INPUTS

Digital board – Central Unit

- Quite complex design:
  - DDR3 onboard (SODIMM + HPS)
  - 10 Gb/s transceivers (10 Gb Ethernet)
  - 400 pins per FMC
  - 1517 FPGA pins

- 16-layer printed circuit board (PCB)
- Impedance controlled differential pairs
- Additional hardware (clock generators, RTCs, fan controllers, USB/ETH PHY chips)

- **What can go wrong?** A lot of things!

Digital board – What can go wrong?

- Classification of faults/mistakes using 3 areas:

1. **Logical / schematic issues**: components not connected correctly (e.g. voltage mismatches on pins, power-up sequence)

2. **PCB design issues** (wrong footprint, impedance rules not obeyed, etc)

3. **Manufacturing issues:** problems during PCB production or assembly phase

Examples – Schematic issues

- **Serial port on HPS not working properly** on certain power sequence – due to Reset pin
- Datasheet unclear and modified – old datasheet still present on manufacturer's website

Revision	Changes	Date
Version 1.0	Initial Release	08-01-2013
Version 1.1	Updated TID info; Added clarification for 5V Tolerant	17-02-2013
Version 1.2	Added reference to WDFN Chip Dimensions	15-08-2015
Version 1.3	Removed Pin 13 from FT234XD Corrected the order of the chip marking text	09-12-2018
Version 1.4	Updated section 4.2 – reset can be connected to VCCIO if not used; Updated section 3.2 and section 7.5 to provide additional information on Tx and Rx LEDs	23-09-2021

Examples – Schematic issues

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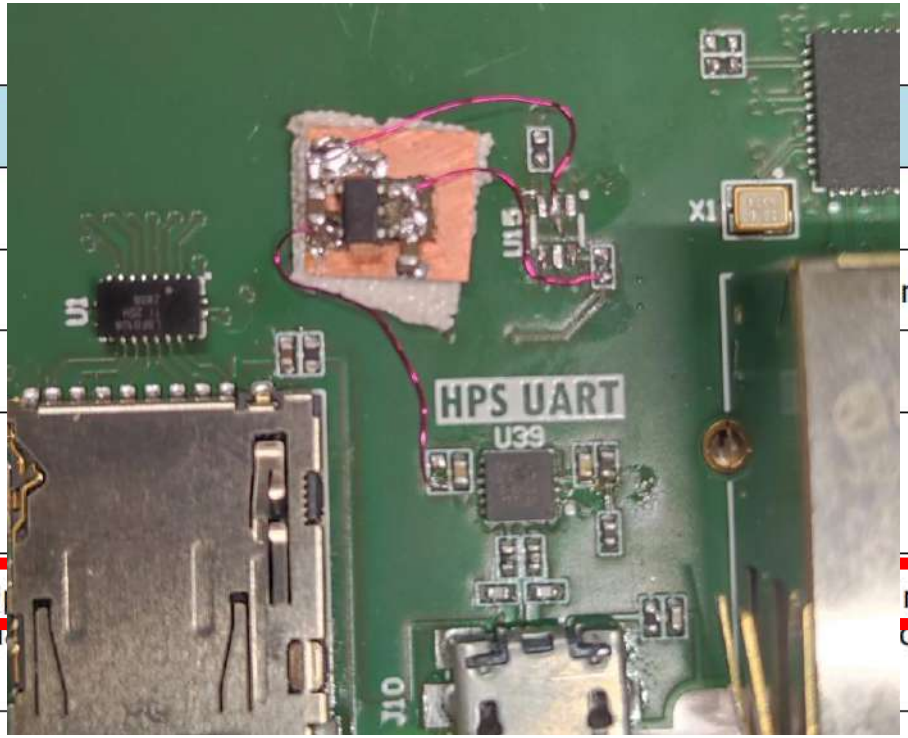

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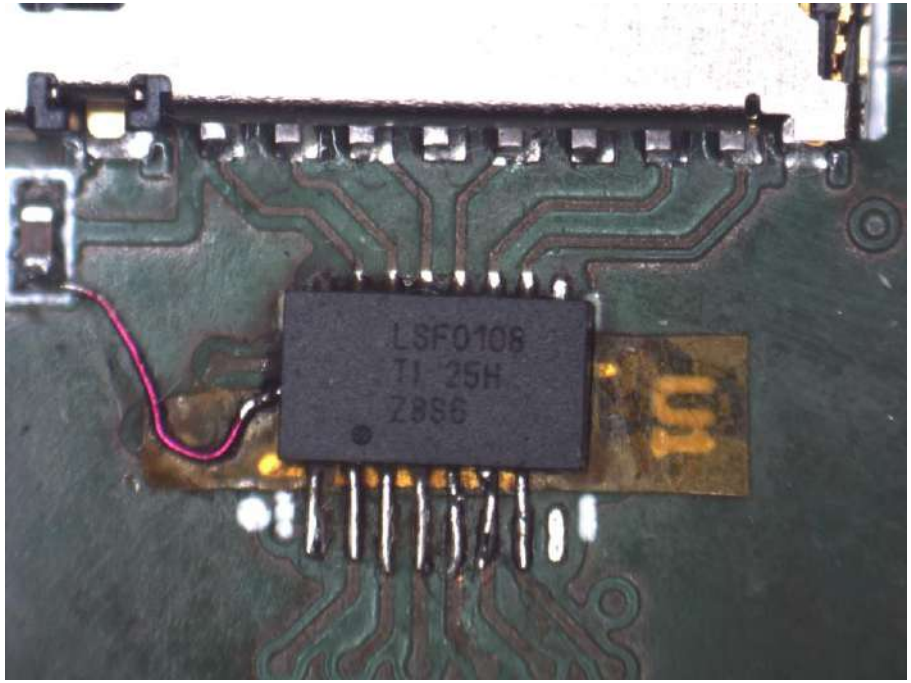
Examples – PCB issues

- **Wrong footprint** – devices with same name have different footprints (different manufacturers)



Examples – PCB issues

- **Wrong footprint** – devices with same name have different footprints (different manufacturers)

Nexperia **74AVC8T245**

8-bit dual supply translating transceiver with configurable voltage translation; 3-state

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC8T245PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74AVC8T245BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1
74AVC8T245BZ	-40 °C to +125 °C	DHXQFN24	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 24 terminals; 0.4 mm pitch; body 2 mm × 4 mm × 0.48 mm	SOT8024-1

TEXAS INSTRUMENTS

SN74AVC8T245 8-Bit Dual-Supply Bu

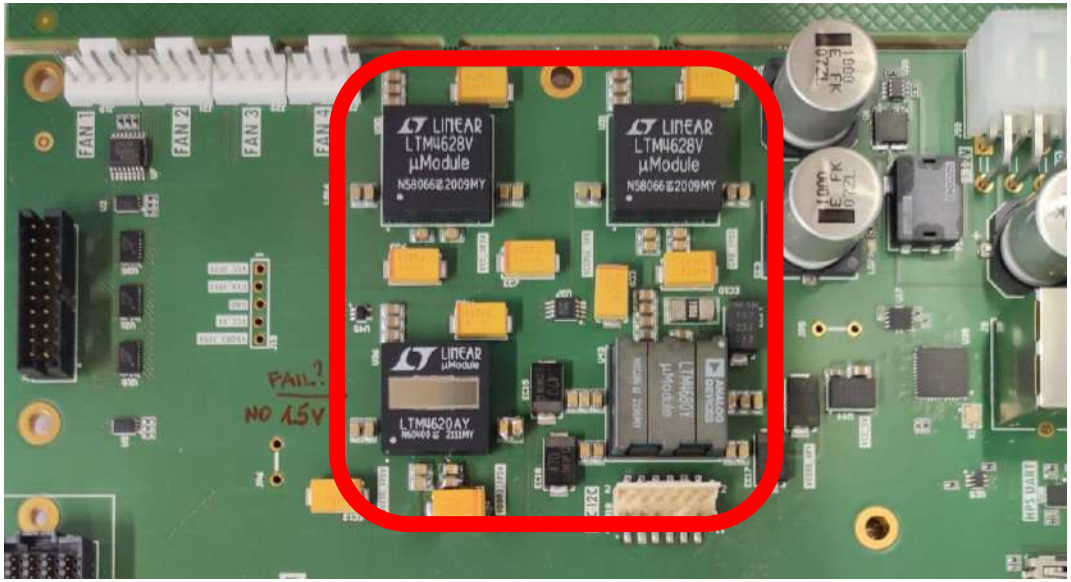
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC8T245	VQFN (24)	3.50 mm x 5.50 mm
	TSSOP (24)	4.40 mm x 7.80 mm
	TVSOP (24)	4.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Examples – Manufacturing issues

- **Power regulator DOA on one board**
- Humidity problem – dedicated application note
- https://www.analog.com/media/en/technical-documentation/product-information/assembly-considerations-for-umodule-bga-lga-package.pdf



Power supply section

Examples – Manufacturing issues

BGA & LGA Moisture Sensitivity, Bake, Pack, & Ship

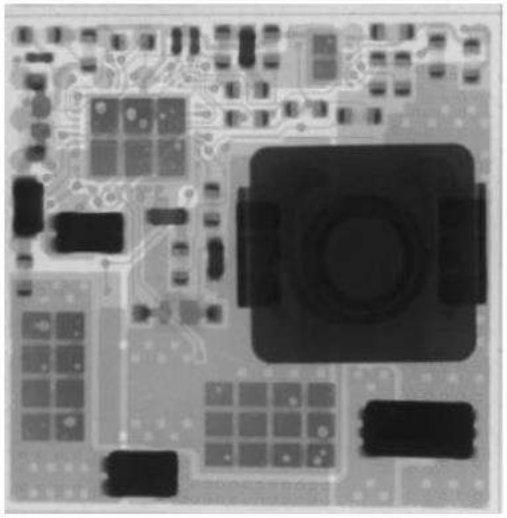
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

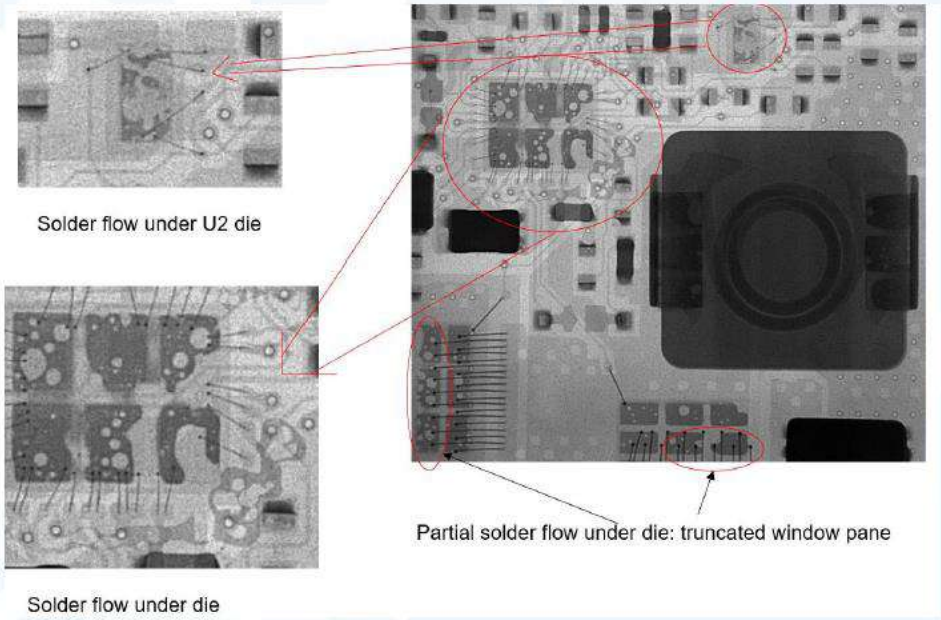
- µModule® products meet MSL 3 or 4 of the IPC/JEDEC specification J-STD-020
  - Floor life (time outside moisture barrier bag) must be tracked
  - Floor life for MSL 3 = 168 hours
  - Floor life for MSL 4 = 72 hours
- ADI ships all µModule® devices in bake-able trays with desiccant and moisture level indicator inside vacuum sealed moisture barrier bag
- Check the packing integrity (may need to check the source of shipment for repack procedures) if parts received in partial trays (other than from ADI)
- If moisture indicator shows pink color, or punctured seal of the bag is observed, bake the packages at 125°C for 48 hours minimum
- Follow J-STD-033 "Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices

Examples – Manufacturing issues

Example of good and bad μModule® Device after PCB assembly and rework

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™





NO SHORTS
- Part met MSL floor life
- Reflow peak temperature within the spec
- Part was baked prior to removal

SOLDER SHORTS INSIDE MODULE
- Part exceeded MSL floor life – delamination
- Reflow peak temperature out of spec – solder melted & spread
- Part was not baked prior to removal

Conclusions

- Designing a complex board from scratch is quite challenging
- Prototypes are needed for confirming design and repeatability (100 units to be produced)
- Partnership with an experienced manufacturer is useful in particular for production phase

- **Next steps:**
  - Produce first digital board pre-series of 10 units
  - Arrange for FATs and prepare documentation for testing and first powerup/programming (operations to be done at the manufacturer's site)
  - Have a complete system (FE, new digital unit) running in Elettra storage ring

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Thank you!

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