INSTRUMENTATION
TECHNOLOGIES

LIBERA

Overview of Libera Platforms and technologies

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Outline

- **Platform A** – single box solution - discontinued
- **Platform B** – modular solution based on MTCA.0
- **Platform C** – SoC based solution for less demanding applications (FPGA resources)
- **Platform C1** – SoC based solutions for more demanding applications (FPGA resources)
- **Temperature stabilized platform**
- **Amplifier 110** - hadron preamplifier
- **MTCA.4 platform** - dual BPM module on uRTM
- **Pilot Tone Front End** - industrialization with ELETTRA
- **Component discontinuation & product improvement** handling
- **Future** possibilities

Platform A

Single box solution: Electron, Brilliance, Bunch-by-Bunch, Hadron

Technologies: SDR in FPGA, electronics drift compensation with switching, DSC, direct RF sampling, Muti gigabit transceivers for FOFB, Single board computer, RS-485

Platform A is discontinued since end of 2012 due to Intel CPU and Xilinx FPGA unavailability. Produced for 9 years. Delivered >2000 units. 11 years after discontinuation we still offer support and service for this platform.

Platform B

Configurability: LLRF, Brilliance+, Hadron, Single pass H, Single pass E
Scalability: from 4 channels up to 36 channels
Modularity: different modules can be combined together
Technologies: MTCA (IPMI), COM express, PCI express, Muti gigabit transceivers for FOFB, Dedicated inter-module low latency links, optical event receiving, RS-485, 10GbE coming soon

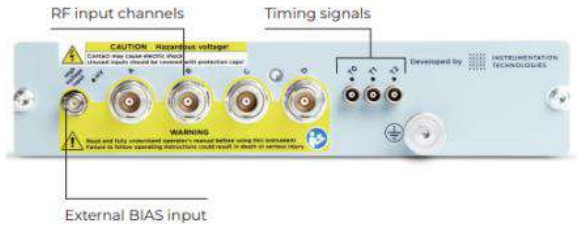
Platform C/C1

Based on Xilinx ZYNQ-7000:

- Less powerful FPGA version for SPARK, BLM, Photon, Current meter
- More powerful FPGA version for DIGIT500, CavityBPM

Challenges:

- Passive cooled platform,
- low maintenance,
- complete configuration on a single microSD card,
- Isolated front end for photon instrument
- JESD 204B,
- SFP data streaming,
- PoE, PoE+



Temperature stabilized platform

Libera SYNC – RF reference transfer system over fibber developed with PSI (very low added jitter ~5 fs @ 3 GHz)

Libera RMO distribution amplifier

Libera temperature stabilized LLRF front end

Challenges:

- Thermal insulation and temperature stability control +/-0.01K
- Power/heat dissipation
- Know how about fibber optics

Amplifier 110

Quad 4 channel amplifier for hadron machines with monitoring output

Initially developed with/for GSI in the frame of the FAIR project

Capable of handling high voltage pulses from 230 Vp down to 1 mVp

Environment with radiation -> Simple control -> no uC

Challenges:

- high voltage pulses (230 Vpeak)
- low noise
- Relatively high BW (55 MHz)
- Fast range switching time
- 110 dB gain range

MTCA.4

Dual BPM on uRTM

Initially developed for DESY Petra IV
Tested with commercially available DAMC FMC2ZUP.
Application optimized board is being developed at DESY MTCA Technology Lab.

Challenges:
Introducing high speed ADCs on uRTM.
Serial LVDS communication as limited number of pins is available.
HW/SW PLL for locking sampling clock to machine clock.
Power budget limited by standard (max 30W)
Remote crossbar switch introduced as a separate module – Libera XBS FE
Radiation resistance improvements

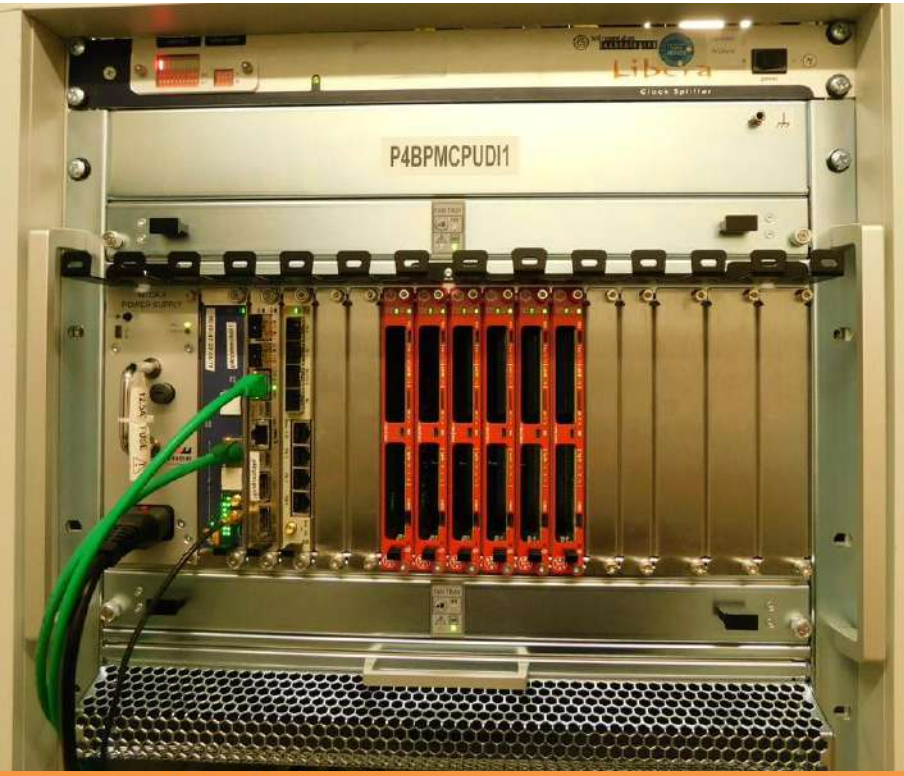
MTCA.4

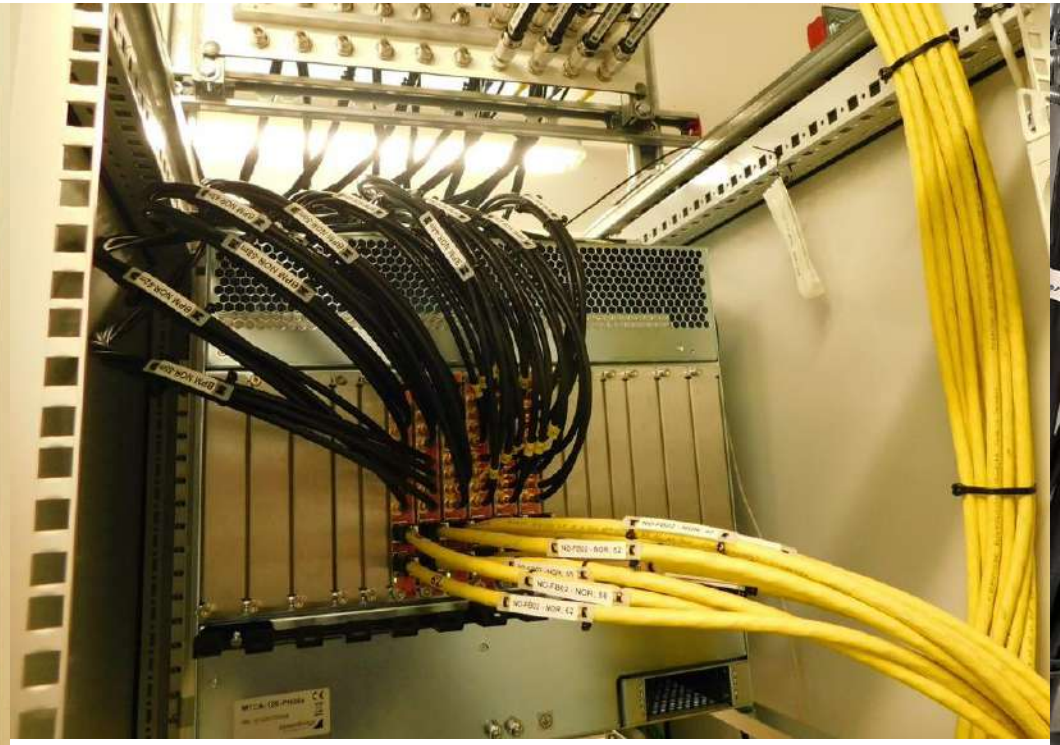
Fully populated crate – 12 BPMs, timing module and CPU

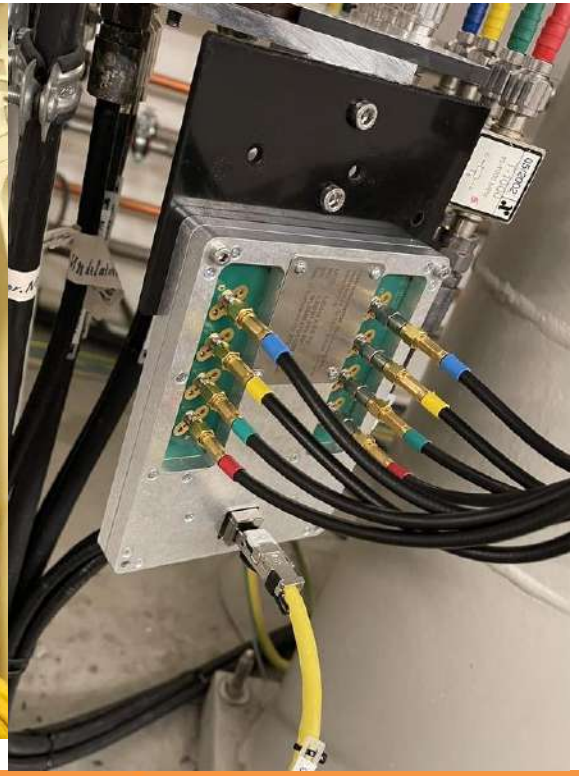
Prototype delivered to DESY – Petra III

From beginning some FW issues discovered but successfully resolved together with Desy

High density of cables.







photos courtesy of Gero Kube - DESY

Pilot Tone Front End

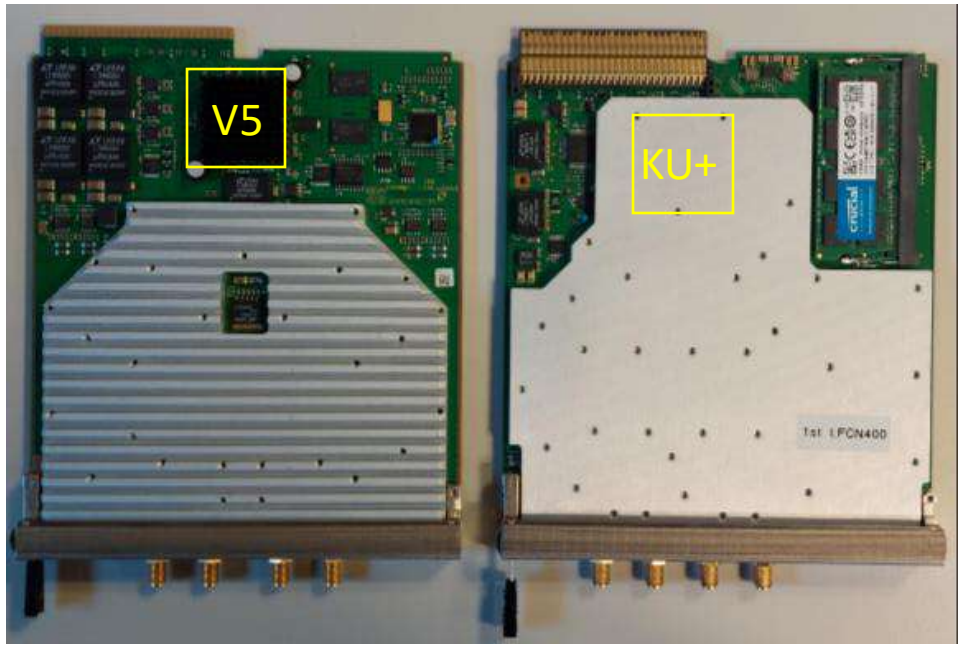
Prototype developed by ELETTRA and improved & industrialized together with Instrumentation technologies.

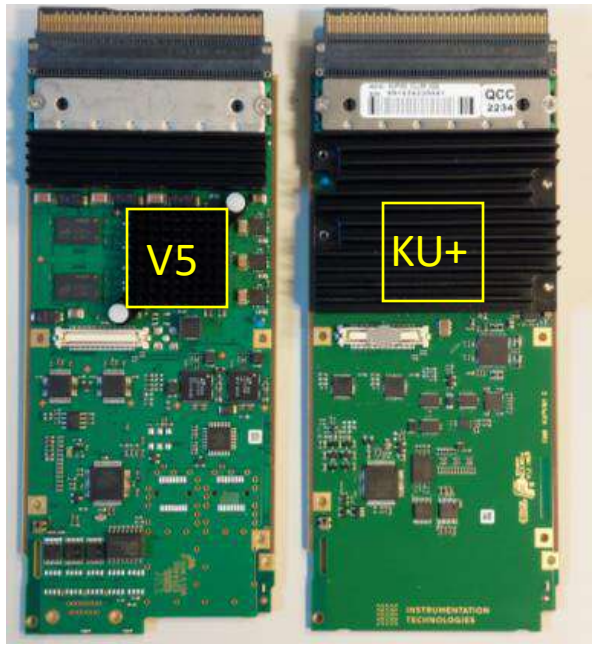
Tunnel mounted, no maintenance unit. PoE for remote power cycling.

Obsolescence and technology update 1/2

Addressing component obsolescence and following latest technologies (lowering the power, increasing the performance)

RAF (BPM module) → KUPRAF, KUPRAF2 (Virtex5 → Kintex Ultra Scale +, SODIMM)
VM1 (vector modulator module) → KUPVM (Virtex5 → Kintex Ultra Scale +)



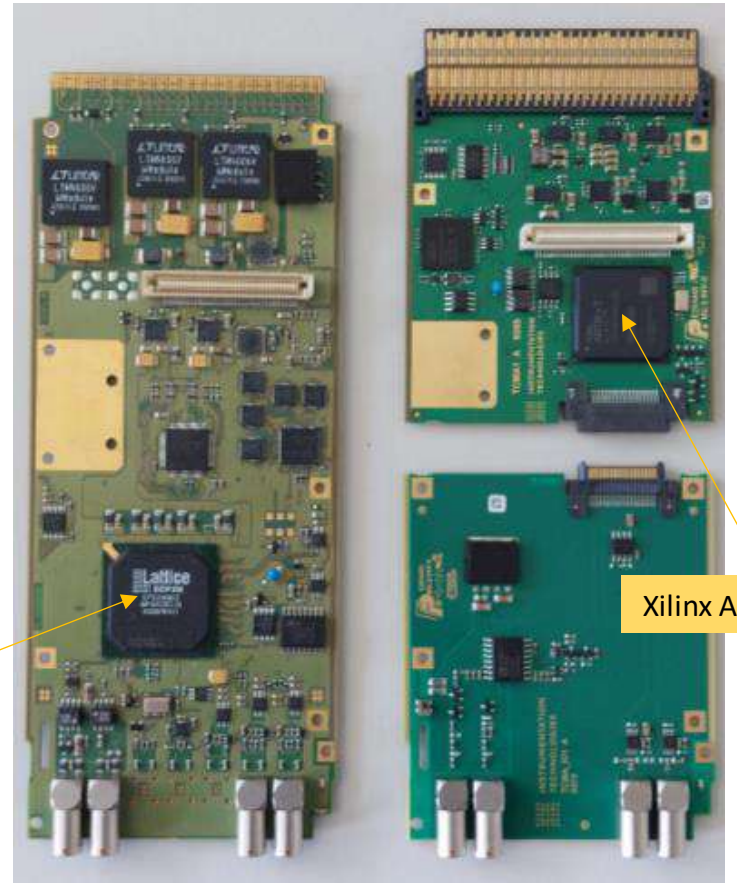


Obsolescence and technology update 2/2

TCM1 (timing module) → TCMA (Lattice → Artix7 + modular IO)

ADC9 (LLRF probe acquisition) → KADC8 (Virtex5 → Kintex Ultra Scale +, new ADCs)

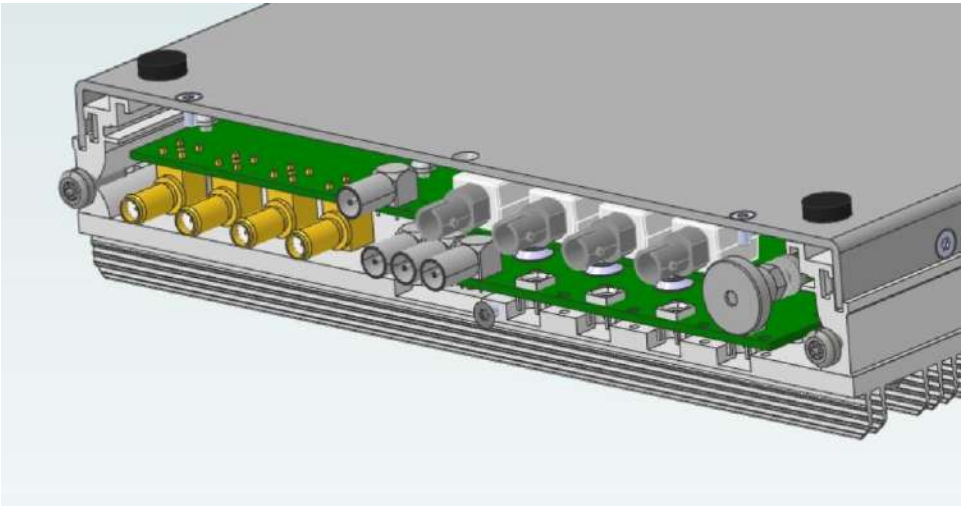
ICB1 (Platform B carrier hub with COMe) → ICB2 (10GEth, PCIe Gen3)



Future possibilities 1/2

Testing Libera XBS FE with Libera Spark – develop the interface (new DAI module) and DSC for Spark

Integration of the RF downconverter inside the Libera Spark for electron LINACs (feasibility)



Future possibilities 2/2

RF SoC

Gen 1 has been evaluated.

High power, high cost

KRIA SoM

Being evaluated.

High performance.

Attractive delivery times and price.

Artificial Inteligence

No activity so far.

Lots of ideas coming from institutes.

Want to be HW ready to support these initiatives.