TEST AND MEASUREMENTS RESULTS OF THE PILOT TONE FRONT END INDUSTRIALIZATION FOR ELETTRA 2.0

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Abstract

Elettra 2.0 will be the low-emittance upgrade of the present machine, a third-generation lightsource based in Trieste, Italy. The new machine, foreseen to be completed in 2025-2026, will be equipped with 168 beam position readout systems divided into 12 cells. The BPM electronics will be based on the prototypes developed by the laboratory, relying on the pilot-tone compensation technique for assuring the required resolution and long-term stability. The industrialization and production of the BPM electronics system are being carried out in partnership with Instrumentation Technologies, a company that has experience with BPM readout systems within the accelerator field. This paper will present the results of the industrialization of one of BPM system's key component: the Pilot Tone Front End, focusing on its improvements introduced on electronic and mechanical sides, giving not only a significant performance gain with respect to the previous prototype but also improving robustness and reliability. An overview of the testing procedures that will assure the performance repeatability of the series will also be provided.

INTRODUCTION

In previous conferences we already presented the overall development of the new electron beam position monitoring system for Elettra 2.0, the low-emittance upgrade of the Italian synchrotron, from the early pilot tone proof of concept [1] to the integration of the complete prototype system in Elettra's global orbit feedback [2]. The partnership signed with Instrumentation Technologies has accelerated the process towards the final industrialized system, foreseen to be installed in 168 locations of the new machine in 2025-2026. In particular, thanks to the modular approach, we firstly focused on the improvement of the pilot tone front end (PTFE) [3] before moving to the digital acquisition unit. In this paper we present the industrialization results of the former, a mature product ready to be produced in series.

MECHANICAL AND ELECTRONIC IMPROVEMENTS

In [3] we listed the foreseen improvements, such as the possibility of changing the bandpass filter, the extra gain stage, the single board design, the integrated power over ethernet feature. After implementing them, further modifications have been made for increasing reliability and performance.



Figure 1: Pilot Tone Front end.

Shielding and heat management: a large-area aluminium heatsink has been applied over the PCB, with mounting holes for future installation on girders: this allows for an homogeneous heat distribution and adequate dissipation (Figure 1). The heatsink serves also as an EMI shield, covering all the RF traces. In addition, another aluminium block completely covers the filters section, reducing external temperature influence.

Amplifiers matching: input and output matching of RF amplifiers that are inside the front end was improved, in order to reduce as much as possible signal reflections and standing waves, with a trade-off between topology of matching circuit, number and value of its components and performance and repeatability of the design. Still, the obtained gain with respect to the original prototype is significant: S_{11} parameter went from -14 dB to -31 dB and S_{22} parameter from -14 dB to -26 dB, measured at 500 MHz.

Ethernet controller: the Ethernet to UART communication chip has been changed from Lantronix to Wiznet, due to PoE compatibility of the latter. The new design is about ten times cheaper, with benefits in term of lower EMI, lower generated heat and power consumption.

Pilot tone generation: accuracy and phase noise of the internal pilot tone generator have been improved: the former has been increased with carefully tuning of crystal's load capacitors, the latter reduced with a new implementation of PLL's loop filter. In addition, the user can choose an external source for supplying the pilot signal.

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Power management: the power tree has completely rearranged. Now the overall load is evenly distributed among the voltage regulators, and their dropout voltage has been lowered in order to reduce the dissipated power.

PERFORMANCE RESULTS

A dedicated setup in two climatic chambers has been prepared to evaluate the effectiveness of the compensation on cables (Figure 2): all the active devices (generator, PTFE and readout electronics) were held at constant temperature and humidity, while a temperature profile was applied in the chamber containing only one cable (LMR-195, 20 metres). It has to be noted that this is a worst case scenario, since in real environments the temperature variation will affect all the four cables more or less in the same way, reducing the produced drift on the calculated position. Three temperature profiles have been applied, a step from 25 to 15 °C, a slow ramp from 15 to 35 °C and another step from 35 to 25 °C.

Results are quite the same for the various profiles, and are shown in Table 1, where the previous PTFE prototype has been compared with the new industrialized version. A reduction of about 4 times of the temperature dependence on the compensated position has been obtained, proving benefits from the improvements made.

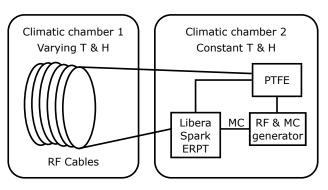


Figure 2: Climatic chamber setup.

Table 1: Compensation effectiveness

	X/T (non comp.) [μm/K]	XC/T (comp.) [µm/K]					
	25 °C-15 °C step						
Prototype	-8.2	-3.7					
PTFE	-6.5	0.9					
	15 °C-35 °C ramp						
Prototype	-7.8	-3.65					
PTFE	-6.3	1.0					
	35 °C-25 °C step						
Prototype	-7.9	-3.6					
PTFE	-6.2	1.0					

Tests at Elettra

In addition to measurements performed in controlled environment, tests have been made also in a real scenario, where temperature and humidity can change.

So, we put the PTFE in Elettra service area: its outputs were connected with high-quality short cables to an in-house developed digitizer already presented in [4]: the processing chain is described in [5]. Position calculation is expressed in nanometers, with a scale factor of 20 mm, and an equivalent bandwidth of 10 Hz. As a source, we used the signal coming from a single Elettra storage ring pickup splitted in four, in order to emulate a stable beam.

Figure 3 shows the results of a long-term measurement in a 12-hour time window. Machine was running at 2 GeV, with 310 mA of current (top-up mode) and a standard multibunch filling pattern (80 %). Digitizer was locked to machine clock and RF frequency was 499.654 MHz.

Standard deviation on calculated positions were 32 nm for the horizontal plane and 51 nm for the vertical plane. In both planes, position remained within ± 150 nm peak-to-peak.

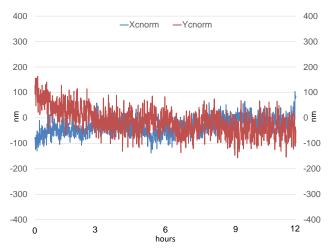


Figure 3: Long-term measurement with short cables in a 12-hour window.

Subsequently, we decided to change connection cables from PTFE to digitizer with longer ones (LMR-195, 20 metres), in order to simulate a common situation in beam diagnostics (PTFE in machine tunnel and digitizer in service area). The source was changed to an RF generator that emulates the beam with the same filling pattern, due to scheduled maintenance of the accelerator. The time window was extended to 24 hours. Results are reported in Figure 4.

Standard deviation on calculated positions increased to 62 nm for the horizontal plane and 120 nm for the vertical plane. In both planes, position remained within $\pm 300 \text{ nm}$ peak-to-peak. Performance worsening is due to cable losses and to temperature and humidity variation during the measurement (Figure 5).

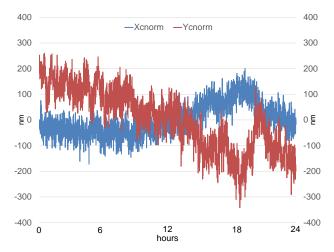


Figure 4: Long-term measurement with long cables in a 24-hour window.

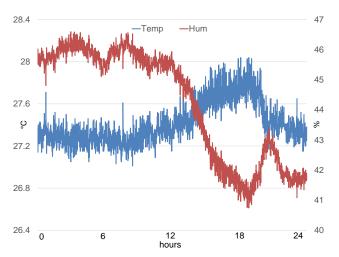


Figure 5: Temperature and humidity variation during 24-hour long-term measurement.

FAT PROCEDURE

Rigorous testing is performed to ensure similar and withinspec operation of all mass-produced units. With every new product rolling off the production line, it is important to set up effective factory acceptance tests (FAT) early in the product's lifespan. Here lies another balancing act of specifying pass-fails early enough to automate the process but also to specify them on enough samples, so that they are effective in detecting defects and don't detect many false positives (test sensitivity and specificity). FATs are also a good opportunity to collect additional statistics about the system while lengthening the whole FAT for only a couple of percent. This can be used later to define better pass-fails or better understand the system. FATs are divided in three categories:

Checking Basic Functionalities

With visual inspection we confirm that all visible components are at their designated place and the lack of physical

damage to the unit indicates that it went through a correct assembly process. Status LEDs are toggled to confirm that all visual interfaces are in good working condition.

Next, a connection to the PTFE is established over telnet to check power supply voltages and currents and compare them to pre-defined pass-fails. Normal working temperature is also checked after initial warmup. Optic latch is visually checked for light pulses when changing attenuators.

RF Signal Chain

Every component along the RF signal chain is included in at least one test case, to ensure correct operation. Testing setup is presented in Figure 6 and 7. A R&S SMB100A signal generator is used for the RF signal and to provide the reference clock to the AWG, spectrum analyzer and indirectly also the machine clock for a Libera Spark ERPT, used as readout electronics.

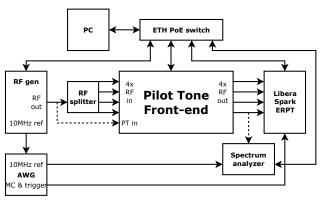


Figure 6: Test setup diagram.

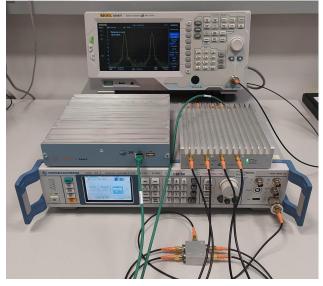


Figure 7: FAT testbench.

With the spectrum analyzer we determine the accuracy of the pilot tone frequency and amplitude and the RF signal amplitude on PTFE inputs and outputs. The latter ensures same power levels regardless of the cables used. The internal pilot tone generator is checked to verify that the PLL remains locked with various frequency settings and that it outputs a signal with consistent power. A frequency sweep is performed on both band-pass filters on all four channels.

For the following tests, an internal Libera Spark ERPT is used to evaluate the compensation effectiveness and to quickly assess all four signal paths of the PTFE. We measure signal-to-noise of each channel with following signal combinations: only RF signal present, only PT from internal generator, only PT from external generator and both RF and PT combined. Signal-to-Noise ratio is defined as $20\log_{10}(\mu/\sigma)$ of 10k samples of fast 10 kHz data. All measurements are done for multiple different attenuator settings on the PTFE. RF generator output is varied so that we have a constant power on the Libera Spark and measure just the properties of the PTFE. With this we also check that all attenuators and amplifiers (three gain stages in total) are in working order. Short example measurement results in Figure 8.

Crosstalk is measured between all channel combinations and a minimum of 50dB isolation is guaranteed.

RF generator + Internal PT						Signal-to-Noise				
Power [dBm]	pt_att [dB]	att_1 [dB]	att_2 [dB]	att_3 [dB]	max adc	A [dB]	B [dB]	C [dB]	D [dB]	Limit [dB]
-20	0	0	20	30	5461	84,0	84,1	83,9	84,0	80
-25	5	0	15	30	5464	83,8	84,0	83,9	83,8	80
-30	10	0	10	30	5504	82,3	82,5	82,3	82,4	80

Figure 8: FAT result example.

Long-term Measurements

The above-mentioned tests are performed on every unit, and since they are all automated, they take less than half an hour to be performed. To balance rigor and effectiveness, one unit out of 10 is tested for a longer period (typically 14 hours), to re-verify long-term behaviour and to root out any systematic defects. Either from components being from different batches, or some other unpredictable factor. In this case, the instrument is left on in the test setup over night with both RF and internal PT signals present and compensated data at 10 Hz rate is logged. A slow and monotonous

temperature change is expected overnight and from that the temperature coefficient of position is calculated, with the pass-fail set to $4 \mu m/K$ in both directions.

CONCLUSION

The industrialization phase of the Pilot Tone Front End has been concluded: several improvements increased its overall quality, both in terms of performance and reliability. A dedicated quality control procedure has been developed in order to assure that all produced units will satisfy the requirements.

However, the worldwide shortage of electronic components remain a critical issue, currently faced with continuous monitoring of delivery dates and availability, weekly meetings to keep the parties informed and constant iterations to find acceptable solutions (e.g. equivalent parts from different suppliers, wise PCB design for mounting different alternatives, etc).

REFERENCES

- [1] G. Brajnik, S. Bassanese, S. Carrato, G. Cautero, and R. De Monte, "A Novel Electron-BPM Front End With Sub-Micron Resolution Based on Pilot-Tone Compensation: Test Results With Beam", in *Proc. IBIC'16*), Barcelona, Spain, Sep. 2016, pp. 308–311, doi:10.18429/JACOW-IBIC2016-TUPG02
- [2] G. Brajnik, S. Bassanese, G. Cautero, S. Cleva, and R. De Monte, "Integration of a Pilot-Tone Based BPM System Within the Global Orbit Feedback Environment of Elettra", in *Proc. IBIC'18*, Shanghai, China, Sep. 2018, pp. 190–195. doi:10. 18429/JACOW-IBIC2018-TUOC01
- [3] G. Brajnik, M. Cargnelutti, R. De Monte, P. Leban, P. Paglovec, and B. Repič, "Current Status of Elettra 2.0 eBPM System", in *Proc. IBIC'21*, Pohang, Rep. of Korea, May 2021, pp. 71–74. doi:10.18429/JACOW-IBIC2021-MOPP16
- [4] G. Brajnik, S. Cleva, R. De Monte, and D. Giuressi, "A Common Diagnostic Platform for Elettra 2.0 and FERMI", in *Proc. IBIC'19*, Malmö, Sweden, Sep. 2019, pp. 280–282. doi:10.18429/JACOW-IBIC2019-TUPP003
- [5] M. Colja, S. Carrato, G. Brajnik and R. De Monte, "Design and Implementation of an FPGA-Based Digital Processor for BPM Applications", presented at IBIC'22, Krakow, Poland, September 2022, paper MOP14, this conference.