The RF BPM Electronics Concept and Developments for the PETRA IV project at DESY

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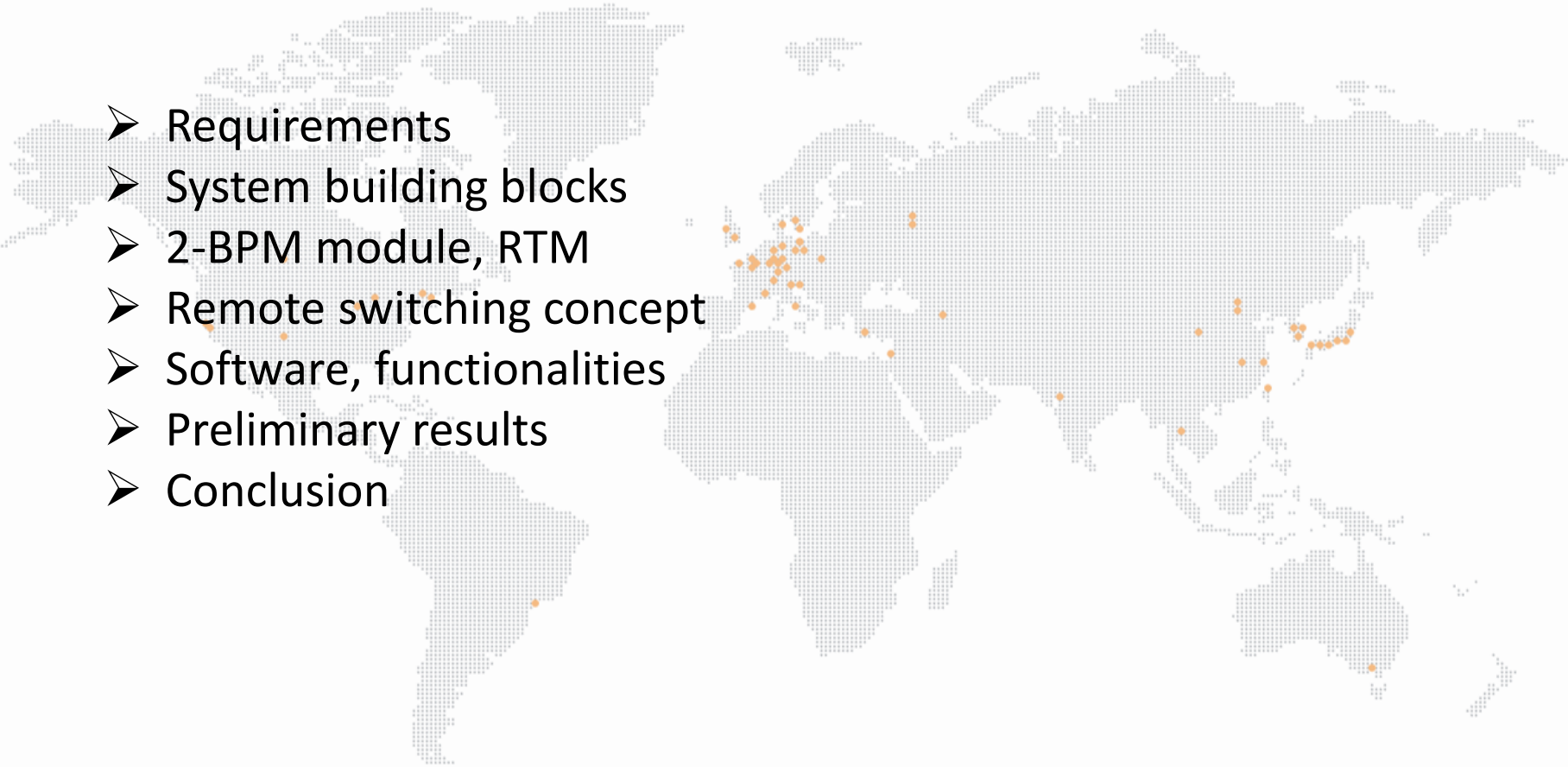
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- ➢ Requirements
- ➢ System building blocks
- ➢ 2-BPM module, RTM
- ➢ Remote switching concept
- ➢ Software, functionalities
- ➢ Preliminary results
- ➢ Conclusion

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Requirements

BPM system for DESY PETRA-4 project

- High channel density per station: about 800 BPMs in total spread over 47 racks / 89 MTCA crates
- MicroTCA.4 platform
- Measurement performance (k=10 mm)
  - <10 µm RMS single bunch single turn (0.5 mA)
  - <0.1 µm RMS closed orbit, 200 mA in 1600 bunches in bandwidth DC to 1 kHz
  - ±2 µm beam current dependence in 60 dBm range, centered beam
  - < 1 µm position stability over 6 days at ±1°C temperature stability
  - BPM system must support operation modes from a single bunch to 80 – 1600 bunches in various spacing conditions
- Real-time turn-by-turn data streaming for the FOFB: required latency up to 3 turns

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System building blocks
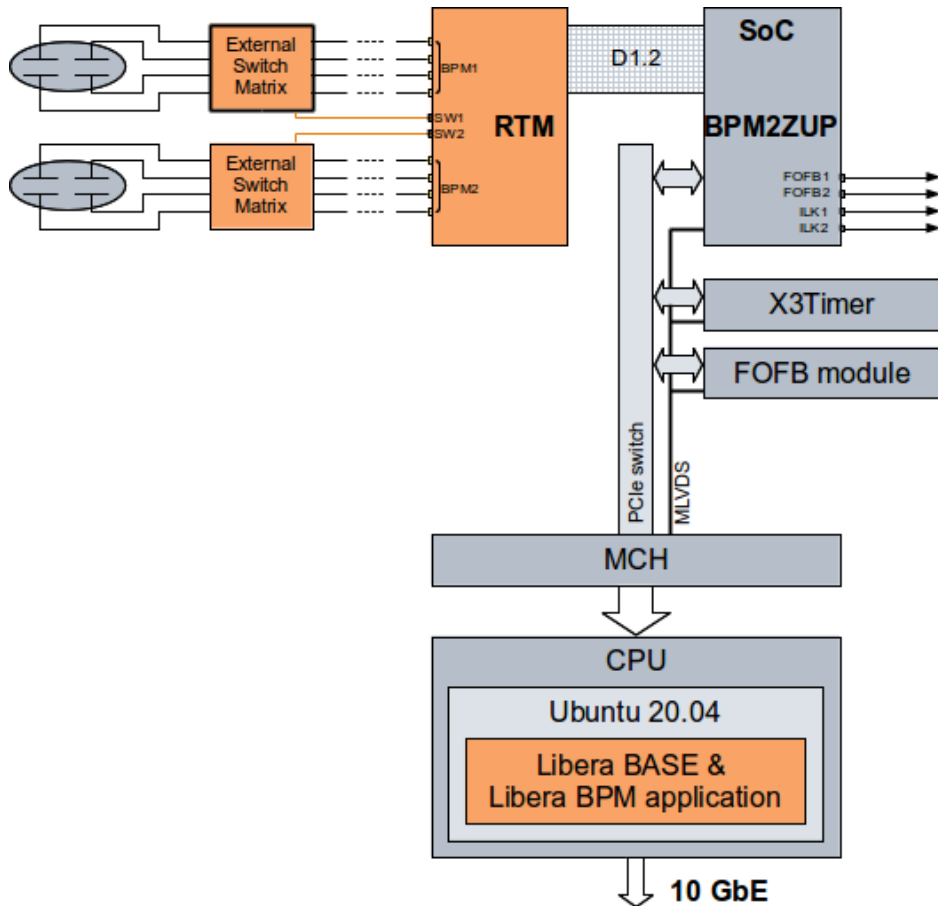
- MicroTCA crate, 12 slots

- MCH module

- CPU module

- X3 Timer module   ← provided by DESY Techlab

- (FOFB module)   ← provided by DESY Techlab

- 8-channel RTM   ← provided by I-Tech

- Connection RTM → AMC is using D1.2 standard

- FMC2ZUP module   ← provided by CAENels (for this project)

- BPM2ZUP module   ← will be provided by DESY Techlab later

- External switch matrix   ← provided by I-Tech

"2-BPM" module
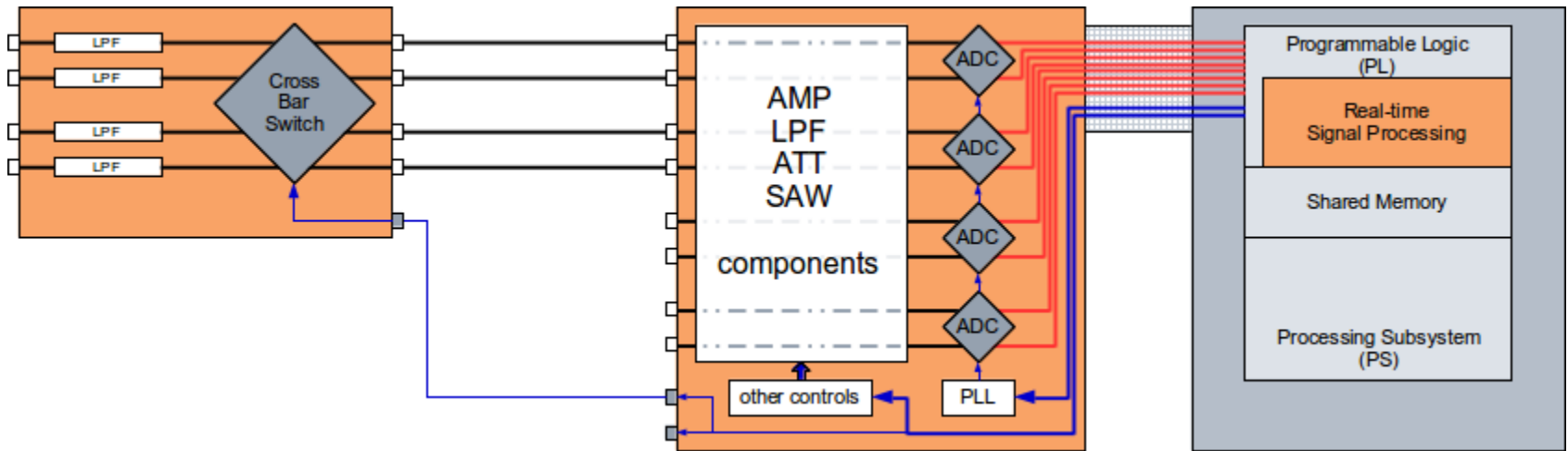
External Switch Matrix
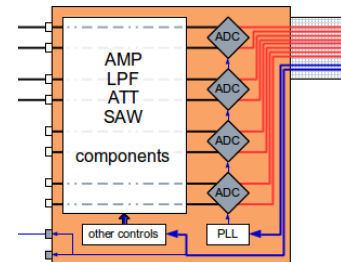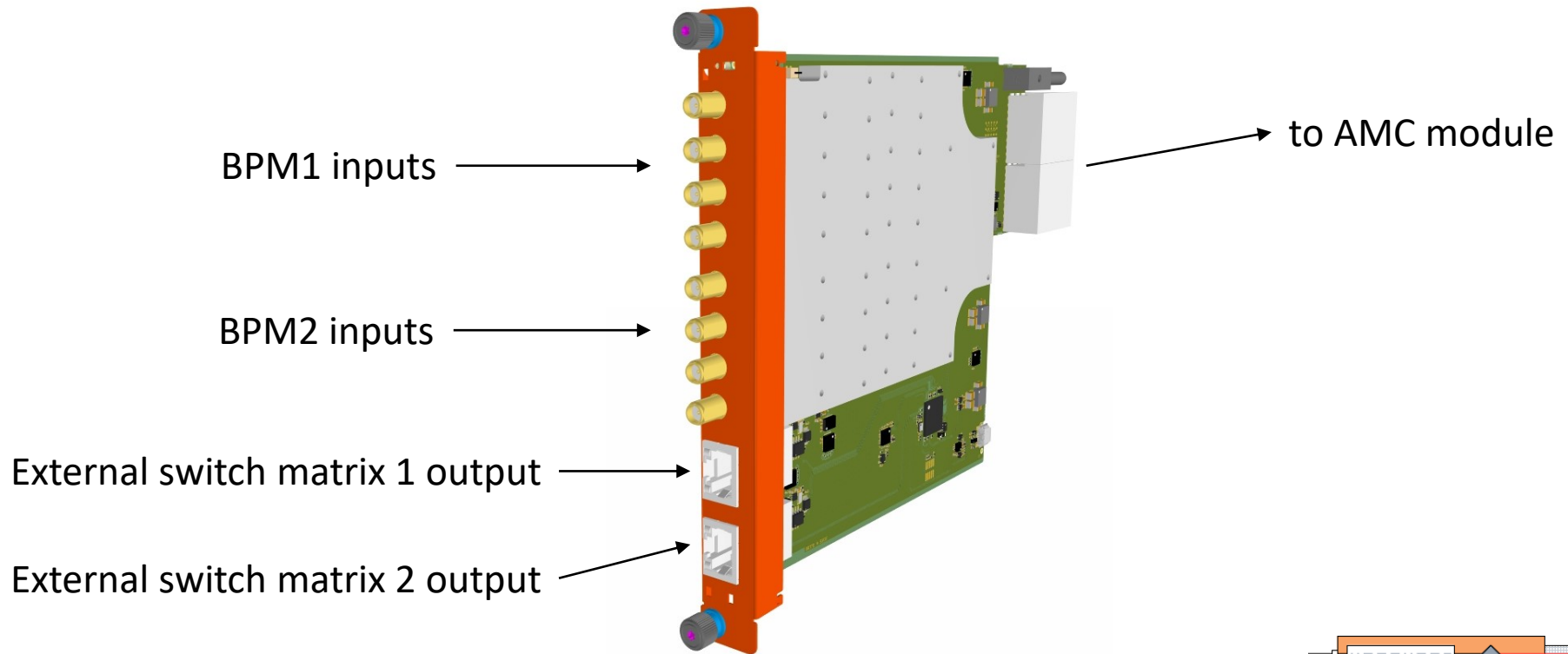- Low pass filters
- Attenuation
- Cross-bar switch

RTM
- Low pass filters
- Programmable Attenuation
- Band-pass (SAW) filters
- 4x 2-channel A/D converters (125 MHz)
- Local PLL (software controlled)
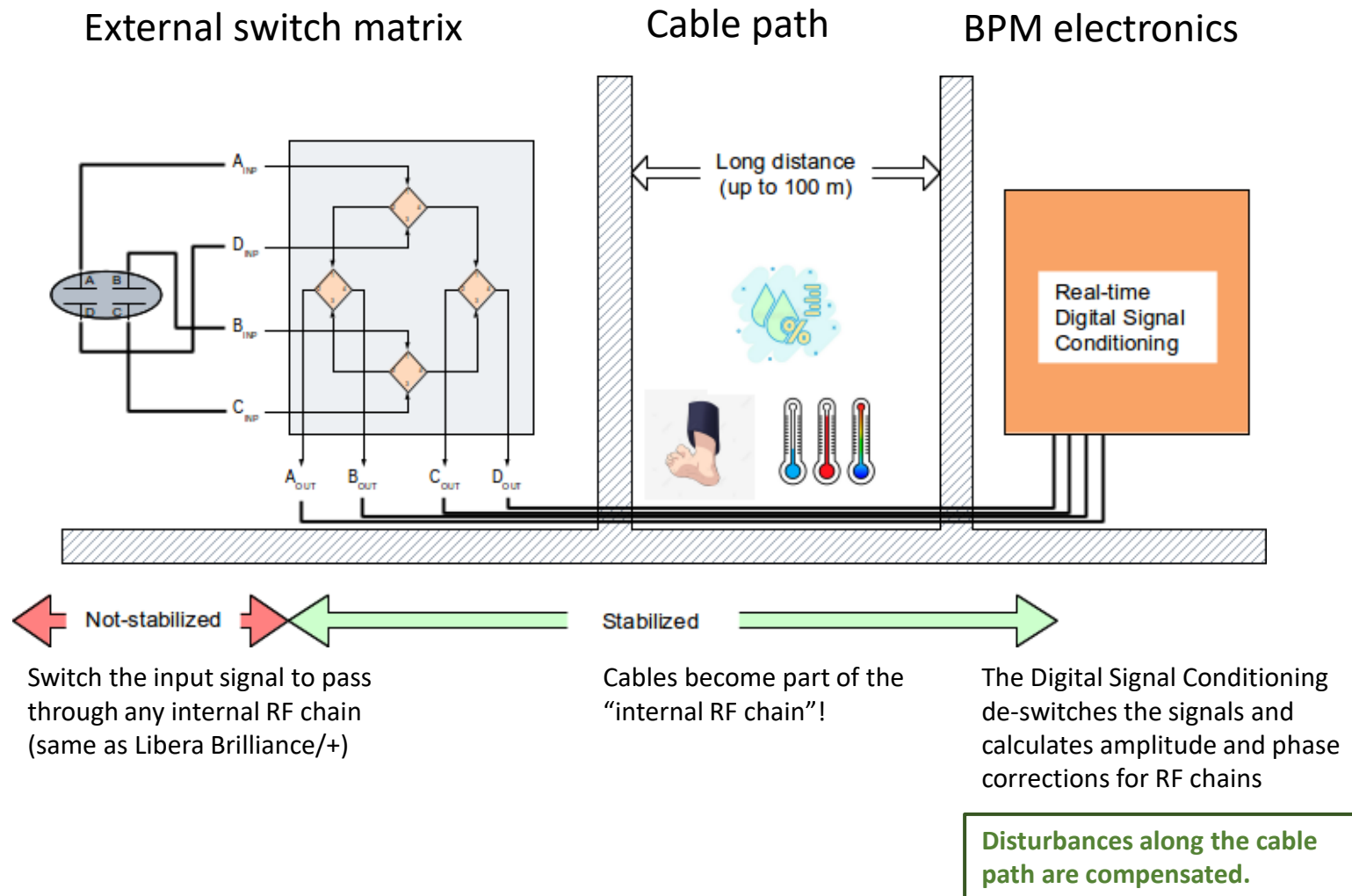- Clock signal to External Switch Matrix

BPM2ZUP module
- Zynq device ZU7EG-1
- 5 GB DDR4 memory
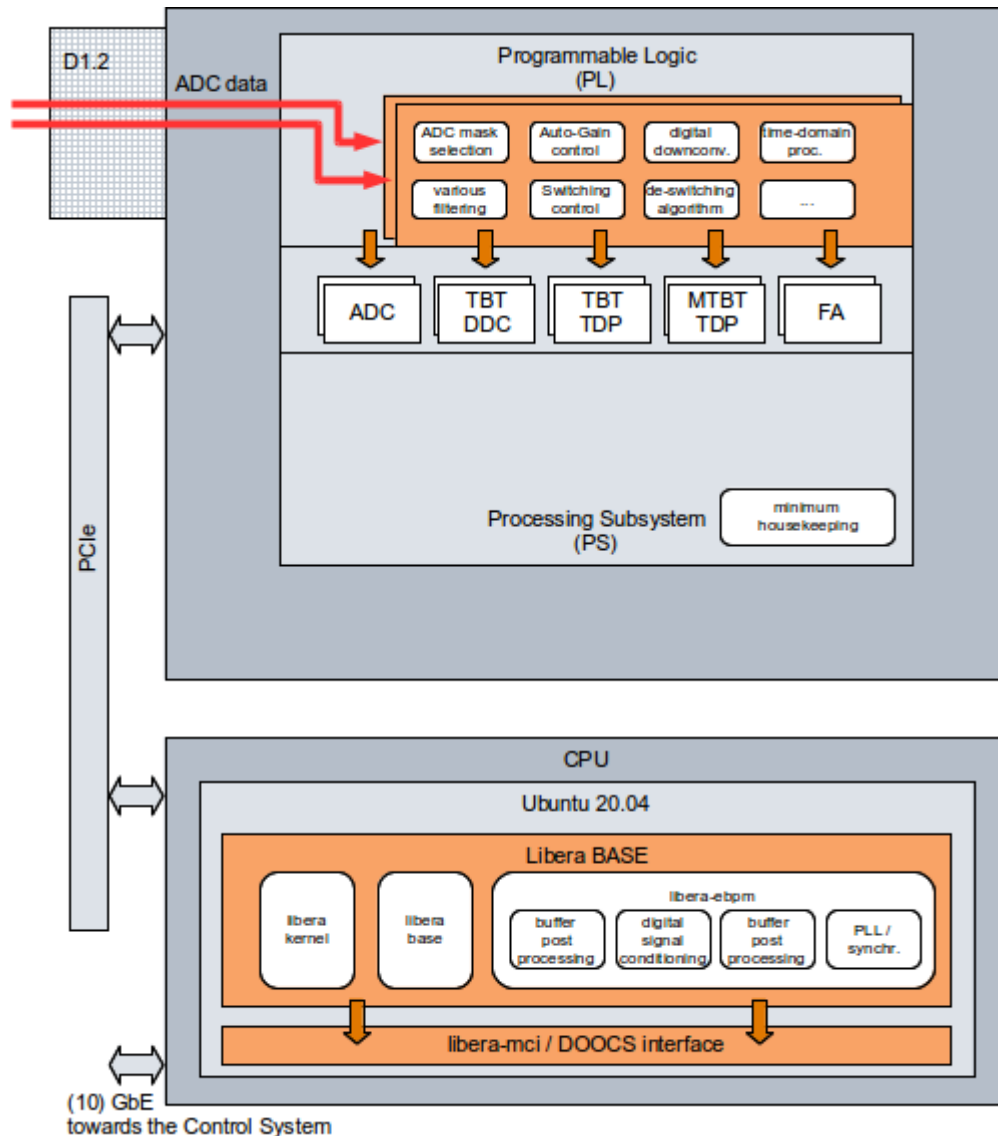- PCIe to the MicroTCA Carrier Hub
- Minimal housekeeping done in the PS

RTM

BPM1 inputs

BPM2 inputs

External switch matrix 1 output

External switch matrix 2 output

to AMC module

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Remote switching concept

External switch matrix   **Cable path**   **BPM electronics**

Not-stabilized ← → **Stabilized** →

Switch the input signal to pass through any internal RF chain (same as Libera Brilliance/+)

Cables become part of the "internal RF chain"!

The Digital Signal Conditioning de-switches the signals and calculates amplitude and phase corrections for RF chains

Disturbances along the cable path are compensated.

Software, functionalities

FPGA
- Turn-by-turn processing
- Digital filtering
- External switch control
- De-switching algorithm
- Data management (circular buffers, streams)
- **… for 2 BPMs!**

CPU
- Libera BASE software infrastructure
- Data readout from multiple 2-BPM modules over PCIe
- Digital Signal Conditioning (for external switch matrix)
- Software PLL, synchronization
- Upper software layer
- Communication channel to the Control System
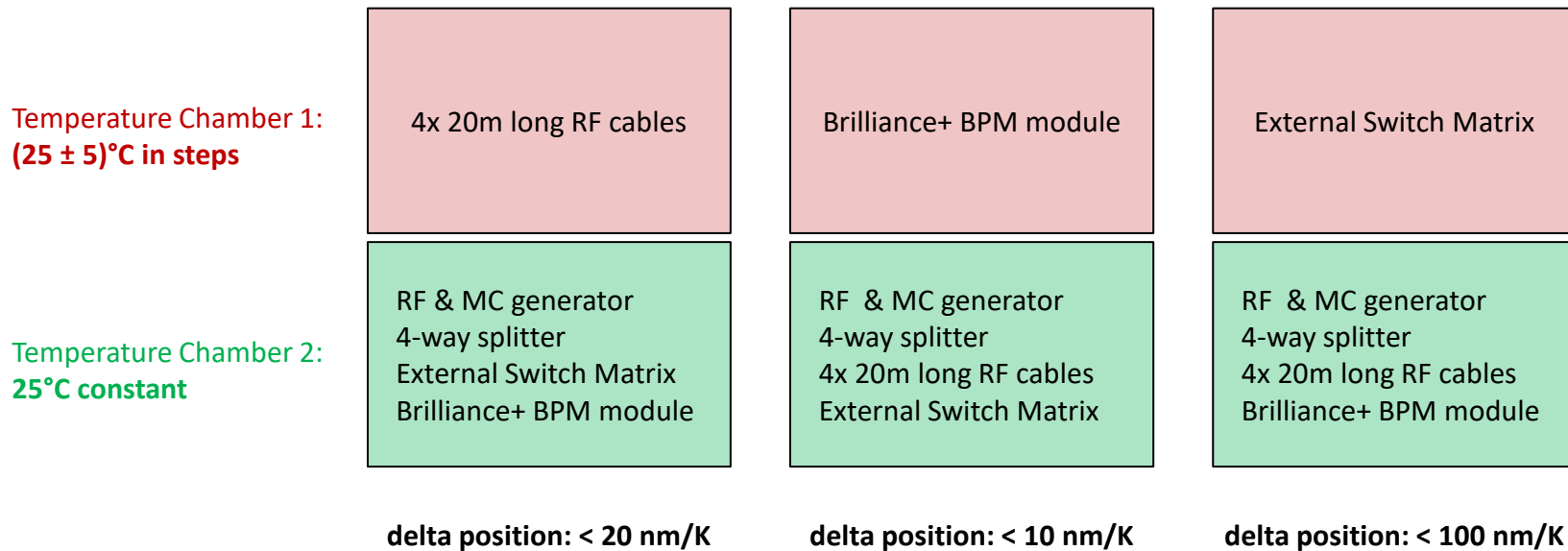
Software, functionalities
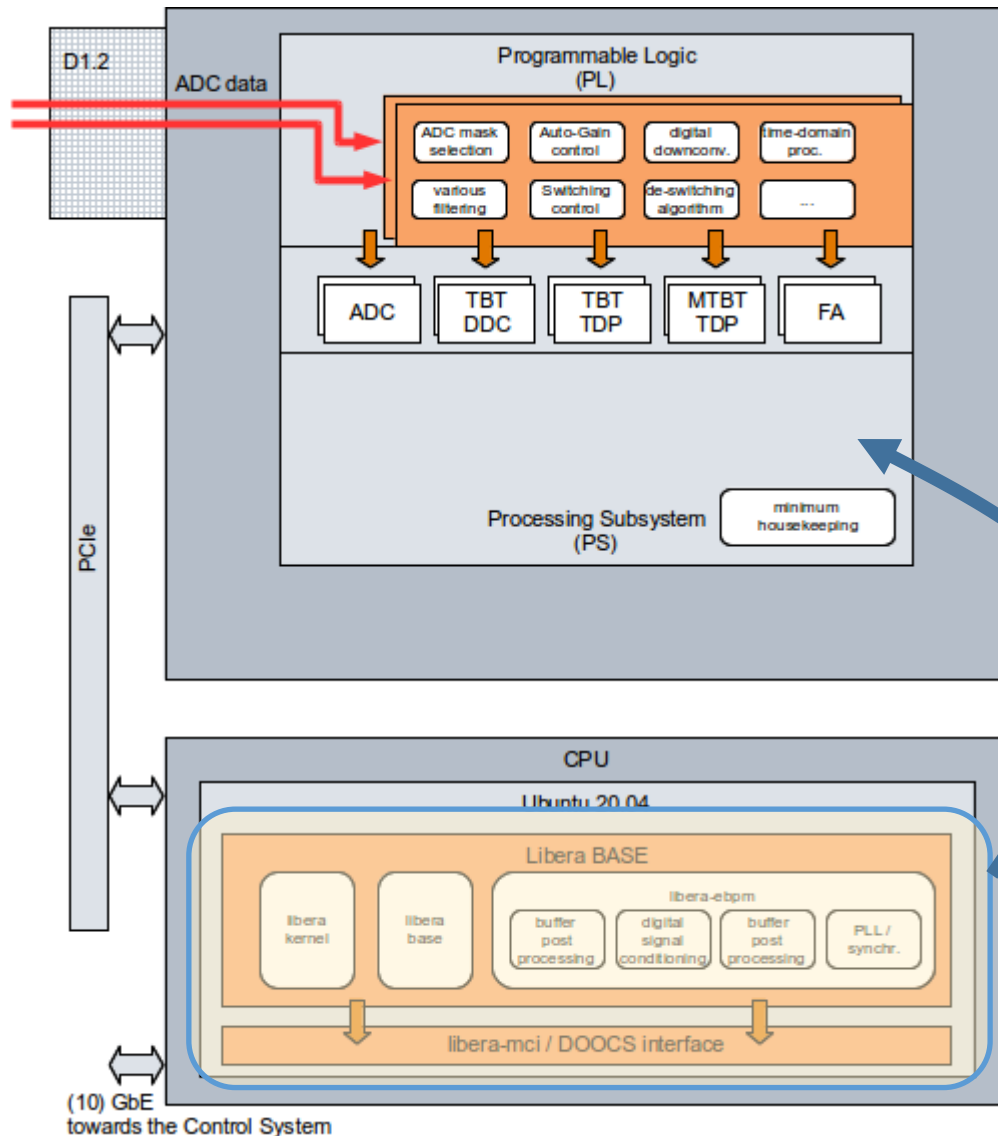
Could also run in the PS and communicate with the Control System over its GbE interface.

CPU module not needed in this case.

Preliminary test results

Longterm tests at Instrumentation Technologies

<u>Purpose of tests:</u> Verify the drift contribution of sub-systems

| Temperature Chamber 1: (25 ± 5)°C in steps	4x 20m long RF cables	Brilliance+ BPM module	External Switch Matrix
Temperature Chamber 2: 25°C constant	RF & MC generator 4-way splitter External Switch Matrix Brilliance+ BPM module	RF & MC generator 4-way splitter 4x 20m long RF cables External Switch Matrix	RF & MC generator 4-way splitter 4x 20m long RF cables Brilliance+ BPM module
	delta position: < 20 nm/K	**delta position: < 10 nm/K**	**delta position: < 100 nm/K**

Typical drift performance of a standard Libera Brilliance+ is < 200 nm/K

Tests done by L.Bogataj

Preliminary test results

Longterm tests at Petra-3

orbit data
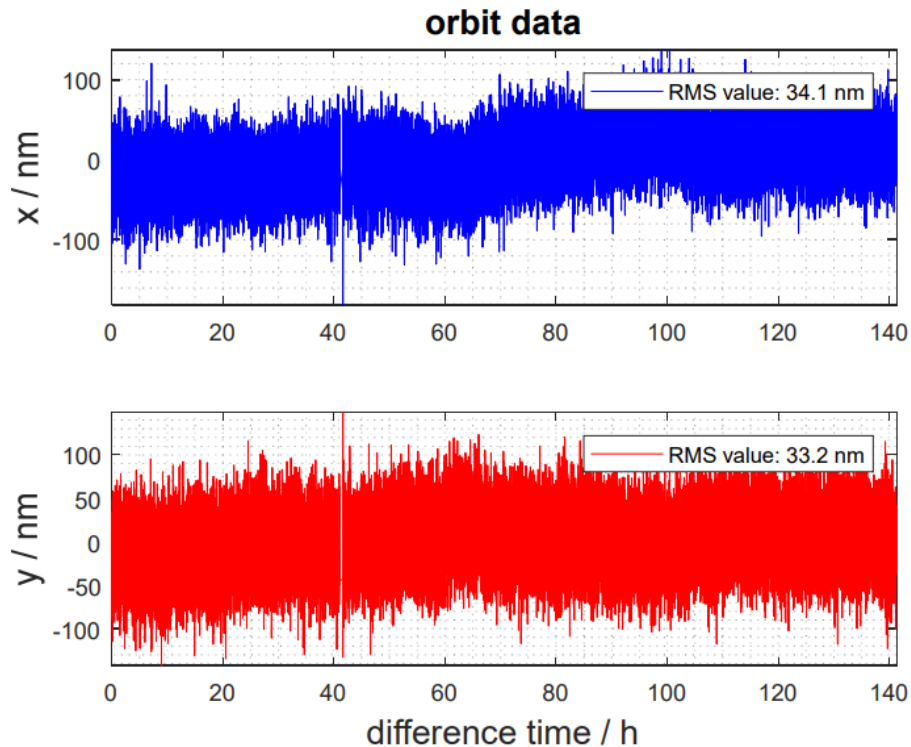
Tests done by
G.Kube

Beam conditions:
- 40 bunch-fill pattern
- 100 mA top-up

BPM system:
- Libera Brilliance+ (installed in a rack)
- External Switch Matrix (installed in the tunnel)

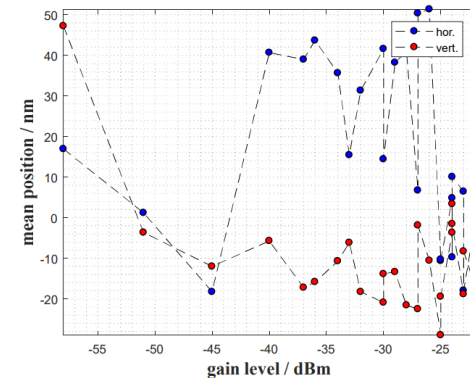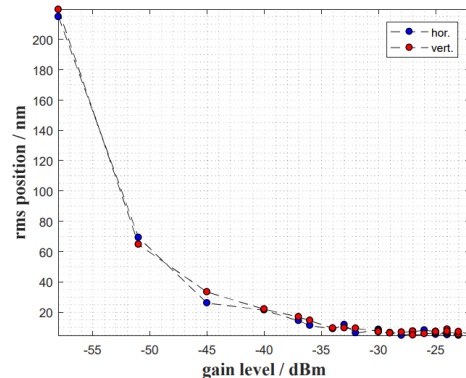INSTRUMENTATION TECHNOLOGIES

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Preliminary test results
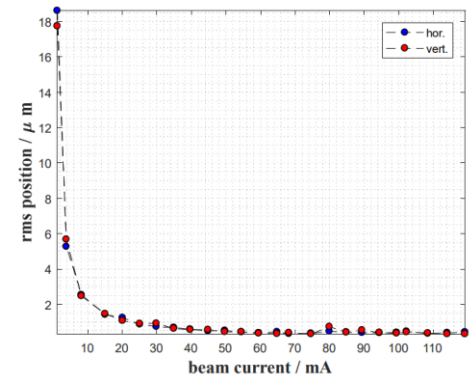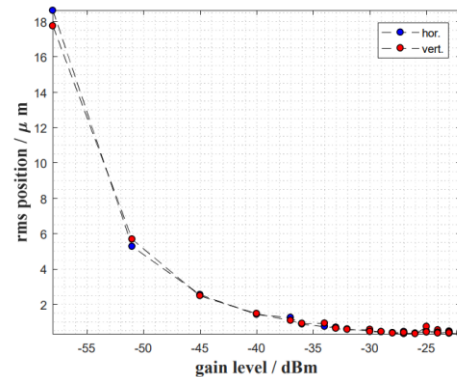
Other performance tests at Petra-3

Beam current dependence
- 120 mA / 480 bunch-fill pattern
- 10 S/s (DC to 4 Hz bandwidth)

Turn-by-turn RMS
- 120 mA / 480 bunch-fill pattern
- 130 kS/s (DC to 50 kHz bandwidth)

Tests done by G.Kube

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Conclusion

- Project running in full pace, prototype ready by end 2022

- Weekly meetings with DESY group

- Flexible scope of activities; things change along the project

  duration

Thank you for your attention

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