LIBERA WORKSHOP 2021

Libera DLLRF Development & Implementation at the APS Linac

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June 10th 2021

Argonne, IL USA

The APS Accelerator Complex

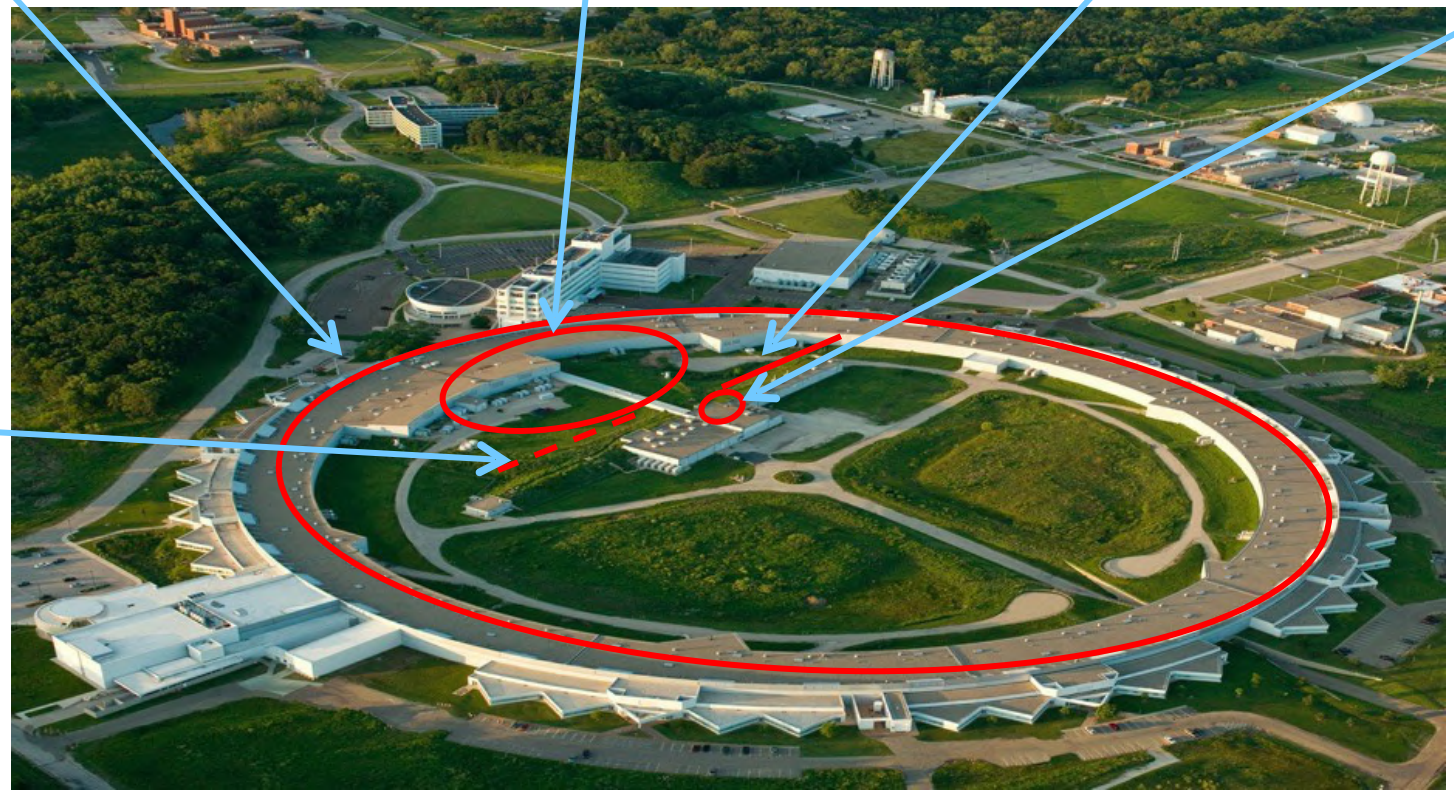
7 GeV, 100 mA, 46 ID, 21 bend magnet BL,

Booster: 0.375-7 GeV, 2 Hz

Linac: S-band, 375 MeV, 30 Hz

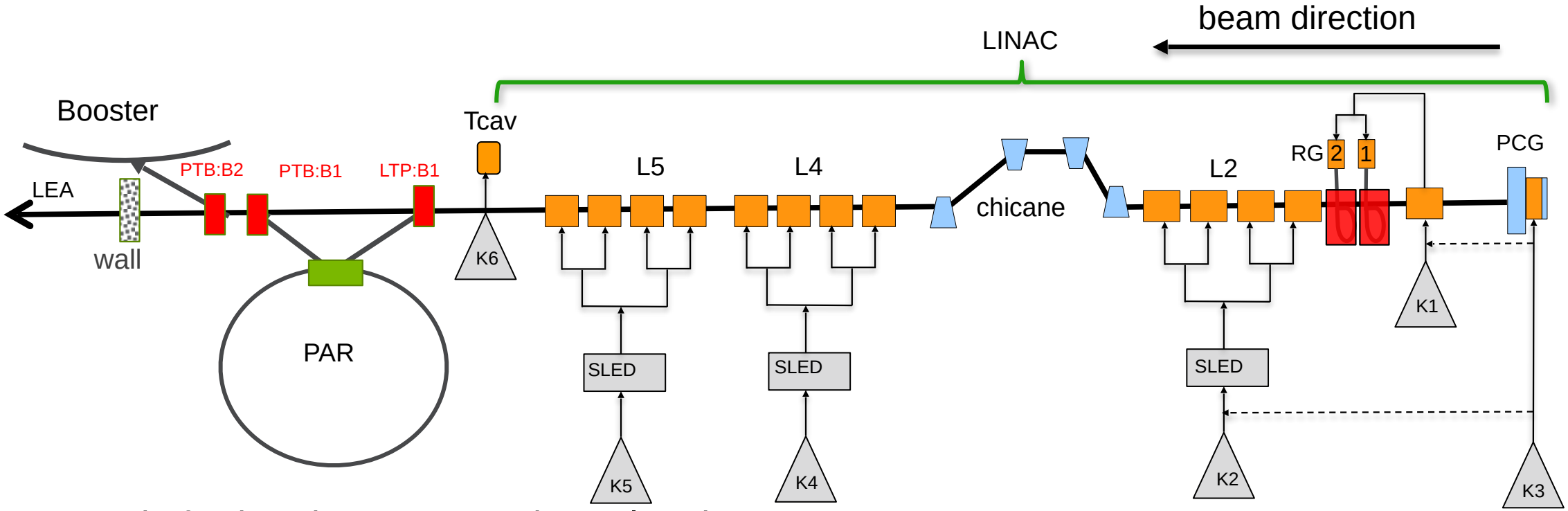
PAR: 375 MeV, 2 Hz, 1-4 nC

LEA



The APS Upgrade (APS-U) will replace the main storage ring but keep the radio-frequency (rf) system. Injector systems will be reused and require increased performance. LEA area is also being built for advanced beam experiment. Better diagnostics and instrumentation are critical for the success of the ongoing projects.

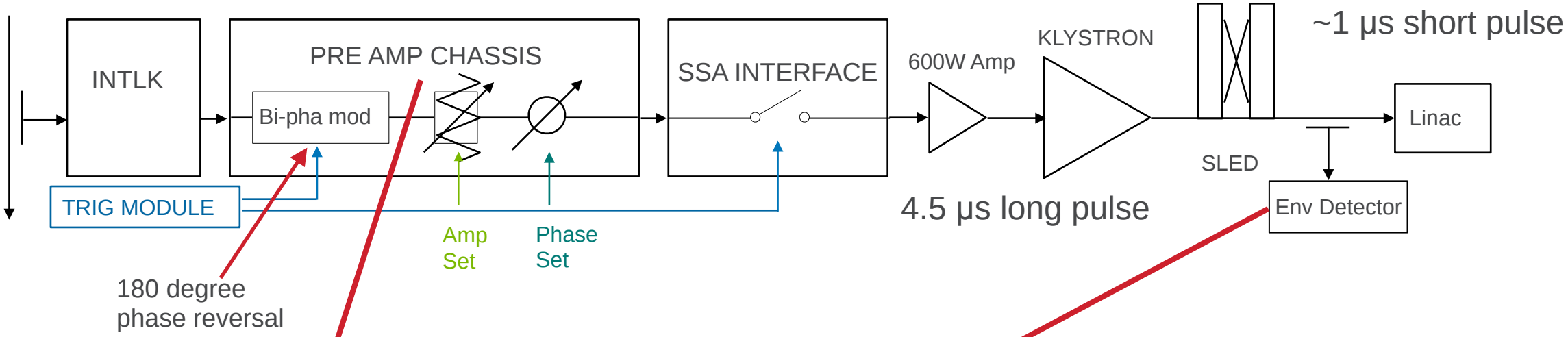
The APS Linac

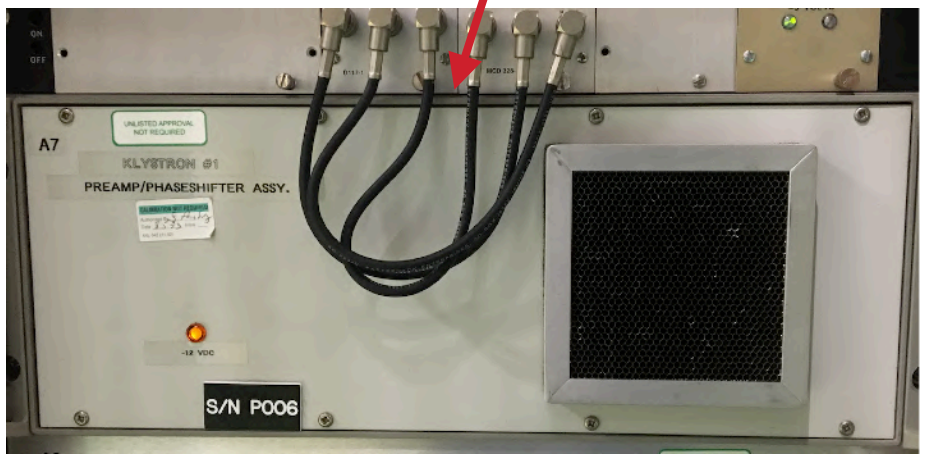


- Composed of S-band RF guns and accelerating structures;
- Two thermionic RF guns (RG1 and RG2), and a Photo-Cathode Gun (PCG):
  - RG2 provides electrons for injection into PAR/Booster/SR;
  - RG1 is a backup;
  - PCG beam for LEA.

- Thirteen 3-meter long accelerating structures
- Five klystrons for operation; three with SLED.
- Operate at 30 Hz
- Beam Energy is being upgraded from 375 MeV to 475 MeV

Existing Linac RF Controller & Monitor





- Many parts are getting obsolete
- Lack of resolved Amp/Pha waveform (Poor resolution)
- Lack of operation flexibility
- Lack of statistics

Considerations of the new Linac DLLRF system

- R&D resources is limited, commercial product is preferred
- Support the phase reversal capability and timing control
  - Need to set the phase reversal and pulse timing with ~10 ns resolution
- Easy to maintain
  - Share maintenance resources with the APS-U
- Time-resolved RF Amp/Pha diagnostics with latest technology
- MicroTCA based LLRF controller

What Libera LLRF can offer

- Libera LLRF controller developed for ELI-NP Linac
  - MicroTCA.0 standard ✅
  - Customized Amp/Phase Pulse shape ✅
  - Shared architecture & EPICS Base w APS-U BPM (Libera Brilliance+) ✅
  - High-resolution RF Amp/Pha Diagnostic ✅
  - Precise temperature stabilization. ✅
  - Virtex-5 FPGA ❌

APS LLRF System Development

- A demo test (Oct 2019) showed Libera LLRF system can generate and control the SLED phase reversal.

- However, a major upgrade is needed to meets the APS specifications
  - FPGA use the latest technology
  - More channels, need over 20 channels per stations
  - Change the Trig and INTLK connector
  - EPICS 7 support
  - SLED Tuning PVs
  - Phoebus GUI
  - Better timestamp
  - Post-mortem buffer for INTLK event
  - RF jitter statistics
  - Better RF calibration and control knobs

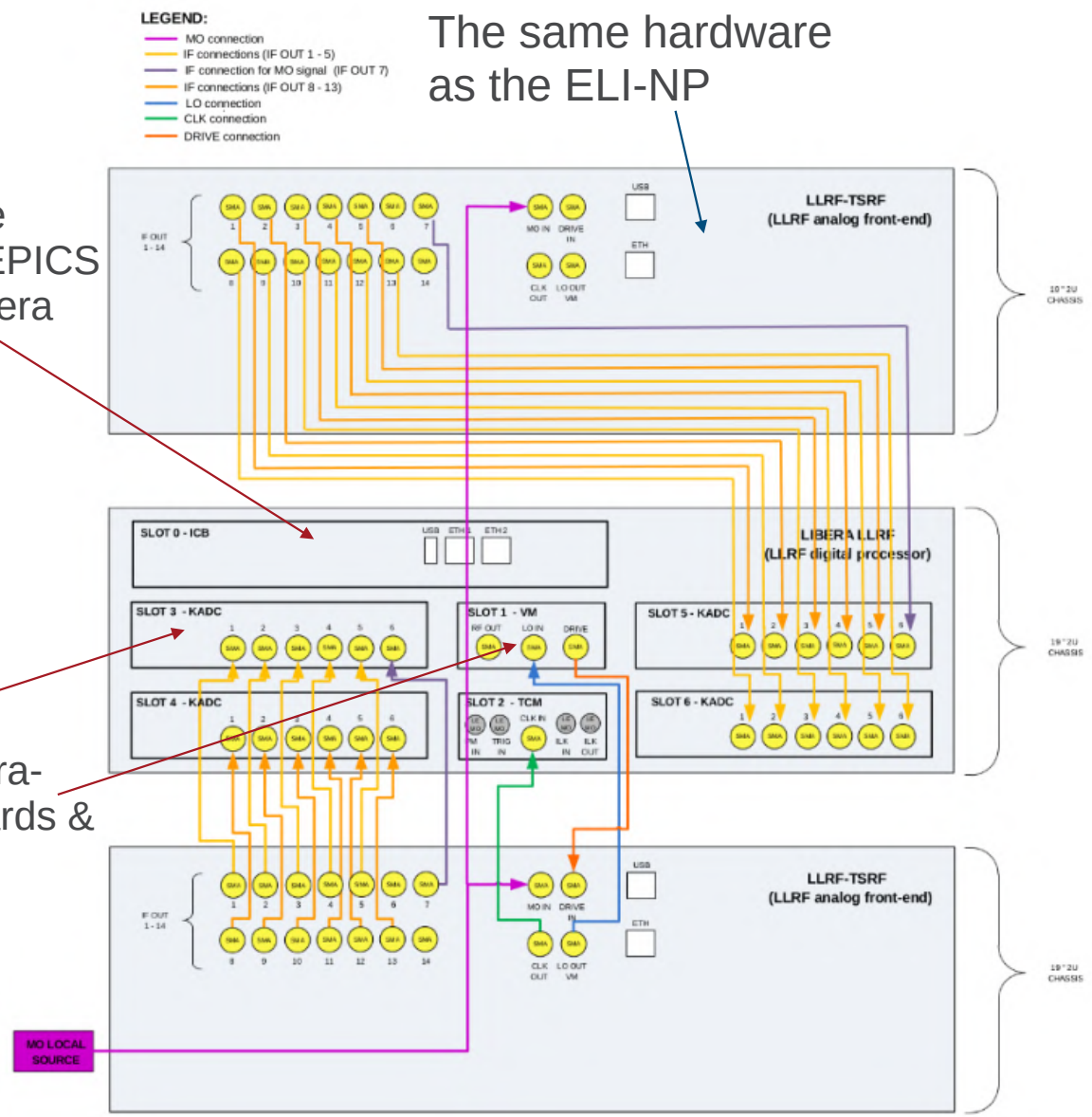
Libera LLRF Development for the APS Linac

• High power demo test at L6 w old system	Sep to Oct 2019
• New system revision specification	Nov 2019 to Feb 2020
• New system quotation and procurement	Awarded on mid-March 2020
• Monthly meeting with I-Tech development team	March 2020 to Nov 2020
• Hardware ready, start the system integration	Early Aug 2020
• System factory acceptance test	Oct 27th 2020
• System delivered to Argonne	Nov 6th 2020
• Start the acceptance test at L6	Nov 30th 2020

Libera LLRF Installed for Acceptance Testing

Share the same hardware and EPICS base as the Libera Brilliance+

New Kintex Ultra-scale ADC Boards & VM board



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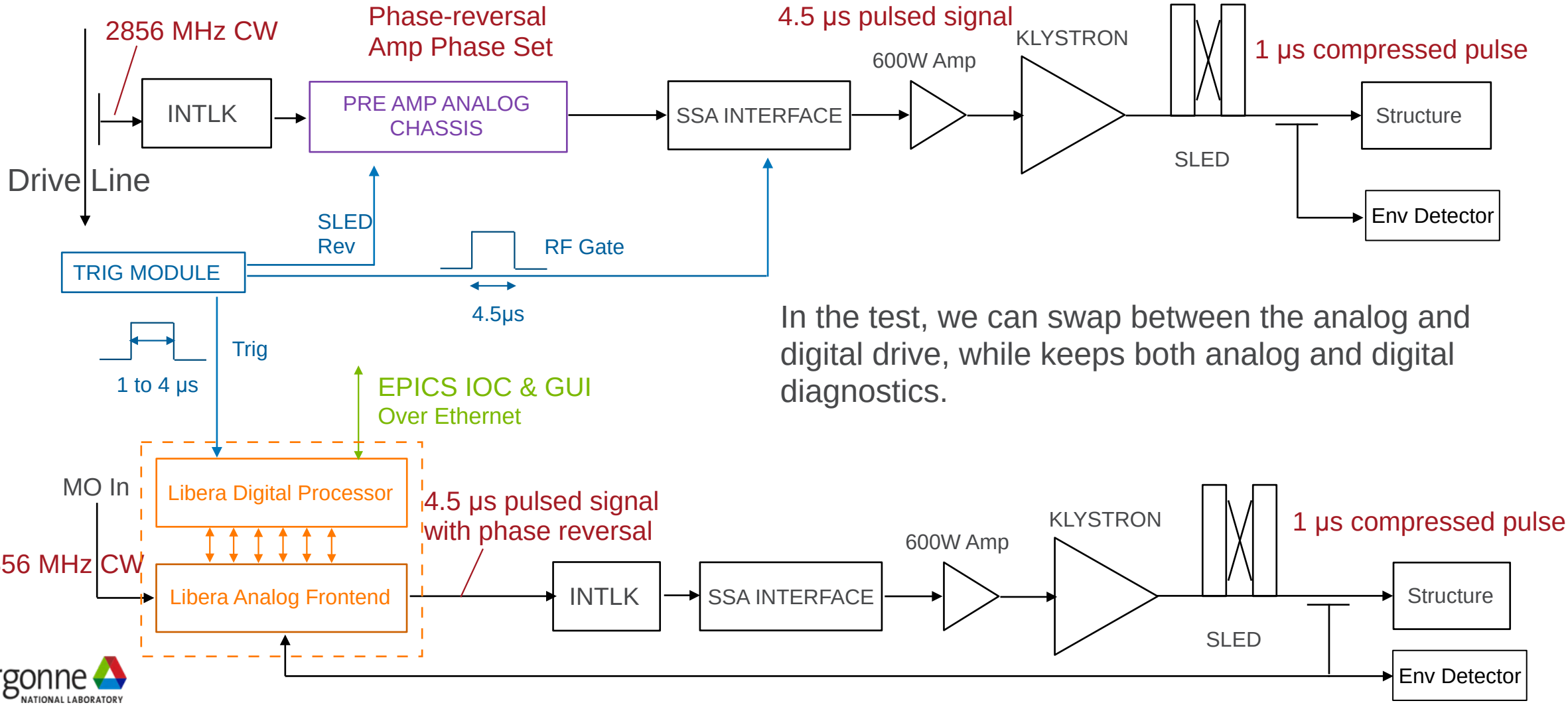
Libera LLRF Acceptance Testing at L6

- The New Libera S-Band LLRF system test setup at L6



In the test, we can swap between the analog and digital drive, while keeps both analog and digital diagnostics.

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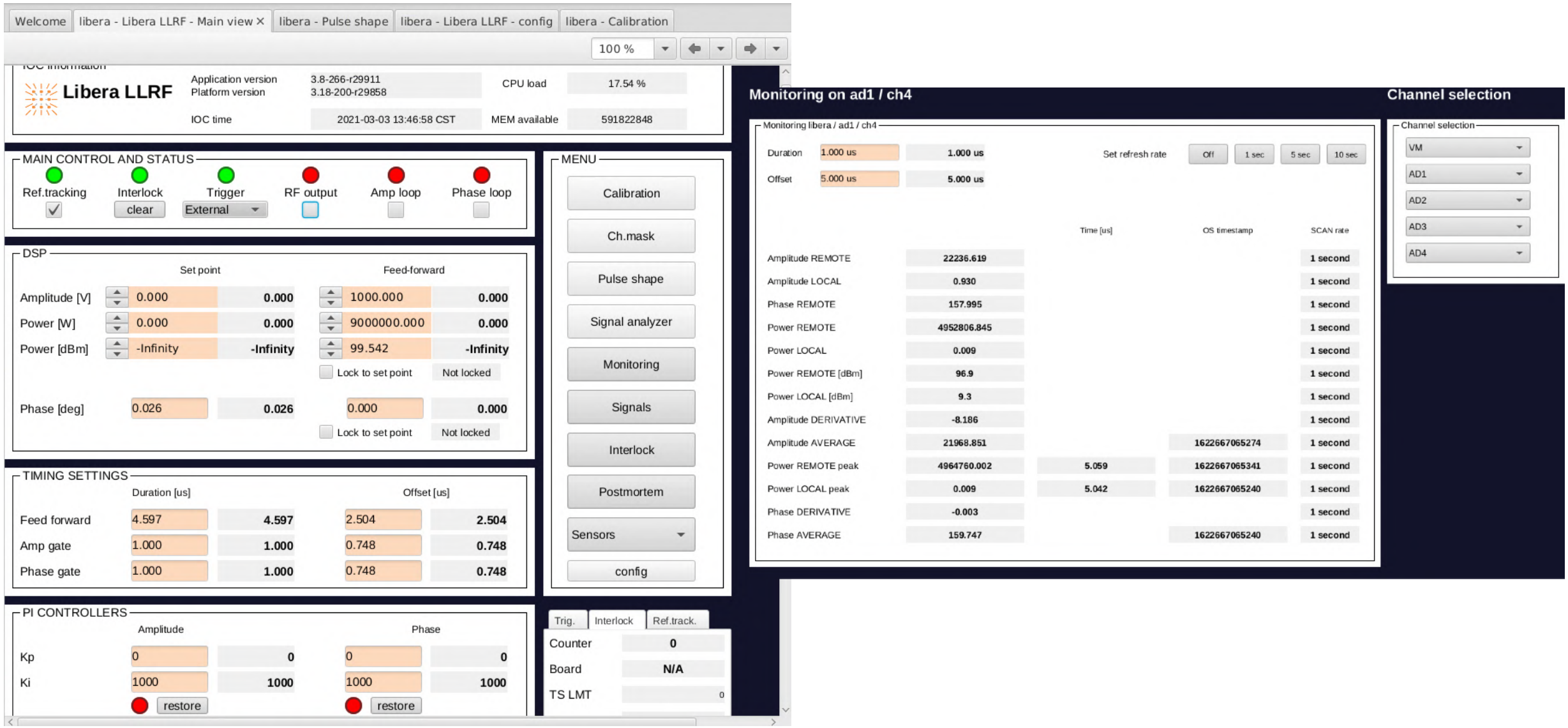
Remote Collaborative Development

- Debugging is part of the system development
- Lots of software bugs are identified during onsite test at L6
- Good communication & quick response with I-Tech
- With two software release, all the confirmed bugs have been fixed

Drive Setting & Monitoring on Phoebus GUI



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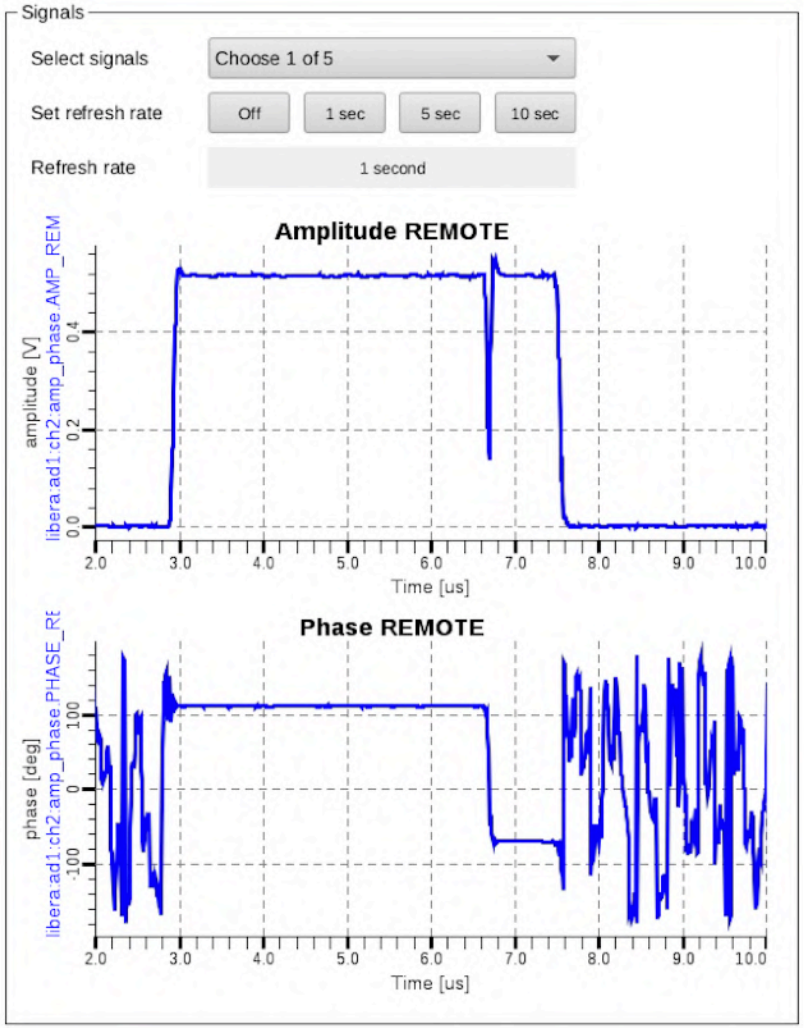
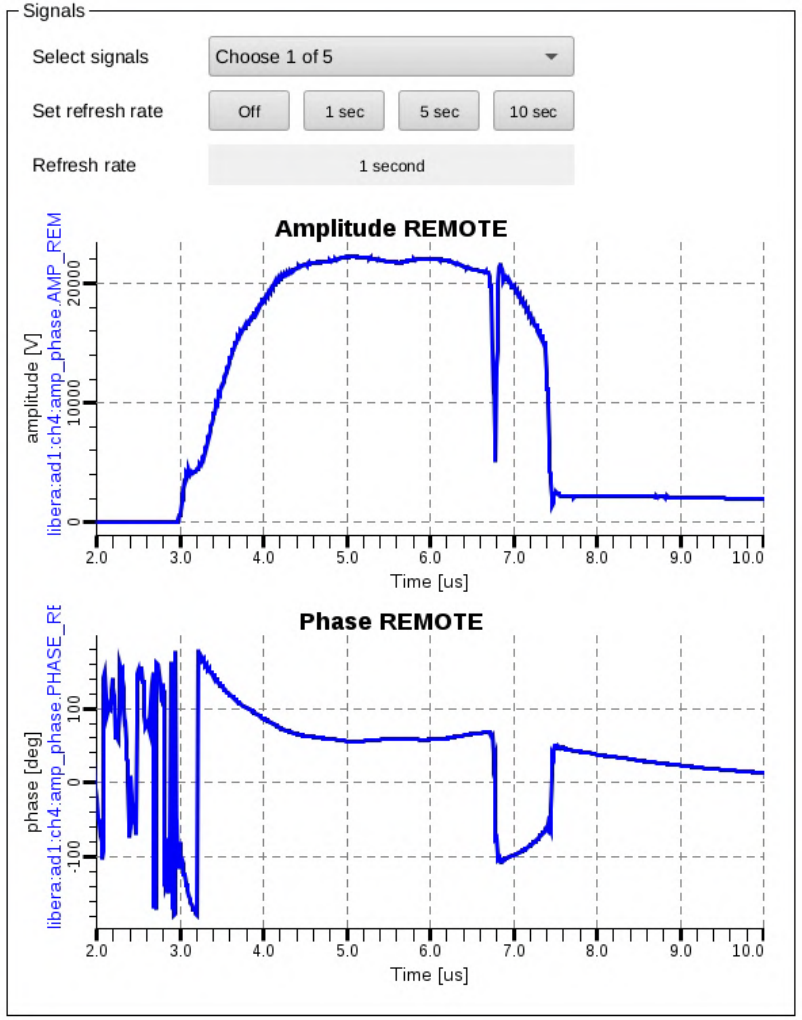
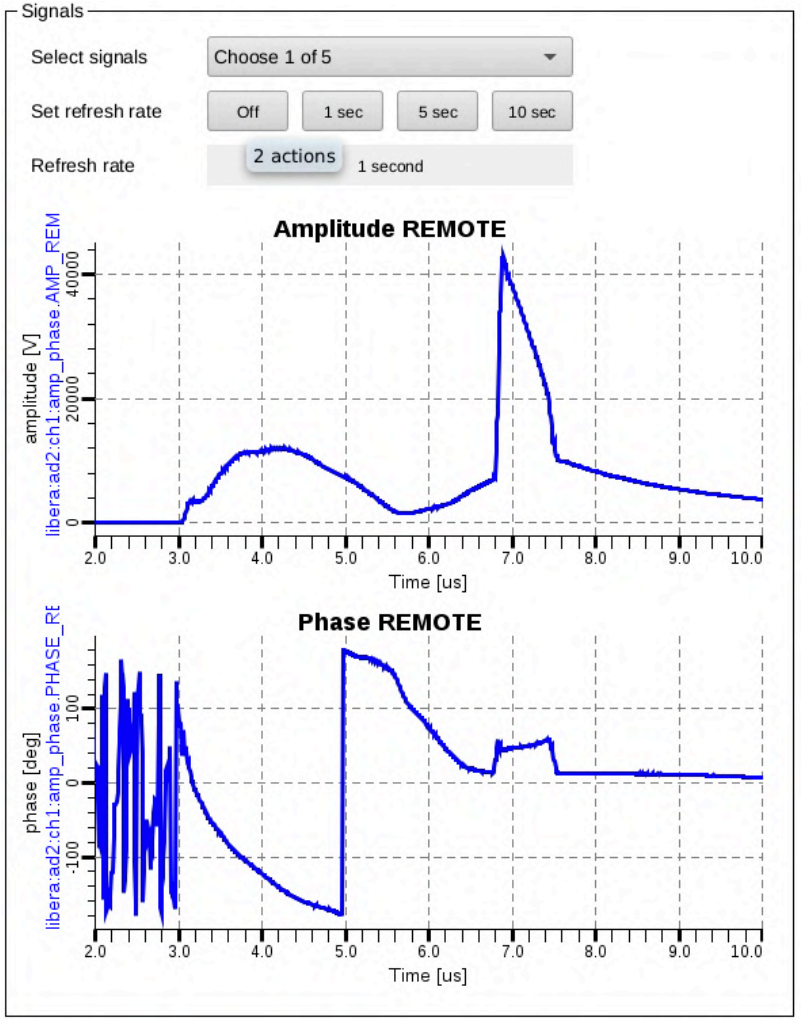
Time-Resolved Measurement on Phoebus GUI



RF Drive Output



Klystron Output



SLED Output

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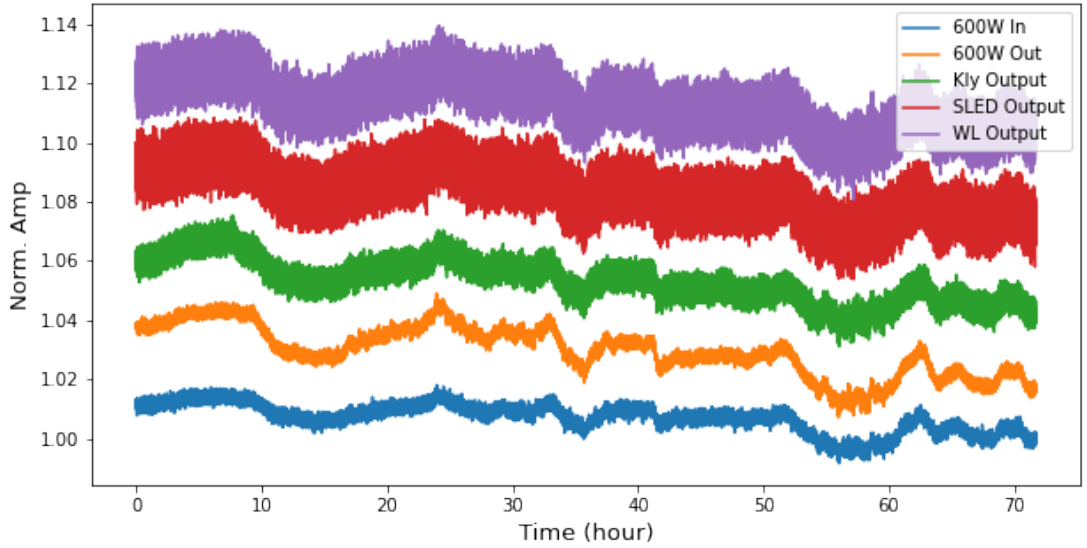
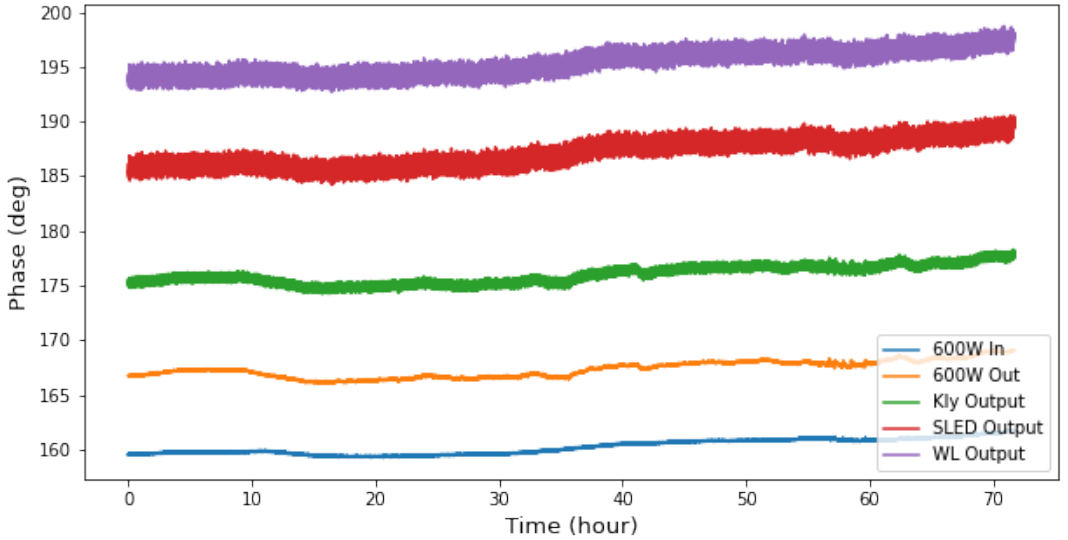
THE NEW SOFTWARE RELEASE TEST SUMMARY



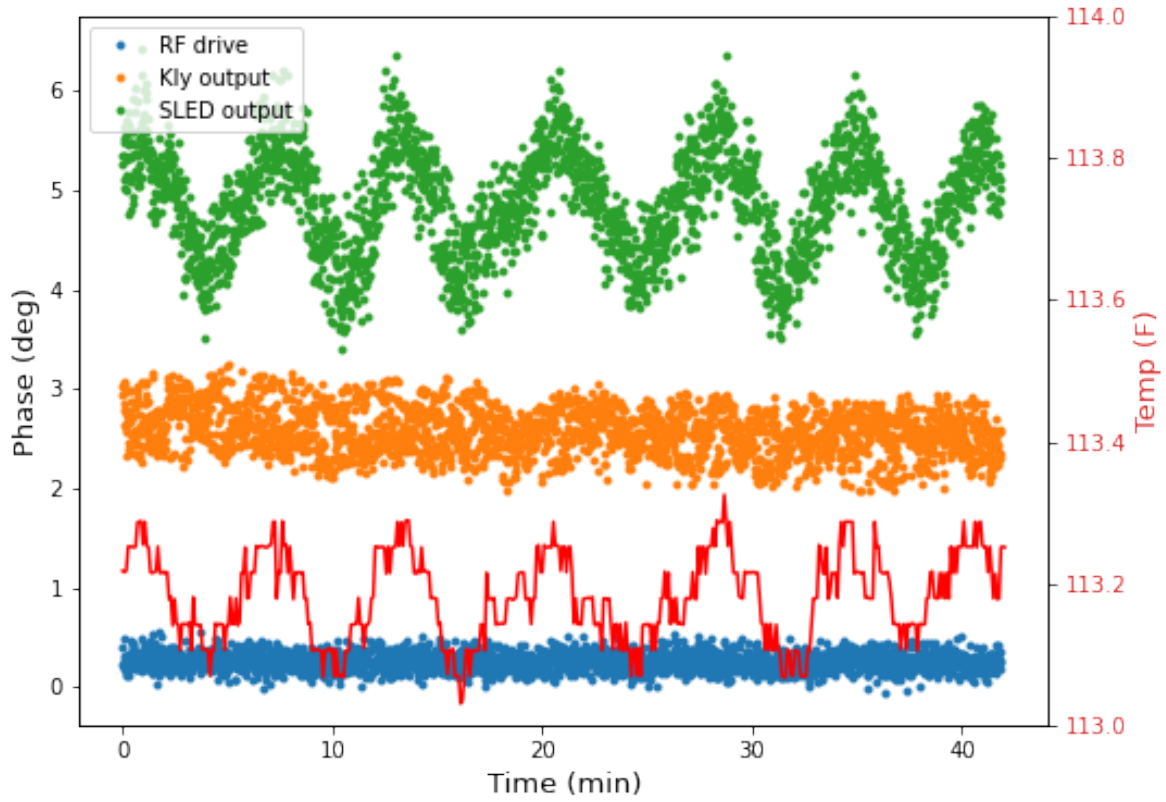


		CHANNEL SELECTOR		DURATION		OFFSET		AMPLITUDE	PHASE	TIMESTAMP
RF Drive Mon	SD_0 channel	Ch2	**Ch2**	1.000 us	**1.000 us**	3.500 us	**3.504 us**	**0.055 %**	**0.027 deg**	**1618186934921**
600W Amp Out	SD_1 channel	Ch3	**Ch3**	1.000 us	**1.000 us**	4.000 us	**4.000 us**	**0.042 %**	**0.027 deg**	**1618186934921**
Kly Out Fwd	SD_2 channel	Ch4	**Ch4**	1.000 us	**1.000 us**	5.000 us	**5.000 us**	**0.092 %**	**0.156 deg**	**1618186934921**

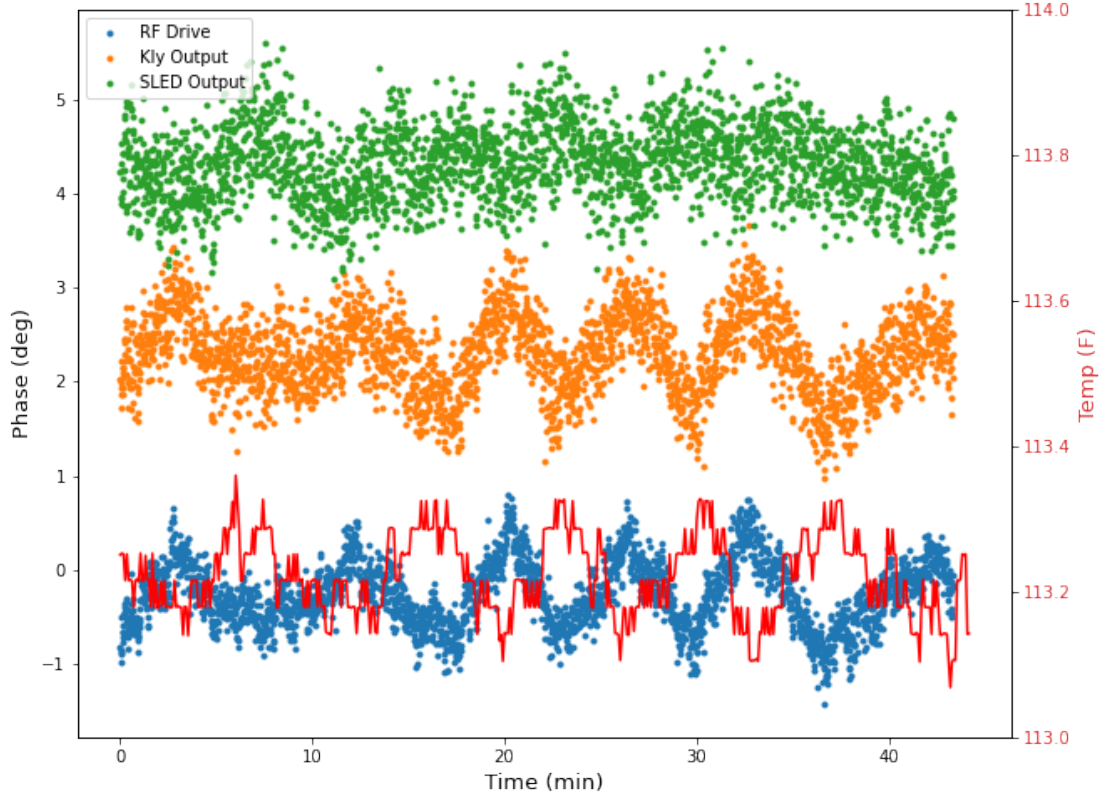
		CHANNEL SELECTOR		DURATION		OFFSET		AMPLITUDE	PHASE	TIMESTAMP
SLED Out Fwd	SD_0 channel	Ch3	**Ch3**	0.600 us	**0.597 us**	6.820 us	**6.824 us**	**0.169 %**	**0.238 deg**	**1618186819473**
Water Load	SD_1 channel	Ch5	**Ch5**	0.600 us	**0.597 us**	6.780 us	**6.782 us**	**0.138 %**	**0.205 deg**	**1618186819473**

The new software can provide pulse-by-pulse Amp & Phase jitter within the specified window

NEW FUNCTIONS WITH DLLRF



OPEN LOOP

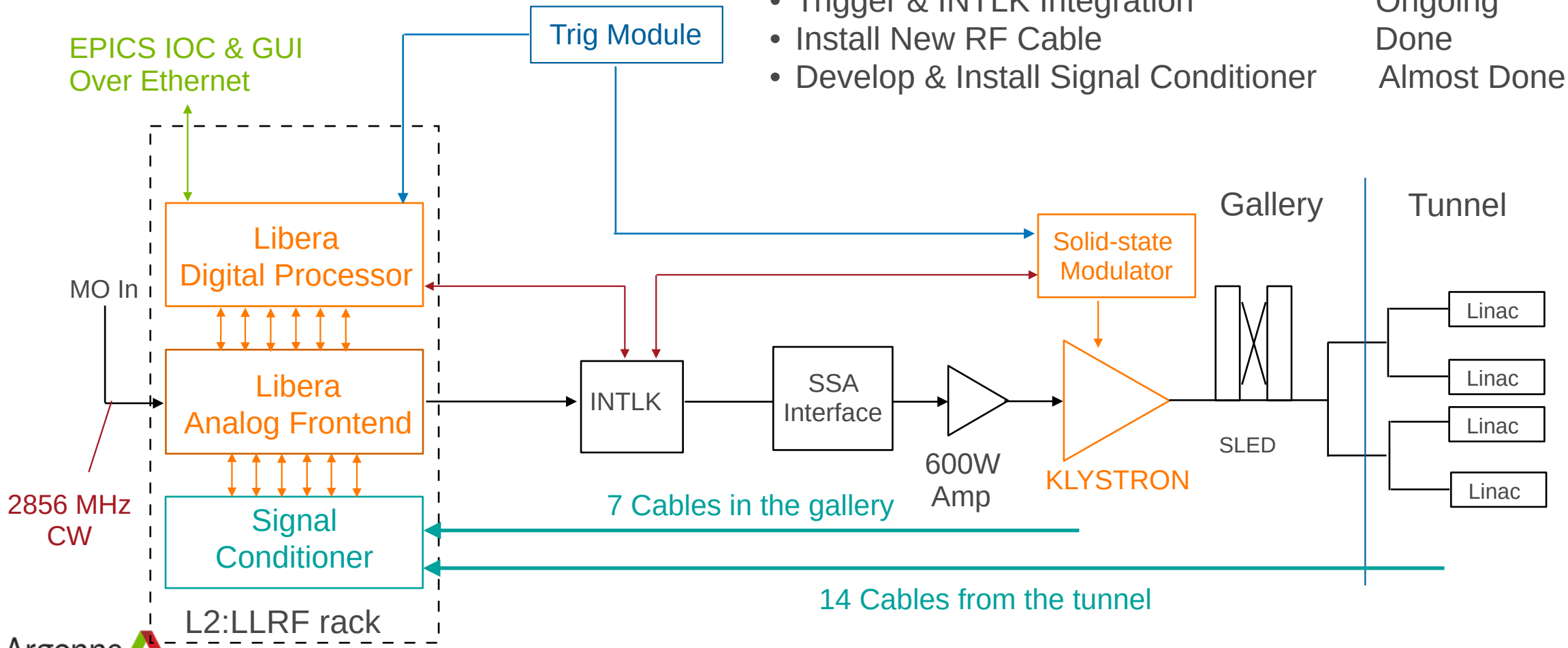


CLOSE LOOP with the feedback on.

The New DLLRF will be installed for operation by early 2022

- New 50 MW RF Station Diagram

- LLRF Acceptance Test — Almost Done
- EPICS Integration & MEDM — Ongoing
- Trigger & INTLK Integration — Ongoing
- Install New RF Cable — Done
- Develop & Install Signal Conditioner — Almost Done



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Acknowledgement

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- David Meyer
- Terry Smith
- David Jefferson
- Tony Pietryla
- Ali Nassiri
- Yine Sun

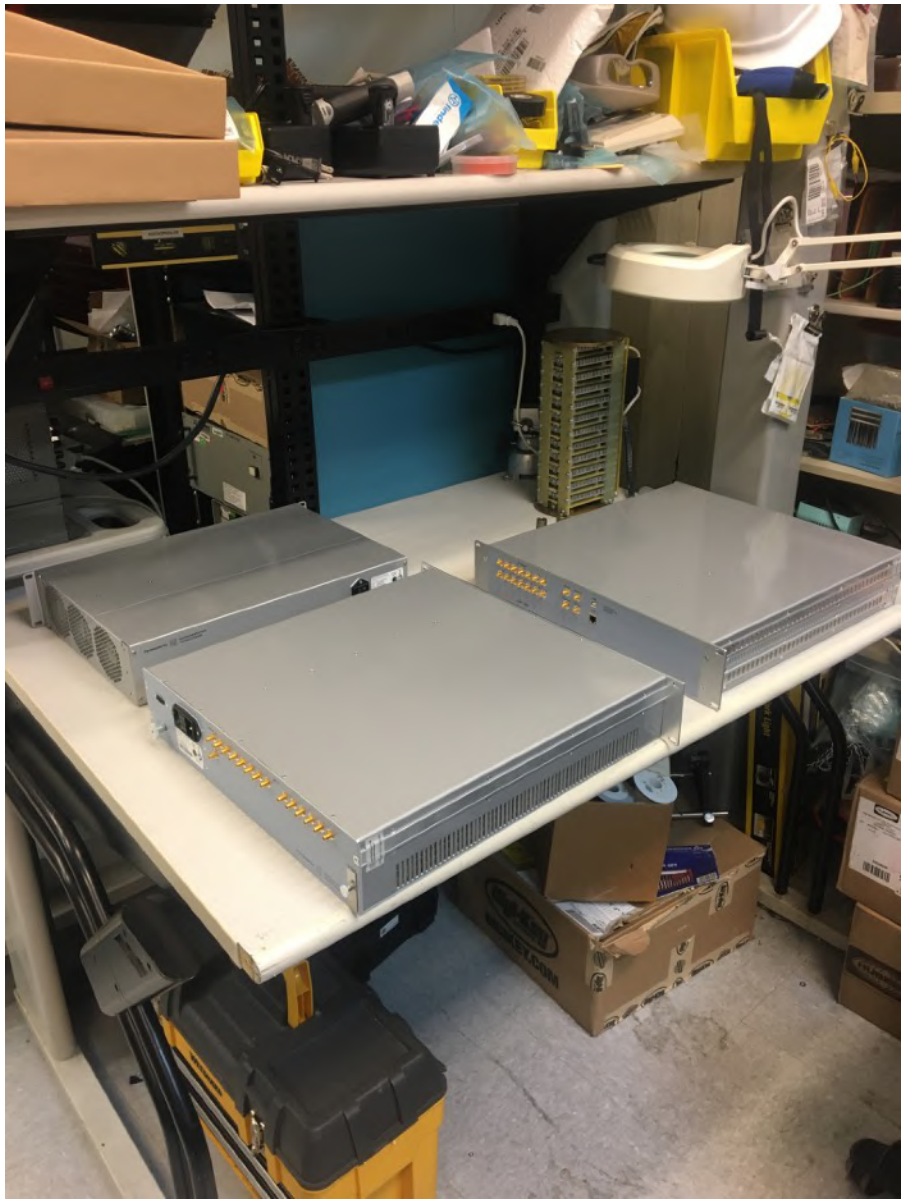
INSTRUMENTATION TECHNOLOGIES

- Borut Baricevic
- Damijan Skvarc
- Peter Leban
- Peter Paglovec
- Manuel Cargnelutti
- ….

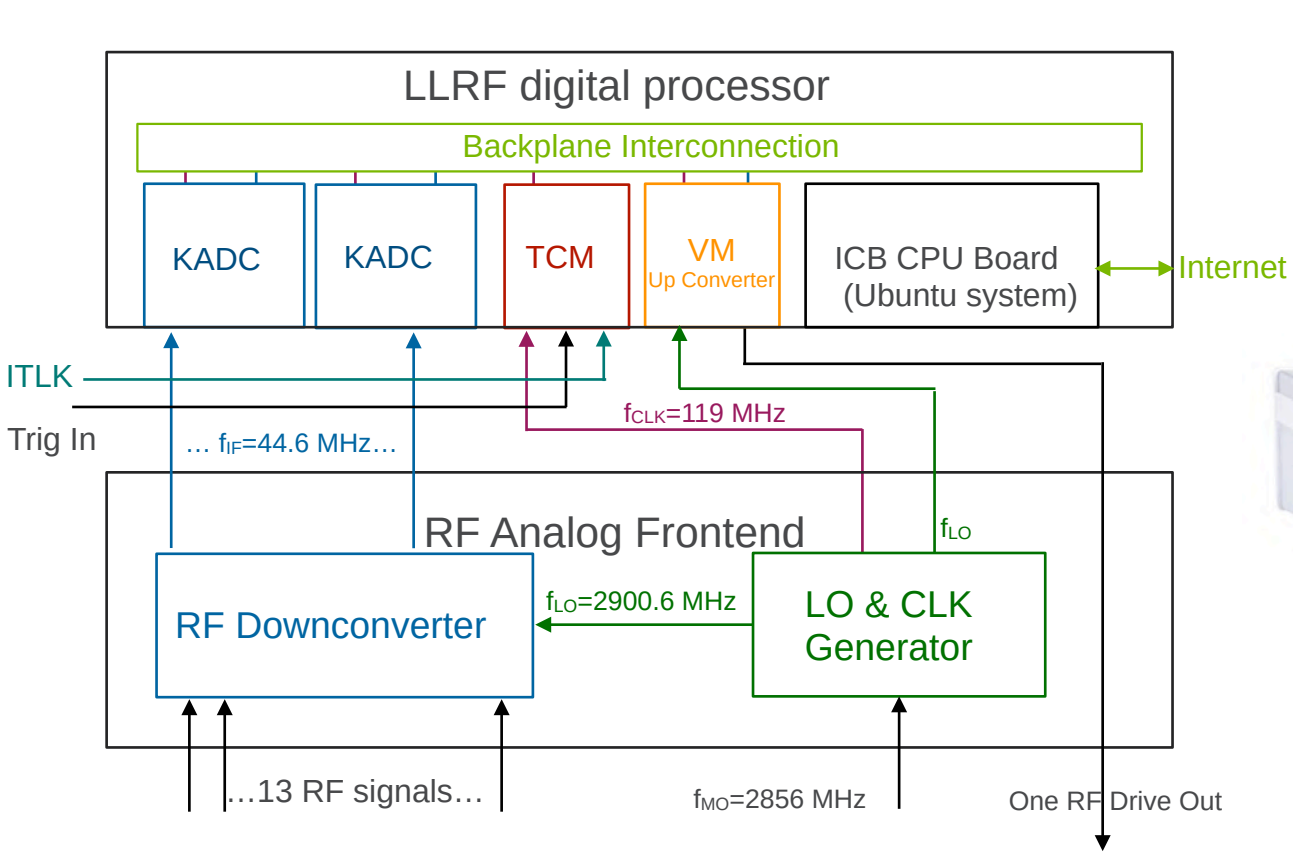
Thank you

Backup Slides

Libera LLRF System test at L6



Libera LLRF System



The Libera S-band LLRF system is based on the MicroTCA standard, developed in 2017.

New LLRF System Development

- Through a number of discussions, I-Tech and Argonne has come to an agreement on 13 required revisions and I-Tech proposed a plan.

Type	Argonne Recommendation	I-Tech Revision Plan
Hardware	Digitizer ADC & VM FPGA need latest technology	Will implement Kintex Ultrascale+
Hardware	Increase the number of channels from 13 to at least 20.	Use 2 Analog Frontends with 4 ADC boards to support 22 channels
Hardware	Increase the drive power level and add monitor port	Will increase power level to 20 dBm, and add one RF monitor port.
Software development	Need specific EPICS PVs to control the SLED phase reversal timing.	Will add customized wavetable and software function to support that, will add this function to sub window in GUI
Software Upgrade	Upgrade to EPICS 7	Will upgrade to EPICS
Software Development	Current GUI based on CaQT is not well supported, need MEDM	Will develop GUI based on MEDM with Argonne specified tool

New LLRF System Development

- Argonne Recommendation & I-Tech Revision Plan / continue

Type	Recommendation	I-Tech Revision Plan
Hardware	TRIG & INTLK LEMO pin-type are not supported and hard to integrate	Will change hardware design based on the specification from Argonne
Software development	Need chrony NTP time-stamp with pulse counter & FPGA time	Timestamp will include FPGA counter, pulse counter and NTP (chrony)
Software development	Need to see the waveform when INTLK event happens	Add post-mortem buffer and it will store the waveforms when INTLK events
Software upgrade	Operation system needs to upgrade to 18.04 LTS, 20 LTS is recommended	Will go to 18.04 this time, 20 LTS will be supported in future
Software development	Need specific EPICS PV for Pulse by Pulse RMS Amp/Phase jitter statistics	Will develop that function and implement that.
Software development	We need incremental dB format for klystron set-point in GUI	Will develop this function in MEDM based on Argonne requirement
Software development	Need longer processing window (from 8 us to 16 us)	With hardware upgrade, 32 us can be well supported