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Development of the FAIR pLINAC RF systems and LLRF (Part II)

Borut Baričević, Libera Workshop, June 2017, Vipolže

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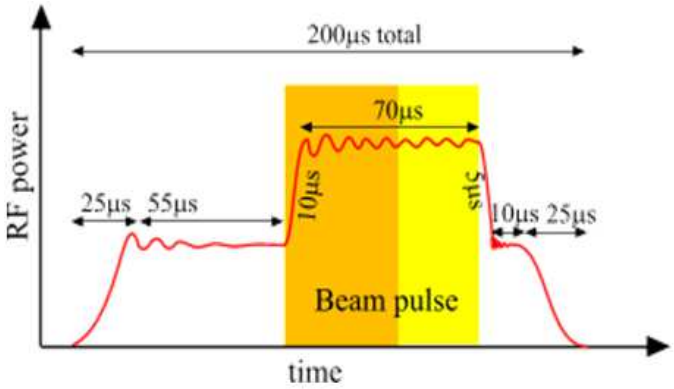
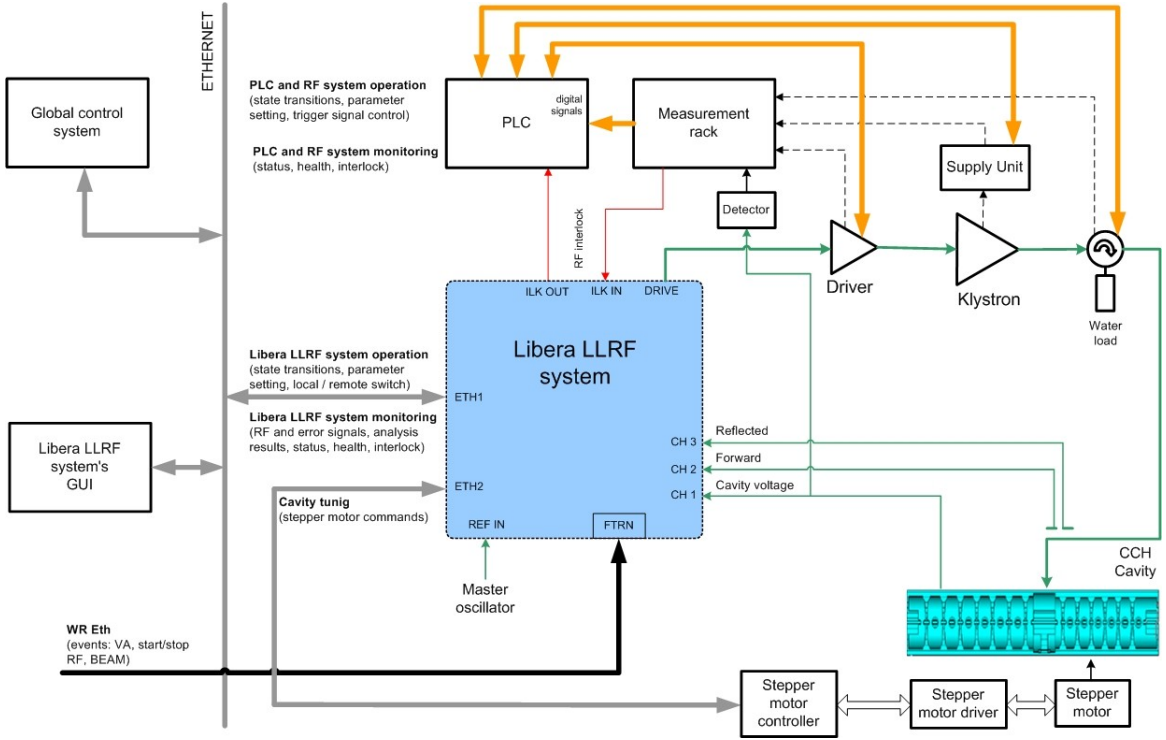
pLINAC LLRF system requirements



- RF: 10 Normal Conducting 325.224 MHz cavities
- RF control over 200 s pulses up to 5 Hz rate
- Heavy beam loading FF compensation (2x input power)
- Smooth leading edge pulse shaping (AWG)
- Stability: Amp 0.1% RMS, phase 0.33 deg RMS
- Stepper motor cavity tuning, applied through states
- Local operation mode: “Expert GUI mode”
- Machine protection: intermittent interlock, persistent interlock and AER
- Virtual accelerator time multiplexed operation through White Rabbit timing system
- Real-time operating system (CentOS)

Instrumentation Technologies

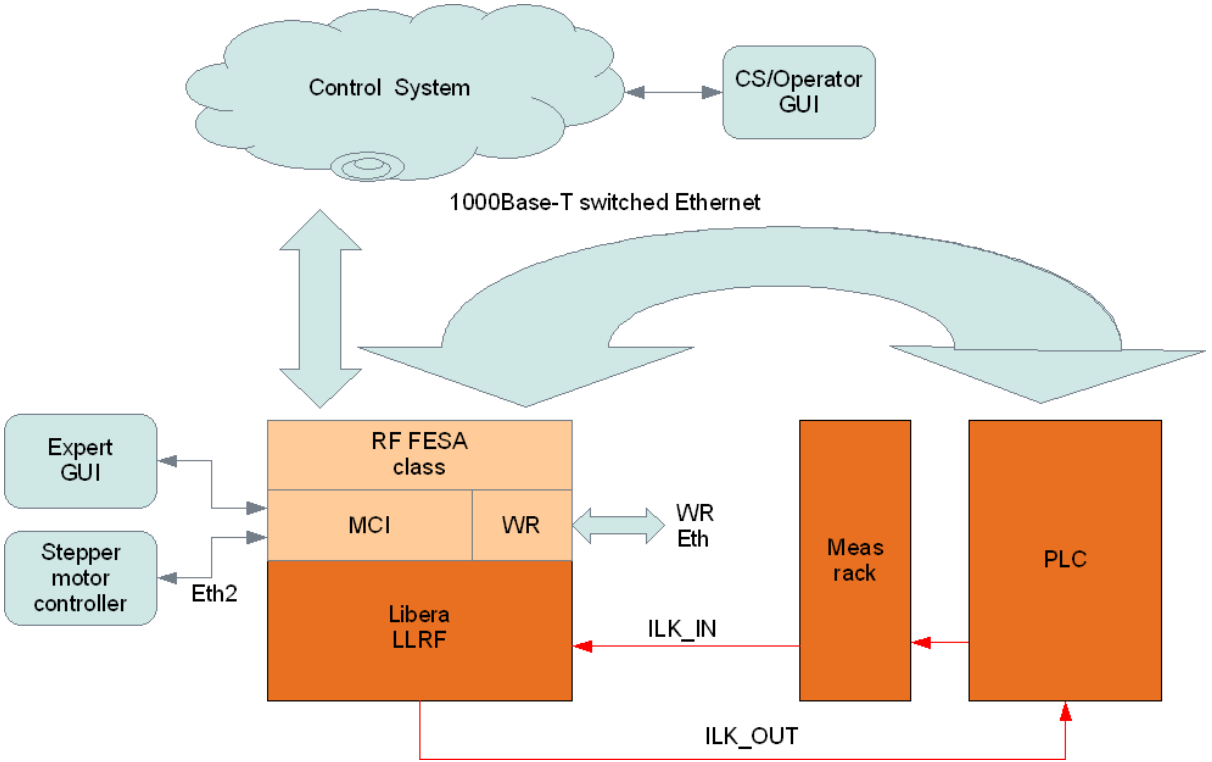
LLRF system block diagram



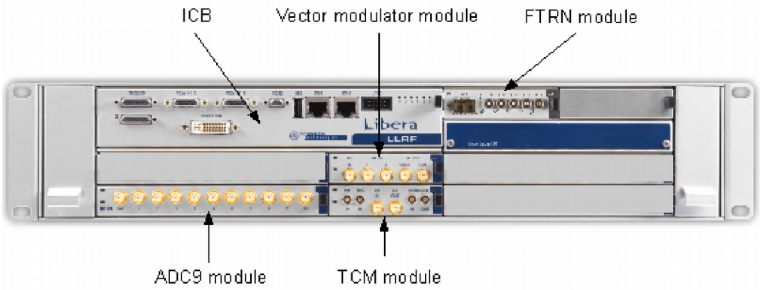
Interfaces to LLRF

RF control interfaces:

- Control System: FESA
- Expert GUI
- Timing system control: FTRN with White Rabbit (Virtual Accelerators)
- Interlock
- Stepper motor controller



Libera LLRF HW & connection diagram



The FTRN module:

- Receives the timing system events
- Provides RF pulse trigger (trigger 1)
- Provides beam trigger (trigger 2) for beam loading compensation
- Configures Libera LLRF controller in real-time

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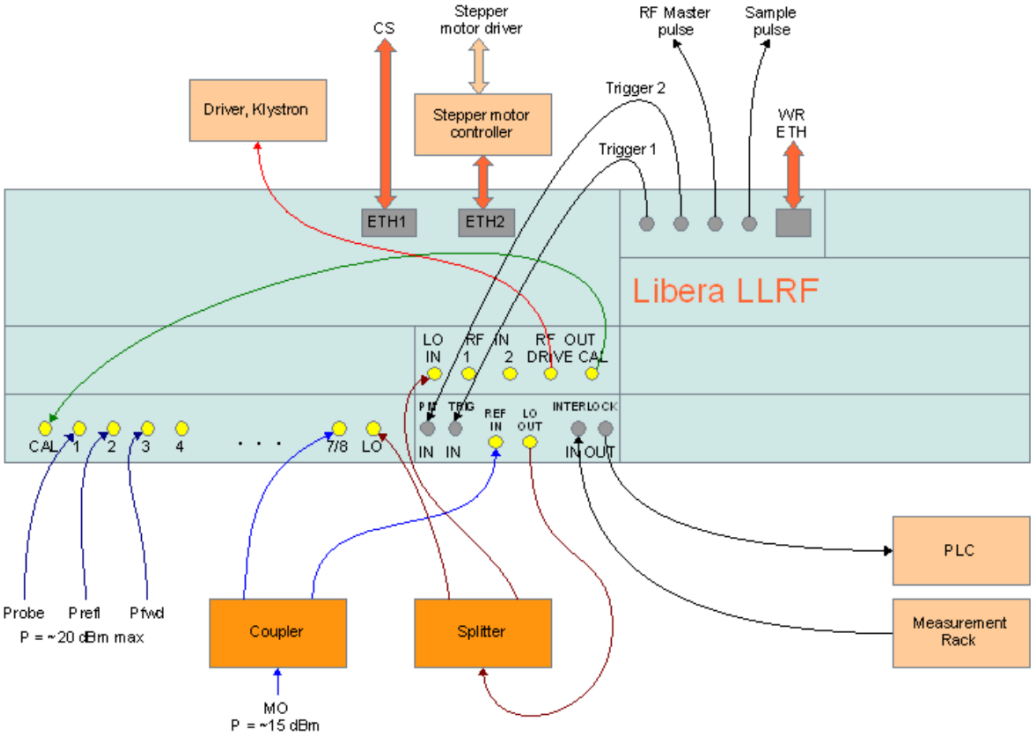
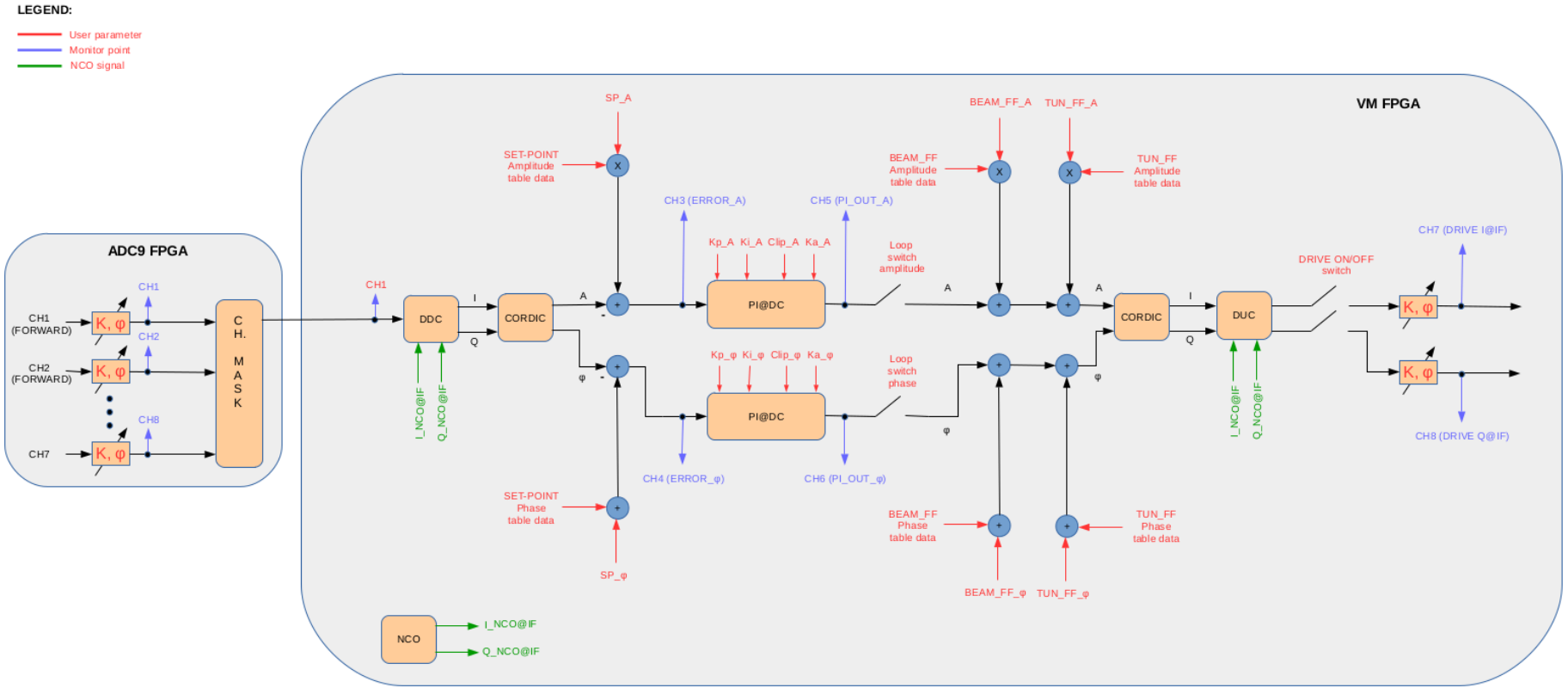


Libera DSP block diagram (main RF control loop)



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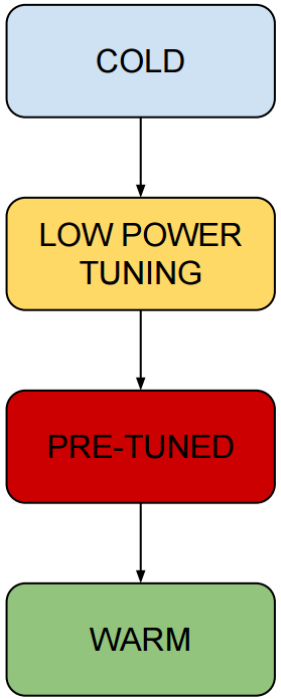
Cavity tuning system

Slow Cavity Tuning Feedback (SCTF)

- Input: cavity field decay analysis combined with dir. coupler signal analysis (FWD,RFL)
- Output: stepper motor controller

LLRF tuning states:

- Cold: initial state
- Low-power tuning: open loop at 1-10% nominal voltage, tuning cavities
- Pre-tuned: closed loop cavity voltage ramp-up to nominal voltage
- Warm: normal LLRF operation



Instrumentation Technologies

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Machine protection

- Intermittent interlock: Interlock conditions suspend RF drive within the same pulse and restore it for the next pulse.
- Persistent interlock: If a predefined number of intermittent interlock conditions are detected in a row, the RF drive is disabled and a persistent interlock is issued by the LLRF.
- Advanced Error Reporting (AER): An additional interlock condition is included by means of monitoring the LLRF controller error signal within a predefined timeframe.

Conclusion

- FAIR and I-Tech have jointly discussed the pLINAC LLRF requirements and defined the LLRF system conceptual design.
- The Libera LLRF system is being customized in order to implement the required features.
- Development is planned to be completed till mid 2018.