Digit500 Tests on SXFEL

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Recent status on SSRF

- Synchrotron radiation facility: upgrade in progress(beam lines construction)
- Soft X-FEL Test Facility: completed in this June. User Facility: will start in August
- SHINE: tunnel construction in progress, and key-technologies research stage

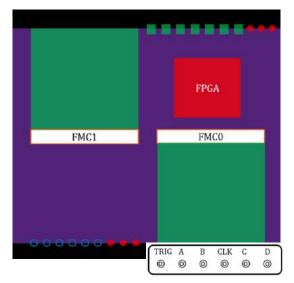






BPM processors for SHINE

- □ Signal processing for Cold Button, Stripline, Cavity BPMs
- □ Standalone structure based on Xilinx SOC FPGA, 1U' height
- □ FPGA mother board, FMC ADC and timing mezzanine cards
- □ \geq 500MSPS, \geq 14bits, also can be used as bunch by bunch processor on synchrotron facility
- □ 1MHz repetition rate
- Digit500 is applied as a test platform to check the design.







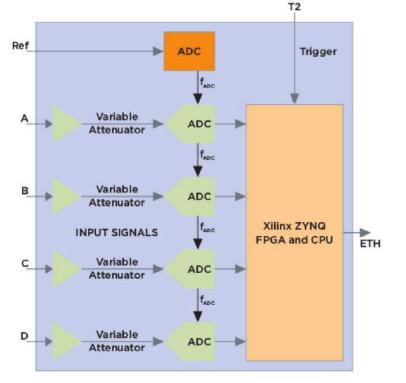
Pre-research with Digit 500

Libera Digit 500 - overview



- 4 input channels 500hm
- ADC: 500MHz 14bit
- Sampling clock: free running or externally locked with HW PLL
- 32 dB of variable gain (channel independent)
- 3x LVTTL trigger lines

DC~250MHz BW







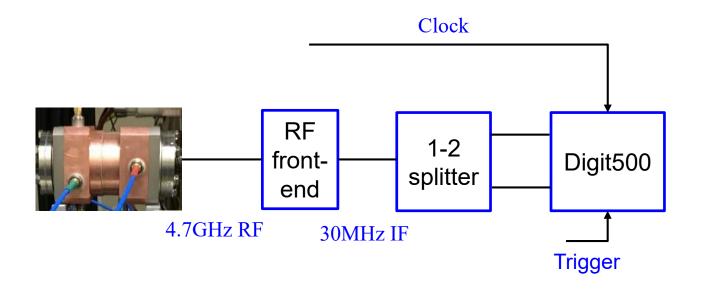


Cavity BPM test

Cavity BPM reference IF signal @700pC was split to 2 ways and fed into Digit500 2 channels

External 476MHz sampling clock

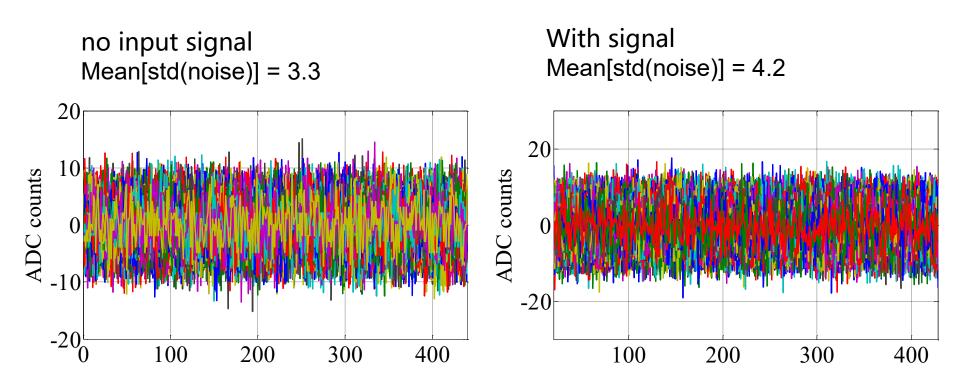
Off-line data evaluation: noise level and resolution







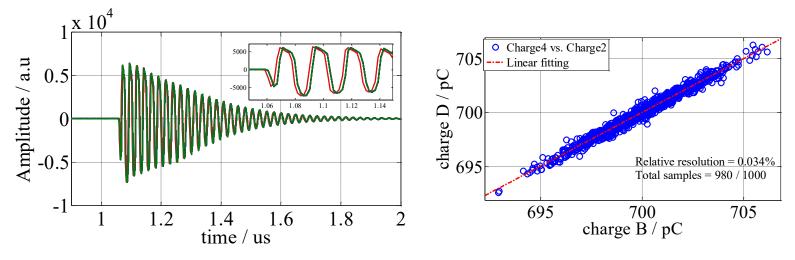
Noise level



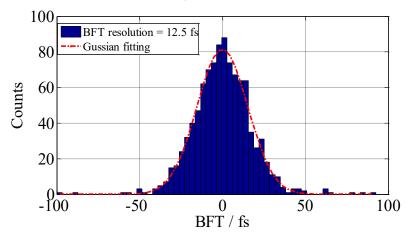


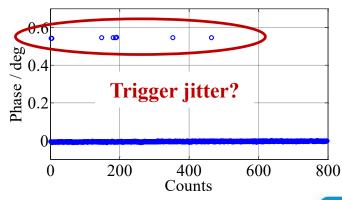


Relative amplitude resolution 0.034%



Relative phase resolution 12.5fs

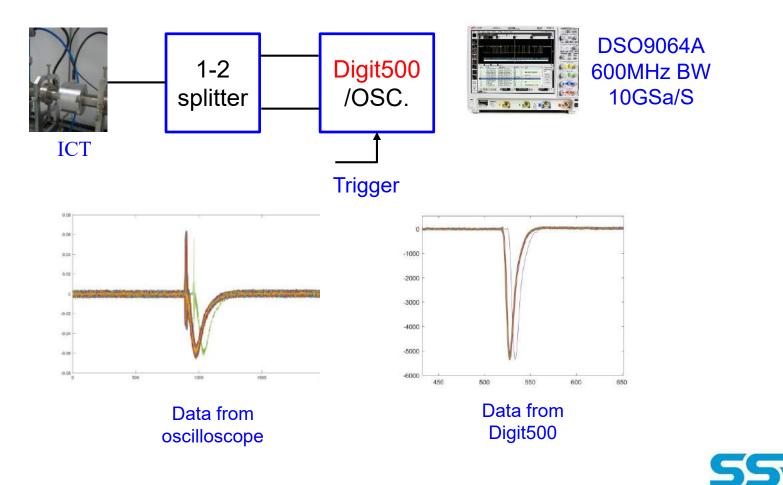








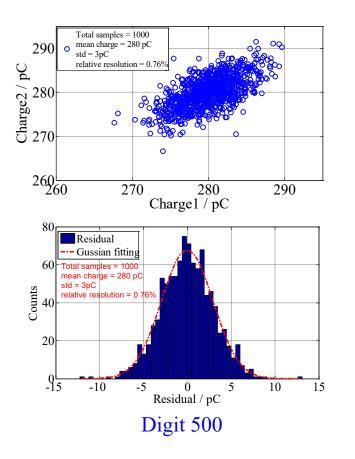
Beam charge measurement

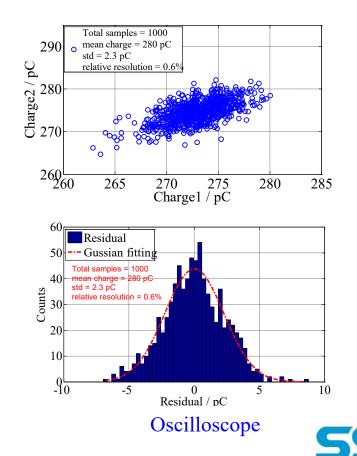




Current calculation directly

The Digit500 relative resolution is 0.76% compared to 0.6% of oscilloscope.

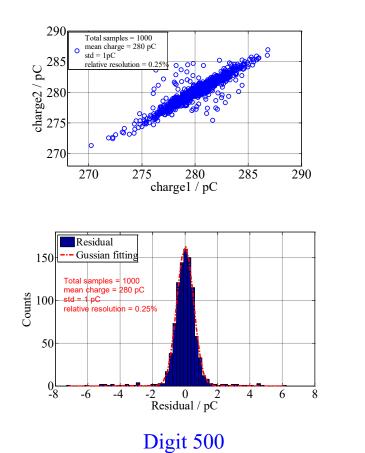


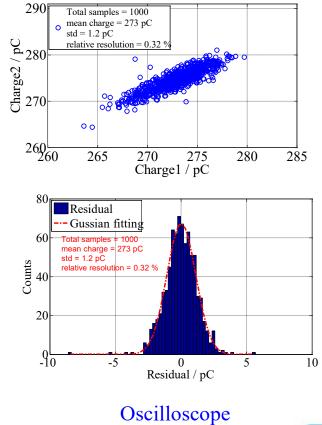




Charge measurement--PCA

After applying PCA, the Digit500 relative resolution is improved to 0.25% compared to 0.32% of oscilloscope.









Conclusions

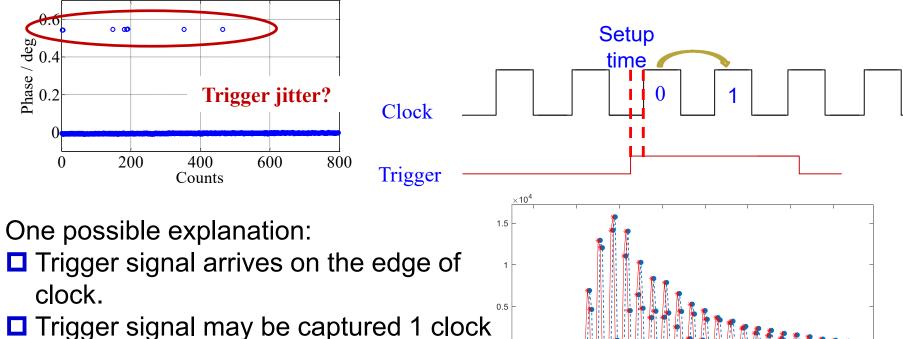
Digit500 hardware shows good performance, can be used for cavity BPM signal acquisition. Also stripline BPM can be used.

SXFEL is using oscilloscope for ICT charge measurement. Digit500 shows comparable performance, could be used for charge measurement after calibration.





Question: How to resolve the clock and trigger jitter?



-0.5

-1.5

220

240

260

280

300

320

340

delayed.Phase result will be different after one

How to resolve this problem?

sample point.