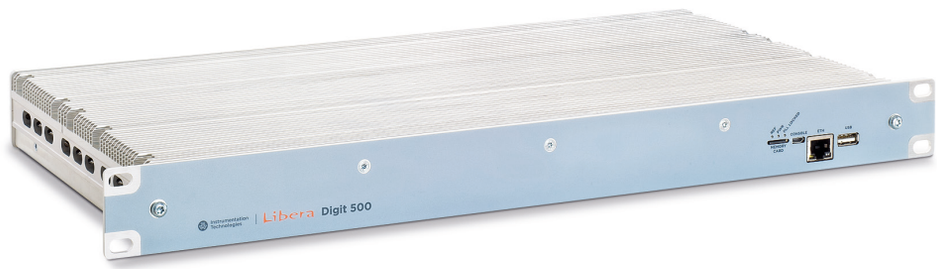
LIBERA

Libera Digit 500

The Libera Digit 500 is a **low-noise and wide dynamic range digitizer** with 4 channels and a sampling frequency of 500 MHz, phase locked to an external reference signal. The data is stored in a configurable segmented buffer, with different acquisition modes and trigger rates up to 1 kHz.



Highlights

- 4 channels sampled at 500 MS/s with 14-bit ADCs
- AC coupled and DC coupled versions
- 31 dB variable gain, more than 90 dB dynamic range
- Different buffer acquisition modes with configurable segmented buffer
- EPICS, Tango, Python, Matlab and LabVIEW compatible
- Passive cooled, PoE++ compatible

Applications

- Particle accelerators
- High energy physics
- Nuclear and particle physics
- Dark matter and astroparticle physics

Digitizer with phase-locked sampling frequency

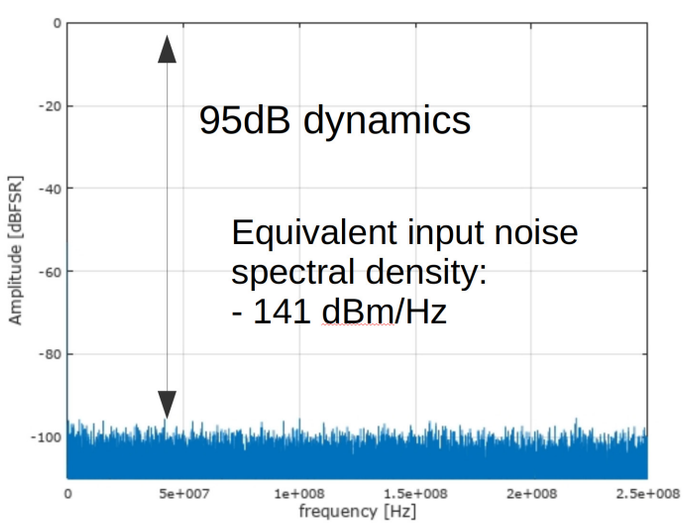
Each of the four inputs is adjusted in amplitude with a 31 dB software-controlled variable attenuator and later sampled by the ADC converter with sampling controlled by an external reference signal locked through a phase-locked-loop (PLL). The dynamic range of the system is over 90 dB.

AC and DC coupled versions

The DC-coupled version has a front end with 250 MHz bandwidth, suitable for time-domain processing of signals coming from different types of sensors.
The AC-coupled front end has a bandwidth ranging from 1 MHz to 2 GHz and is suitable for narrow-band signals and digital down-conversion applications. The front end can also be customized to include different types of analog filtering.

Digital offset removal and flexible data buffering

The ADC data offset can be removed in the FPGA before the data is stored. One LEMO trigger input is used to trigger the data acquisition in a large ADC buffer with a total size of 4 GB. The buffer can be segmented in chunks of minimum 32768 samples and can be acquired in different modes.



Single side-band FFT of 32768 ADC samples acquired with Libera Digit 500 - DC coupled

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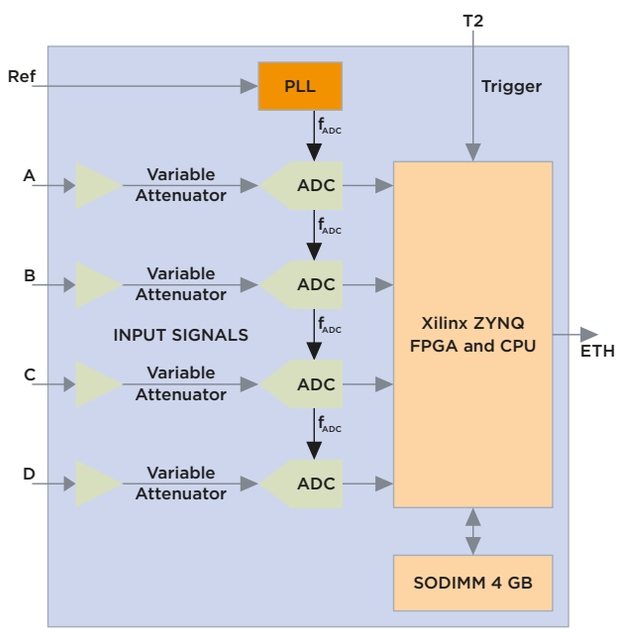
INSTRUMENTATION TECHNOLOGIES

Network connected with several software interfaces

The instrument is accessible via the network, and several standard interfaces are available to facilitate the integration of the instrument into the control system. Besides the EPICS and Tango interfaces, the instrument can also be connected via a TCP-IP socket, enabling connections with Python, LabView, Matlab and others. The operating system is Linux-based and loaded via a Micro-SD card or a TFTP server.

Low power and no maintenance required

The Libera Digit 500 digitizers are based on the Xilinx ZYNQ SoC family, with low power consumption which enables the device to be passive cooled.



HW extensions and further development

SFP connectors

The Xilinx ZYNQ 7035 features four optional small pluggable slots (SFP) which can be used for fast data streaming or feedback applications.

Extension module

An extension module can be added to the digitizer to extend the connection capabilities of the device.

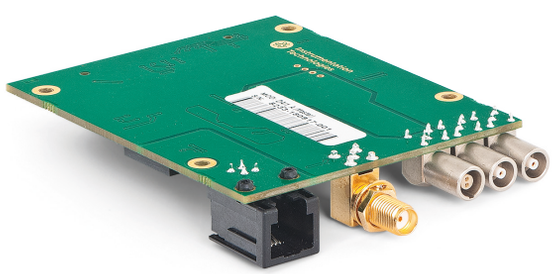
Technical Specifications

Libera Digit 500	
Dimensions	Rack-mountable, 19" wide, 1U high
Input signals and connector	4, SMA connector
Input Impendance	50 Ω
Maximum input signal level	AC-coupled: 10 dBm DC-coupled: ±1 V
Input gain / attenuation	0 – 31 dB SW programmable
Dynamic range	90 dB
Input signal bandwidth	AC-coupled: 1 MHz – 2 GHz DC-coupled: 0 – 250 MHz
ADC conversion	500 MS/s, 14 bit
Equivalent input noise spectral density with 0 dB internal attenuation	AC-coupled: -143 dBm/Hz DC-coupled: -148 dBm/Hz
Sampling clock	Locked to external reference via PLL (300 MHz – 500 MHz)
Long-term sampling phase RMS jitter	1,4 ps
Memory	4 GB RAM / more than 1 second of data per input channel
Memory organization	Segmented buffer / min. Chunk size 32768 samples per channel
FPGA / CPU	Zynq-7035 / ARM Cortex-A9
Booting	Micro-SD, TFTP server
Power	Normal power supply, PoE++
Cooling	Passive

FPGA / Software code availability

The Libera Digit 500 can be further extended by the user with modifications to the FPGA and software code (available under a non-disclosure agreement). Additional features or functionalities can be also added by our developers. For more information contact us at support@i-tech.si.

Interface	Description
LEMO single (2x)	Single-ended LEMO, Input/Output configurable
LEMO differential (1x)	Differential LEMO, Interlock output (requires external circuit)
SMA (1x)	16-bit 100 kSps DAC output, 1 V at 50 Ohm
RJ-14 (1x)	up to 20 Mbps, half-duplex



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