Digital RF Stabilization System Based on MicroTCA Technology

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Abstract–**This article presents a generic digital control system for the stabilization of Radio Frequency (RF) fields used in particle accelerators, the Libera LLRF. Low Level RF (LLRF) systems have an important contribution in the overall performance of the accelerator since they are responsible for the control of amplitude and phase of electromagnetic fields inside the accelerating structures. The goal was to develop a high performance, small form factor system that uses the latest advances in technology. In order to fulfill these design goals Micro Telecommunications Computing Architecture (MicroTCA) and related standards were chosen as a basis for the system's hardware and software development. Results of hardware development are three different types of Advanced Mezzanine Cards (AMC), Interconnection Board (ICB), chassis, backplane and replaceable fan modules. The AMC boards are LLRF application specific and have input/output ports for RF signals. In order to enable support for different RF frequencies, they also include replaceable RF circuits. The ICB implements the functions of a MicroTCA Carrier Hub (MCH) and acts as a COM Express carrier board for the mounted COM Express module. With its different ports at the front, the ICB enables local and remote operation and maintenance of the Libera LLRF. Chassis management is implemented according to the Intelligent Platform Management Interface (IPMI) protocol. The LLRF application software, which runs on the Linux operating system and includes a Graphical User Interface (GUI), enables the user to operate the system and monitor different types of RF signals.**

I. INTRODUCTION

The company Instrumentation Technologies is a provider of the Libera family of instruments. The state-of-the-art instrumentation systems are used for diagnostics and beam stabilization at particle accelerators around the world. The all-in-one instruments cover analog and real-time Digital Signal Processing (DSP) and high-level software.

Due to demanding requirements set by the digital LLRF application and in order to use the latest advances in technology a new platform was developed beyond that used in the established instruments. The newly developed instrument satisfies the following challenging hardware requirements:

1. 36 RF input channels;
2. High performance receiver of RF signals in terms of amplitude and phase noise;
3. High performance transmitter of RF signals in terms of amplitude and phase noise;
4. High quality clock generation and distribution;

5. Dedicated low latency data transfer between Field Programmable Gate Arrays (FPGA);
6. Distributed signal processing;
7. High performance acquisition of data to Double Data Rate (DDR2) Random Access Memory (RAM) (eight channels at 130 MS/s);
8. High data throughput between FPGAs and the Central Processing Unit (CPU);
9. High performance CPU;
10. Support for straightforward local and remote operation and maintenance;
11. Generic design to support different LLRF application use cases;
12. Generic design to support reuse of developed hardware for the development of new instruments;
13. Small form factor.

The new instrument satisfies the following software requirements:

1. Implementation of Intelligent Platform Management Interface (IPMI) protocol for chassis management;
2. Implementation of low latency data transfer between FPGAs;
3. Implementation of Peripheral Component Interconnect Express (PCIe) in the FPGA;
4. Development of drivers for control and transfer of user data between FPGA and CPU;
5. Use of the Linux operating system (OS);
6. Implementation of LLRF application specific algorithms in FPGAs and in application software running on Linux OS;
7. Implementation of a Graphical User Interface (GUI) for local and remote operation and maintenance of the system.

The Libera LLRF is based on Micro Telecommunications Computing Architecture (MicroTCA) and related standards [1]-[4].

II. HARDWARE ARCHITECTURE

Fig. 1. shows a fully populated Libera LLRF unit. The chassis is designed to fit into a 19 inch industrial rack and has 2U height. It includes an integrated power supply module that produces 12 V DC payload power. The mechanical structure of the chassis including backplane can host up to eight application specific Advanced Mezzanine Cards (AMCs). Four slots accept double width mid-size AMC modules and the other four slots accept single width mid-size AMC modules. Two single width slots at the top right are not used by the current implementation of the LLRF application. The

Interconnection Board (ICB) is located at the top left and it also connects to the backplane. Apart from the power supply connector, all connectors are at the front. Cooling is performed by two replaceable fan modules located at both sides of the chassis. They produce horizontal air flow. The replaceable fans modules with front side access simplify unit maintenance. This is of high importance, since fans usually have the lowest Mean Time Between Fault (MTBF) figure.

Fig. 1. Front view of fully populated Libera LLRF

III. BOARDS AND BACKPLANE

A. ICB

Fig. 2. shows the bottom view of the ICB. The ICB implements the functions of MicroTCA Carrier Hub (MCH) based on the MicroTCA standard and acts as a Computer On Module (COM) Express carrier board for the mounted COM Express module.

Fig. 2. Bottom view of the ICB

The principal implemented functions are the following:
1. Power distribution;
2. High throughput PCIe switch fabric;
3. Distribution of switch fabric clock;
4. IPMI management of AMC boards;
5. Integrated COM express module with powerful CPU;
6. FPGA for configuration and control of the ICB hardware;
7. Different types of connectors for local and remote operation and maintenance of the Libera LLRF.

Joint Test Action Group (JTAG) is used to access the ARM processors and the FPGAs located on the ICB or AMC modules. The primary application of JTAG is the transfer of ARM firmware into internal flash memory. It is also used for debugging during development of new firmware.

Two PCIe connectors provide the possibility of connecting external PCIe endpoints, where a one lane PCIe link between the external endpoint and the COM Express CPU can be established.

Standard LAN eXtensions for Instrumentation (LXI) connectors are currently used for the distribution of trigger signals when interconnecting multiple chassis to operate as one large Libera LLRF system.

The ICB offers the possibility to connect a local console by connecting a PC display to video output and keyboard to a user USB port. The standard user USB port can also be used for connecting any other USB device for the PC.

There are two possibilities available to access the ARM processors using IPMI protocol:
1. A dedicated host USB port;
2. A management Ethernet port.
A serial RS232 port is available for different applications.

Two Gigabit Ethernet (GbE) ports can be used for remote operation and maintenance of the Libera LLRF and transfer of LLRF application's signals to external systems for monitoring and offline analysis.

B. AMC Modules

These are LLRF application specific although they were designed with other applications in mind to enable reuse if future AMC module modifications are required. One of the key characteristics of all three types of AMC modules are integrated high performance RF circuits. They were developed and are manufactured as separate PCBs using high performance material suitable for RF PCBs. The RF circuit is mounted on a digital PCB at assembly of AMC module. All three types of AMC modules include FPGA and ARM processor.

Fig. 3. shows the bottom view of the 9 channel LLRF receiver double width AMC module. The chassis accepts up to four such AMC modules, which makes the Libera LLRF scalable in terms of available input RF channels. The RF circuit at the front is shielded on both sides and implements 9 RF input channels. Since a down conversion technique is used for the receiver channels, the LLRF receiver includes a Local Oscillator (LO) input. The LO signal is distributed to all the channels. The RF signals connected to the RF inputs are down-converted to an Intermediate Frequency (IF) of approximately 30 MHz (this values depends on the frequency version of the LLRF solution). Calibration input is used for a pilot signal that is distributed to all the channels. Insertion is performed at the beginning of the RF channels in order to perform accurate compensation of slow transfer function changes of individual channels. The LLRF receiver has only RF inputs for which SMA connectors are used. The digital

part of the LLRF receiver contains 9 ADCs. These are connected to the FPGA where digital signal processing is performed. Each ADC belongs to one of the RF channels and performs sampling of the RF signal at the IF frequency. The FPGA implements the Direct Memory Access (DMA) function for reading from and writing to DDR2 RAM. It also acts as a PCIe endpoint and has an eight lane PCIe link to the backplane connector. Dedicated low latency links are used to transfer digital data from the LLRF receiver FPGA to the LLRF transmitter FPGA which acts as a digital data concentrator. Data transfer is based on Serializer/Deserializer (SerDes) technique.

Fig. 3. Bottom view of the 9 channel LLRF receiver double width AMC module

Fig. 4. Bottom view of the LLRF transmitter single width AMC module

The LLRF transmitter single width module is shown on Fig. 4. and has a similar board topology (FPGA, DDR2 RAM) as LLRF receiver. The LLRF transmitter FPGA has dedicated low latency Low-Voltage Differential Signaling (LVDS) links to four LLRF receivers. There are five SMA connectors at the front. The RF circuit at the front is shielded on one side and implements two RF input channels and two output RF channels. Since down-conversion and up-conversion techniques are used, the LLRF transmitter includes a LO input. The LO signal is distributed to all the channels. One output channel is used to generate the drive signal that is fed to the external power amplifier that is connected to the accelerating structures. The other output generates a pilot RF signal used for the compensation of slow transfer function changes of the LLRF receiver analog part as mentioned in the previous paragraph. The FPGA generates the two output signals through digital-to-analog conversion. There are two double DACs located on the digital part of the LLRF transmitter. There are also two ADCs located on the digital part of the LLRF transmitter corresponding to two input RF channels. The LLRF transmitter FPGA implements PCIe endpoint functions and has a four lane PCIe link to the backplane connector.

Fig. 5. shows the digital part of the LLRF timing AMC module. Since the RF circuit is not mounted, the white connector at the rear for interconnection between digital and RF circuits is clearly visible. The digital part of the LLRF timing module has four LEMO connectors visible at the front. Two are three pole connectors used for interlock input and output. The interlock functions are used to protect different accelerator systems from being damaged in case of critical faults at the accelerator facility. The interlock output enables the Libera LLRF to report interlocks to the external interlock system. Interlock input provides an interface to enable reporting of interlocks from an external interlock system to the Libera LLRF. Two other LEMO connectors are used for two separate triggers. Triggers are distributed to all other AMC modules. The RF circuit (not shown on Fig. 5.) has two SMA connectors. One is used for reception of the master oscillator signal (MO) that is available at the accelerator facility for precise synchronization purposes. The MO signal is used to generate the ADC clock that is distributed to all AMC modules where it is transferred to ADCs, DACs and FPGAs. The RF circuit is also responsible for generation of the LO signal, which is available at the LO output. The FPGA implements PCIe endpoint with one lane PCIe link to the backplane connector.

Fig. 5. Bottom view of the digital part of LLRF timing AMC module

C. Backplane

The backplane implements all the physical connections between the ICB and the AMC modules described in the previous sections. It uses standard AMC backplane connectors for the AMC modules. A list of all the physical connections is the following:

1. 3.3 V and 12 V payload power connections from the ICB to all the AMC modules;
2. Differential lines between the ICB and each AMC module used for PCIe lanes and PCIe clock;
3. Differential line between the ICB and each AMC module for USB communication;
4. Digital lines for JTAG communication between the ICB and each AMC module;
5. Digital lines for Inter-Integrated Circuit (I2C) communication between the ICB and each AMC module;
6. LVDS lines between the LLRF transmitter and each LLRF receiver;
7. Differential lines between the Timing AMC module and each AMC module used for sampling clock distribution;
8. Two digital lines (2x interlock bus) between AMC modules for interlock information transfer.

IV. DIGITAL SIGNAL PROCESSING

The LLRF application specific DSP is shown in Fig. 6. where a simplified block diagram is presented. The algorithm used is a digital feed-back with multiple inputs (located on the LLRF receiver) and one output (located on the LLRF transmitter). Light orange squares on the left represent the LLRF receiver's FPGAs. Signals sampled by the ADCs are phase rotated and scaled. Signals arriving from the accelerating structures and that contain amplitude and phase information of the RF field are summed to form a partial vector sum. This is then transferred to the LLRF transmitter FPGA (light gray square in Fig. 6.) via low latency LVDS links where the global vector sum is calculated.
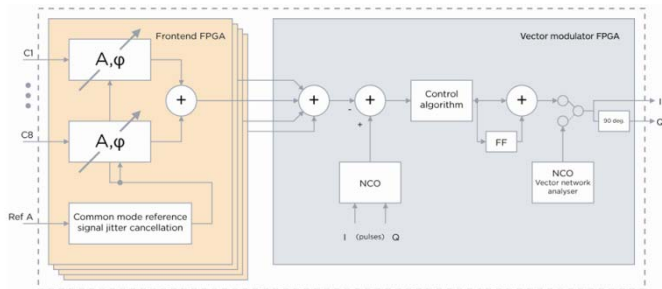

Fig. 6. LLRF application specific digital signal processing
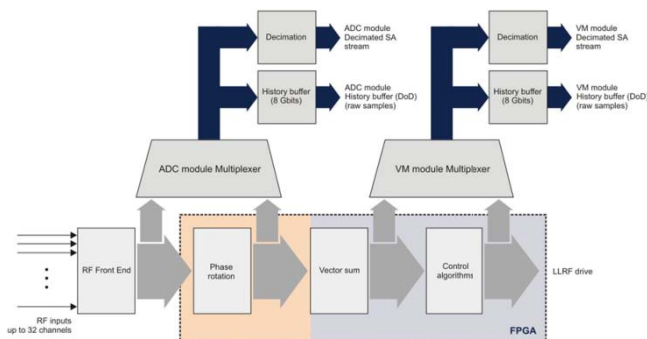

Fig. 7. DSP support for digital signal monitoring

The error signal at the digital IF frequency is calculated by subtracting the global vector signal from the set-point IF

signal that is generated by a Numerically-Controlled Oscillator (NCO). The control algorithm, implemented as a Proportional-Integral (PI) controller at the IF frequency, uses the error signal as input and calculates the feed-back output (drive) signal. In order to support advanced RF field stabilization algorithms and diagnostics of the RF system there are two additional NCOs available. One of them can be used in pulse-to-pulse feedback.

Fig. 7. Describes the infrastructure implemented in the LLRF receiver's and the LLRF transmitter's FPGAs to support digital signal monitoring. It is possible to monitor digital signals at different locations along the DSP chains. Multiplexers are used to switch between locations. Digital signal processing algorithms on the LLRF receiver and transmitter offer two types of signal monitoring. Raw samples can be saved to a history buffer in DDR2 RAM. This type is called Data On Demand (DoD). A second type of digital signal monitoring is implemented as a decimated stream of I and Q values called Slow Acquisition (SA). I and Q values are calculated by using the Digital Down-Converter (DDC) algorithm.

V. SOFTWARE ARCHITECTURE

Fig. 8. describes the software architecture used for software in the Libera LLRF. The software supplied with the Libera LLRF can be divided into software running on the COM Express module on Linux OS and GUI software that is normally running on a remote computer. The GUI was developed to be used by an advanced Libera LLRF user to independently operate the system without the need for control system integration. As shown in Fig. 8. the software running on the COM Express module (light orange square) can be further divided into hardware drivers, LLRF application and control system support. Hardware drivers provide support for the following functions over PCIe links:
1. FPGA configuration management;
2. Transfer of DoD and SA data;
3. FPGA event notifications.

Measurement and Control Interface (MCI) is implemented as a separate software layer that hides the complexity of the LLRF application to the accelerator control system. This intermediate software layer enables changes to application software without the need to update the control system as long as the interface towards control system does not change. With the support for different types of control system (EPICS, TANGO) such a strategy becomes mandatory.

Fig. 9. shows an example screenshot of the Libera LLRF GUI. The GUI is configured to monitor demodulated SA and DoD streams (amplitude on the right and phase on the left) of one signal that is selected in the menu on the left. Some buttons at the top are used for transitions between system states of the LLRF application (close the loop or open the loop for example). Others are used for starting data recording, interlock control and access to additional windows with advanced parameters.
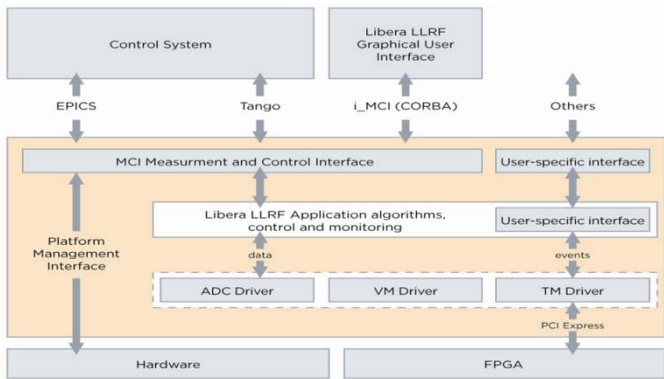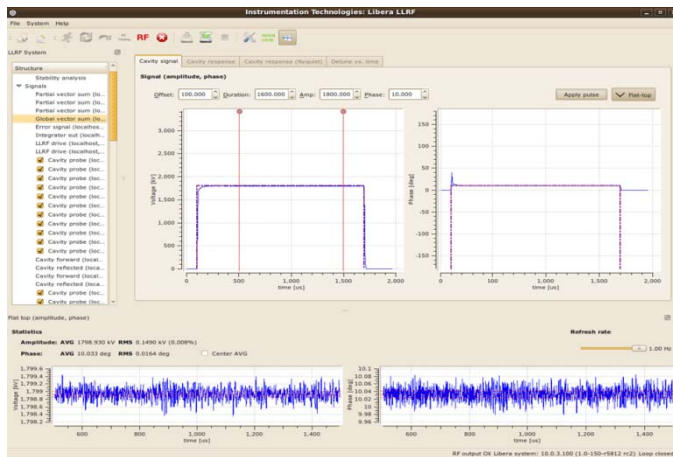
Fig. 8. Software architecture

Fig. 9. Screenshot of the Libera LLRF GUI with demodulated SA and DoD streams (amplitude on the right and phase on the left) of one of the signals that are available in the menu on the left.

VI. CONCLUSIONS

The Libera LLRF has been developed based on MircoTCA and related standards. These standards offer clear advantages when developing a new system since they provide many good solutions for mechanics, thermal management, electrical interfaces and chassis management. There is another advantage when developing to a standard in that many mechanical and electrical components are readily available and compatible to ones own development. Similar concepts apply also for software development.

Libera LLRF is a highly integrated product where all AMC modules already include replaceable RF circuits. This characteristic makes adding support for additional RF frequencies easier since only development of new RF circuits is needed.

Thanks to its modular architecture and advanced technologies that are implemented in the system, the Libera LLRF can be customized to support different LLRF application use cases at different accelerator facilities.

ACKNOWLEDGMENT

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