BEAM POSITION ELECTRONICS BASED ON SYSTEM ON CHIP PLATFORM

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Abstract

With the advances in system-on-chip (SoC) technology, the CPU and FPGA are today enclosed in the same device. This enables high-speed processing, inherent fast communication and memory sharing between the two entities. However, dedicated tools for implementation are needed as the CPU and FPGA functionalities cannot easily be decoupled.

We used the advantages of the new architecture in the development of a booster BPM electronics. Its requirements are relaxed compared to up-to-now Libera beam position monitors. Proper design of the RF part of the instrument is still a challenge. Furthermore, with optimized FPGA design we target low overall power consumption so that the instrument can be cooled passively.

INTRODUCTION

Instrumentation used in particle accelerators is today one of the most demanding fields for electronic devices and of system integration. Required performances are usually at the cutting edge in terms of signal-to-noise ratio, computational power and data throughput. Even more impressive are the requirements in terms of reliability, long term stability and fault tolerance. As a consequence, instruments are usually a complex inter-connection of different boards that host RF circuits, field programmable gate arrays (FPGAs), communication buses and CPUs. Every logical component from hardware to software is optimized for the specific application.

On the other hand, not every accelerator, or at least not every part in it, needs a top-level device to work properly. A natural example here concerns beam position monitors (BPMs) used in synchrotrons boosters and injectors, compared to those used in the storage ring. Furthermore, a lot of applications have figures of merit such as low power consumption, no need for HW and SW maintenance, and user friendliness. This can be the case for a beam loss monitor (BLM), for example.

In this paper we introduce a compact platform that aims to host a wide range of applications, being able to cover all the points presented above. Details about the system design are presented in the third section. In order to give a real picture, we will consider the development of a BPM instrument for the European Synchrotron Radiation Facility (ESRF) booster [1] as an example.

A NEW PLATFORM

Looking at the beam instrumentation used to monitor and stabilize an accelerator, every device suits a specific role, but it is possible to identify some key components that are always present:

- digital signal processing and elaboration units (e.g. FPGAs and CPUs)
- RF front-end and analogue signal processing chains
- internal communication buses
- power supply unit
- crate and cooling system (often is an active system with fans).

In this new development, we take advantage of the latest advances in SoC technology to introduce a compact platform that combines a high level of hardware integration with our knowledge regarding reconfigurable analogue signal processing.

HW and SW integration

Hardware and software are designed taking in account the balance between generality and optimization. It will be always possible to add specific features to customize it, opening at the same time the way for developing different applications, as shown in Fig. 1.

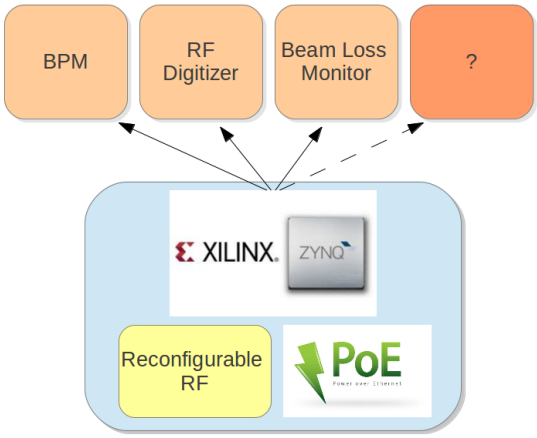

Figure 1: Platform concept based on SoC.

The core part is the SoC Xilinix Zynq 7020 [2] which combines the high-speed processing of the FPGA together with the flexibility of a CPU, all within the same chip. The inner communication between the two entities and the chance to share the same memory removes at the same time two of the biggest bottle-necks that still characterize separate-chip solutions:

- no communication protocols needed
- no data copy between FPGA and CPU.

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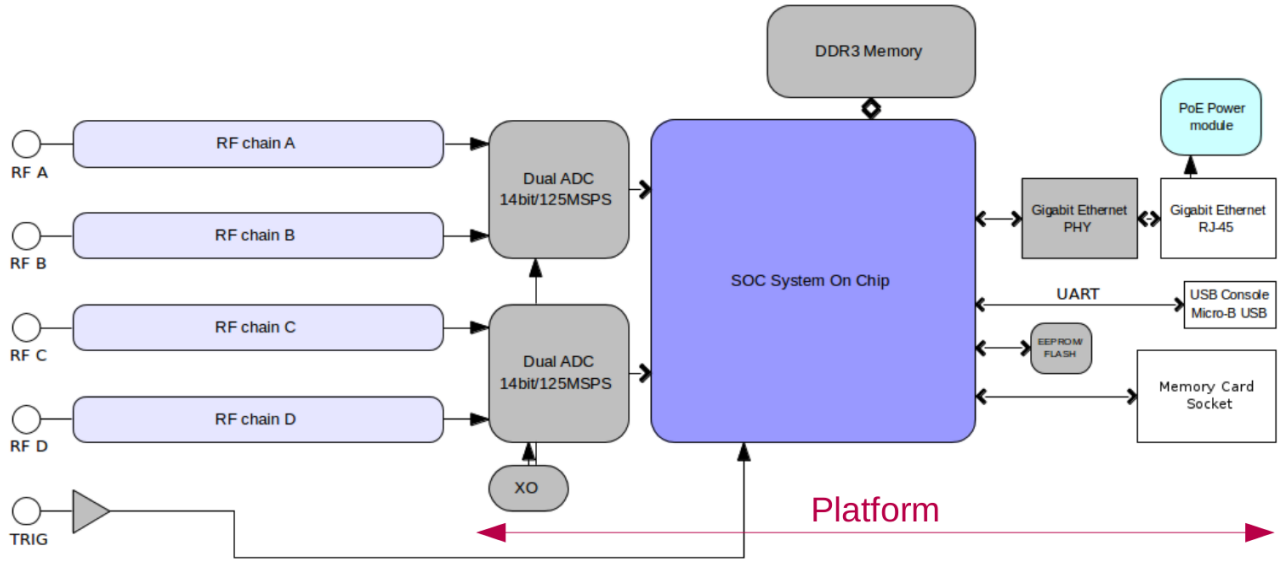

Figure 2: Basic HW architecture of the BPM instrument.

The specifics of the analogue front-end will cover the user requirements. Integrations with specific band-pass filters, phase-locked-loop (PLL) and variable attenuators are possible if the application requires them. Fig. 2 shows an example of the HW architecture of a BPM application.

Low power instrument

SoC requires less power than a multiple-board solution, and a proper selection of the RF components (amplifiers, analog-to-digital-converters (ADCs), etc.) reduces the amount of heat that the cooling system has to treat. This enables the way towards passive cooling with the integration of the heat sink in the crate. Consequently fans are no longer needed, and from the system point of view, the main advantages are:

- no moving parts means no maintenance required
- fans-induced noise is no longer present on the signals
- less space and less power required from the system.

With the low power requirement, precisely less than 15 Watt, the system can be powered over Ethernet according to the PoE standard IEEE802.3af.

In the case of accelerator applications, if the unit is powered over Ethernet, it is possible to put it closer to the machine (e.g. 5m), reducing at the same time the cost of cables and noise on the signal.

Easy SW maintenance

The unit software can be basically divided in the design that configures the FPGA and application and other interfaces supported by the operating system on the CPU side. The operating system running on Xilinx Zynq SoC is Linux OS.

In the presented platform, the software packages will not be installed in the device memory, but both FPGA and Linux code will be loaded from the same image when the unit is turned on. In more details two different boot procedures will be supported:

- ***memory card boot***: if a memory card is inserted in the device socket (see Fig. 2), then the Linux OS will boot from the image contained in the memory
- ***trivial File Transfer Protocol (TFTP) boot:*** if no memory is inserted, the boot procedure will start from the FLASH memory, and the software image will be downloaded from a configured TFTP server.

In both cases a software update can easily be realized replacing the software image in each unit, with no need to deal with packages and configuration files in the operating system. In particular for a complete set of units configured to use TFTP, only one image should be modified.

DESIGN CONCEPT FOR A BPM

The beam position monitor is the first application developed on this new platform, and 75 units will be installed in the ESRF booster ring [3].

Generally, the requirements for boosters are more relaxed compared with storage rings, and a resolution in the range of micrometers is more than enough. With a slight simplification of the measurement concept and the performances offered by this new platform, it is possible to match the requirements with an excellent price-to-performance ratio. Table 1 recaps part of the booster specifications that are important for the development.

Table 1: ESRF booster specifications

Parameter	**Value**
Circumference	300 m
Energy gap	200MeV – 6 GeV
RF frequency	352.2 MHz
Repetition rate	10 Hz
Required resolution	< 0.5 mm

The RF front-end should deliver the signals to the ADCs, achieving both wide bandwidth and good signal quality. With the low power constraint, a clever design of each stage is necessary, and the use of filters and amplifiers should be limited to the strictly necessary. Obtained bandwidth ranges from 300 MHz to ~500 MHz, and special Surface Acoustic Wave (SAW) filters will be placed to enhance the signal quality at required frequency, in this case 352.2 MHz.

Sampling frequency is programmable in a range from 80 MHz to 125 MHz. Selected ADCs support such sampling frequency and output 14-bit data.
Data acquisition is started either providing an external trigger signal (see Fig. 2) or using the SW trigger functionality, with a 10 Hz maximum rate that meets the ESRF specifications. Samples acquired through ADCs are then processed in the FPGA through three different data paths and stored in different memory buffers, as shown in Fig. 3.

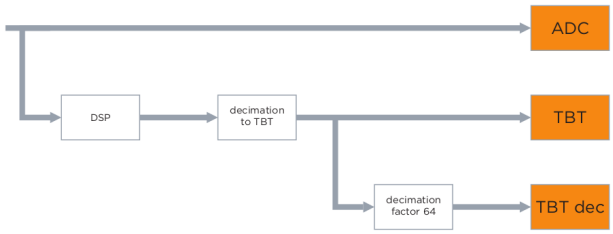

Figure 3: Data-paths and buffers overview.

- ***ADC raw data***: raw samples acquired at the sampling frequency, stored in a buffer with capacity 1 Msample.
- ***TBT data***: ADC samples regarding a whole turn in the ring are processed by a digital-down-conversion (DDC) algorithm using filters whose parameters are optimized for the machine physical dimensions and RF frequency. Data stored in the buffer are I and Q samples of each chain. Reducing the bandwidth, also the noise contribution is lower, and a better position resolution is then achieved. Its capacity is 256k samples.
- ***TBT-decimated data***: this buffer contains the data stored in the TBT buffer, after a decimation with factor 64. Its capacity is the same as the TBT buffer.

On the CPU side, data stored in the buffers can be further processed in order to deliver a more complete set of information to the user: from I and Q, also X and Y and sum signals are available. The position is computed using difference over sum formulas, and proper parameters can be tuned to remove offsets and adjust the gain.

The upper software layer provides the communication interface with the instrument. This is based on Standard Commands for Programmable Instruments (SCPI) specifications. Integration in the accelerator control system environment (EPICS, TANGO, etc.) can easily be done either implementing a specific server in the unit or using an external device server.

The development of the instrument is on the way with first prototype boards produced – see figure 4. First results of the measurements of the HW and ADC buffer part are within the specifications:

- crosstalk between RF channels is better than -60 dB
- expected position resolution at turn-by-turn frequency of 1 MHz is in the range below 10 micro-meters
- PoE functionality and boot options work properly.

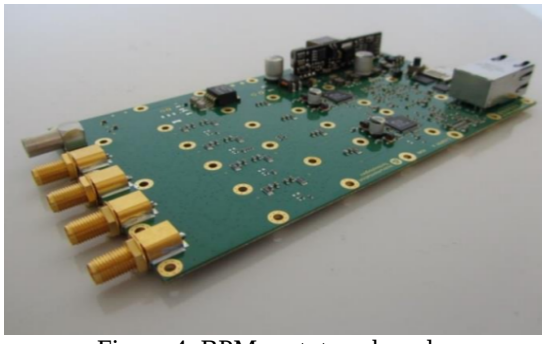

Figure 4: BPM prototype board.

CONCLUSIONS

The development of a new compact electronics based on the SoC technology has been presented in this article. The introduced platform combines knowledge about reconfigurable RF front-ends with the advantages of a compact and passively cooled instrument that can be powered over Ethernet and booted from a server using only one SW image.

It is intended to be the base for several applications, but the BPM case is the first of these and is described in details. Many others such as RF digitizers, BLMs and beam current monitors will come in the future. FPGA and CPU software will be provided to the user in order to give the opportunity to extend and optimize the instrument's original functionalities.

As a first development, the BPM prototype is a promising application that shows very good performance, simple and straightforward architecture and an interesting price-to-performance ratio.

REFERENCES

[1] G. Jug, M. Cargnelutti, K. B. Scheidt, "Development of Compact Electronics Dedicated to Beam Position Monitors in Injectors and Boosters" IBIC'13, Oxford, September 2013, WEPC18.
[2] Xylinx Zynq-7000 web page: http://www.xilinx.com/content/xilinx/en/products/silicon-devices/soc/zynq-7000.html
[3] ESRF booster specifications: http://www.esrf.eu/Accelerators/Accelerators/Booster