

MTCA.4 Timing Module Development

Rok Hrovatin, 6th Workshop on ATCA and MicroTCA for Physics, June 2012, Berkely, CA

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Overview

- Background
- General considerations
- Event Receiver Module
- Schedule

Two Platforms

- uTCA for Physics (particular applications)
- Libera Platform B (uTCA based, since 2009)



Libera Platform B

Hardware

- Chassis & Computer
- Processor module
- Timing module
- GDX module

Software

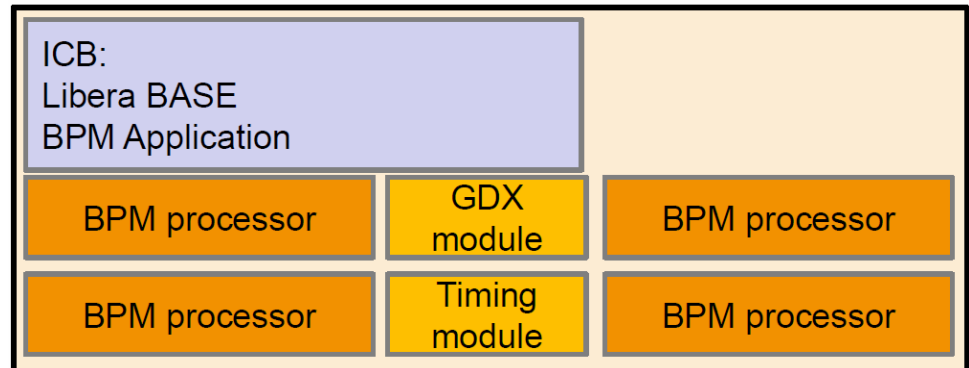
- LiberaBASE

Application (on top)

- LLRF
- Beam position processors



Schematical overview



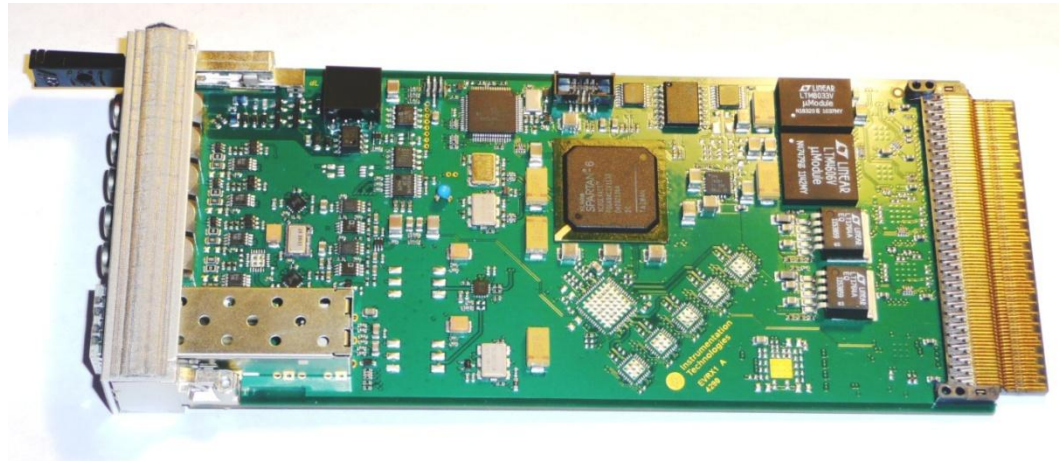
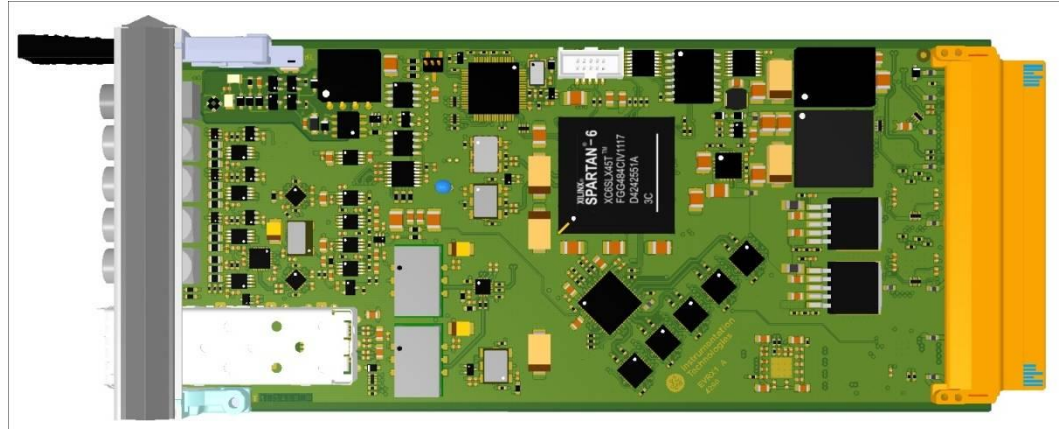
Extending the platform range

- The need for EvRX arose in Libera platform B segment
- User's requirements (data requirements besides pure timing signals, operating with MRF protocol)
- Being "uTCA-based" the development of EvRX module was obvious for both platforms

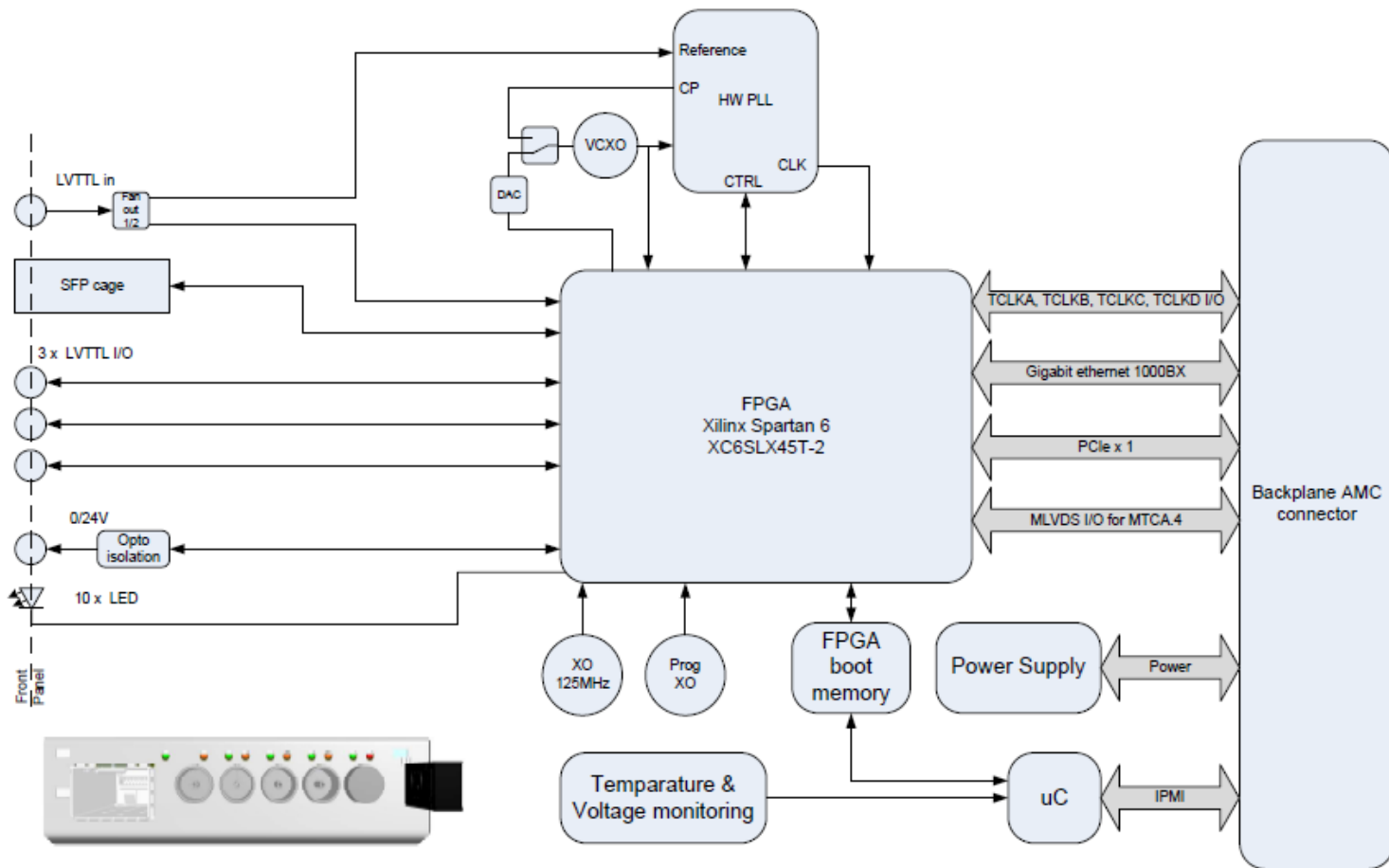


EvRX module

- Single Width / midsize AMC
- 4 x LEMO coaxial for trigger inputs / outputs
- 1 x LEMO differential for interlock output (24V)
- 1 x SFP cage - optical receiver input
- backplane pins configurable with pull-down resistors



Module schematic



Triggering mechanism

- RTC (Relevant Trigger Coding) added to the trigger sources – 16 bit MRF protocol
- RTC tables are defined for mapping 16-bit EVRX codes into 4-bit internal codes
- Basic mechanism: The mask (M) is used to select the bits from the incoming event. If masked event matches the function (F) then the serial code (S) is sent over the trigger link.
 - SW: FPGA header, Kernel module, Board Management Controller (BMC)
 - Possibilities for implementation of other protocols (WR)
 - Dual designation of channels allows for Event Generator.

Schedule

- Basic functionality set is confirmed for Libera platform B.
- Final performance tests are ongoing.
- Delivery of first boards in August.
- Final confirmation: interoperability Wshop (October)
- Official presentation of the EvRX module:
Libera Workshop (October)
<http://www.i-tech.si/announcements/8th-annual-libera-workshop>



Thank you